International Journal of Electrical and Computer Engineering (IJECE)
Vol. 8, No. 3, June 2018, pp. 1467~1477
ISSN: 2088-8708, DOI: 10.11591/ijece.v8i3.pp1467-1477

I_{DDQ} Testing of Low Voltage CMOS Operational Transconductance Amplifier

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Article Info

Article history:

Received Dec 20, 2017
Revised Feb 19, 2018
Accepted Mar 9, 2018

Keyword:

Bridging faults
Build in current sensor (BICS)
Open faults
Circuit under test (CUT)
Fault injection transistor (FIT)
I_{DDQ} testing
Operational transconductance amplifier (OTA)

ABSTRACT

The paper describes the design for testability (DFT) of low voltage two stage operational transconductance amplifiers based on quiescent power supply current (I_{DDQ}) testing. I_{DDQ} testing refers to the integral circuit testing method based upon measurement of steady state power supply current for testing both digital as well as analog VLSI circuit. A built in current sensor, which introduces insignificant performance degradation of the circuit-under-test, has been proposed to monitor the power supply quiescent current changes in the circuit under test. Moreover, the BICS requires neither an external voltage reference nor a current source and able to detect, identify and localize the circuit faults. Hence the BICS requires less area and is more efficient than the conventional current sensors. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. Both bridging and open faults have been analyzed in proposed work by using n-well 0.18µm CMOS technology.

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1. INTRODUCTION

Testing of the low-voltage large VLSI circuits is the critical portion of the circuit designing and implementation. Current measurement based testing has been very effective in detecting physical defects such as open, shorts and bridging defects [1], [2]. I_{DDQ} testing is a current-based test method that does not require propagation of a fault effect to an observe output. It requires only exercising the fault circuit and then calculating the current from power supply. The fault is observed by the measurement of current which exceed some threshold limit. The circuit draws a very low current (µA) in the quiescent state but for the certain input state this current may raise to an abnormal level due to the presence of faults [3], [4]. I_{DDQ} test methodologies can be classified into two groups, external (off- chip) and internal (on-chip) I_{DDQ} testing. External I_{DDQ} testing monitors supply current through the power pins of the integrated circuit package while internal I_{DDQ} testing monitors power supply current through the built-in current sensors (BICS). On-chip built-in current sensors are advantageous over off-chip current sensors for detecting the defective quiescent current due to better discrimination and higher testing speeds [5]. Figure 1 shows the block diagram of the I_{DDQ} testing with BICS.

I_{DDQ} testing can be done by adding BICS in series with power supply (VDD) or ground (GND) lines of the circuit under test. A series of input stimuli is applied to the device under test while monitoring the current of the power supply (VDD) or ground (GND) terminals in the quiescent state conditions after the

inputs have changed and prior to the next input change. The steady state or quiescent current testing of CMOS integrated circuits is known to be very efficient for improving test quality [6]-[8].

I_{DDQ} testing can be used as a reliability predictor due to its ability to detect defects that do not yet involve faulty circuit behavior, but could be transformed into functional failures at an early stage of circuit life. Thus, I_{DDQ} testing became a powerful complement to the conventional logic testing. Under the fault conditions, the normal values of quiescent current may be increased, decreased or generally distorted. Thus, fault detection can be accomplished by monitoring the quiescent current fluctuations using a current sensing circuit. Any current above the quiescent current would indicate the presence of physical defects in the circuit. In this paper, a simple built-in current sensor (BICS) is presented to detect short (Bridging) and open fault in low voltage two-stage CMOS operational transconductance amplifier with fault injection transistor [9]-[11].

The format of this paper is as follows; two stage operational transconductance amplifiers are discussed in Section 2. Section 3 introduces fault modeling whereas Section 4 describes the design consideration for BICS. Test simulation results and discussion are given in Section 5 and Section 6 contains conclusions.

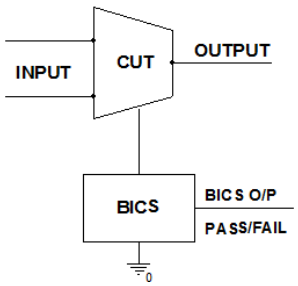

Figure 1. Block diagram of I_{DDQ} testing

2. TWO STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

In high performance analog integrated circuits, operational transconductance amplifier with very high DC gain and high unity gain frequency are needed to meet both accuracy and fast settling requirements of the systems [12]. Therefore, two-stage CMOS OTA are considered ideal for above requirement. Operational transconductance amplifier is voltage controlled current source whose differential input voltage produces an output current. An OTA is basically an operational amplifier (OPAMP) without an output buffer. It can drive only capacitive loads. The OTA can also be defined as an amplifier where all nodes are at low impedance except the input and output nodes. The characteristic feature of an ideal transconductance amplifier is that it has infinite input and output resistances. There is usually an additional input for a current to control the amplifier transconductance. It replaces operational amplifier because of its high bandwidth, high voltage swing, high SNR, low power dissipation, and high input impedance even at low voltages and low power. OTA constitute as a major building block in the analog designing due to its unique characteristic suited for applications such as gain control, multiplexing, comparator, analog modulation, active-c filter, oscillator etc. The OTA is a current-mode circuit and a versatile amplifier which convert input voltage to linearly proportional output differential current with transconductance gain (G_m). At higher frequencies, they provide more reliable performance due to its current mode operation. OTAs provide highly linear tenability of their transconductance (G_m) [13], [14]. In OTA the output current is linear function of differential input voltage as shown in Equation (1).

$$I_{OUT} = G_m V_{in} \quad (1)$$

Where G_m is the transconductance gain, I_{OUT} is output current and V_{in} is the input voltage.

The basic circuit diagram of two-stage OTA is shown in Figure 2 with differential amplifier and current mirror as first stage which convert differential input to single–ended output. The transistor M6 serves as P-channel common source amplifier which is the second stage of op-amp which provides high voltage swing. IBIAS of the circuit goes through current mirrors formed by P-channel MOSFETS, M8, M5 and M7. The sizes of the transistors are designed for a bias current of 113 µA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.

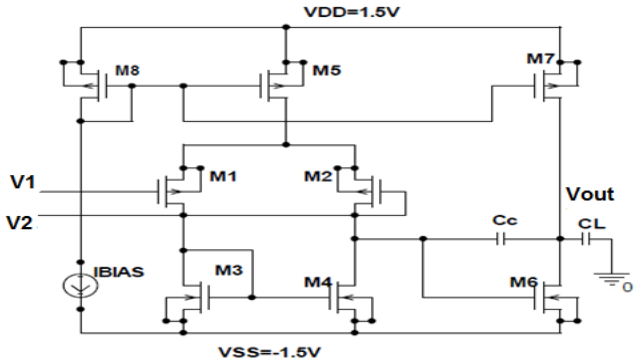

Figure 2. Schematic diagram of two stage CMOS OTA

3. FAULT MODELING

3.1. Fault type

In analog or mixed-signal integrated circuits, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS) [15], [16]:

a. Bridging Faults: Bridging Faults are the short circuit between two different layers in very large scale integrated circuits, caused because of unexposed photo resist, presence of a foreign particle, metallization defect, scratch on the mask etc., are popularly termed as bridging faults. Bridging fault could be between the following nodes: 1) drain and source, 2) drain and gate, 3) source and gate, and 4) bulk and gate. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate.
b. Gate-Oxide Short Defects: The defect causing a short between the gate and one of the other regions of a MOS transistor (drain, source or substrate) is gate-oxide short. A MOS transistor having a GOS may show gate current some orders of magnitude beyond the normal values depending on the device biasing.
c. Open Fault: Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state and cause elevated I_{DDQ} Node. Open defects are not only caused during fabrication but also because of extreme circuit operation conditions.

The faults considered in this study comprise open and bridging faults.

3.2. Fault injection transistor (FIT)

Fault injection transistor (FIT) basically n-MOS transistor is used for inducing bridging faults in the system to measure the fault tolerance or robustness of the system. The fault in the CUT can be activated by the fault injection transistor. Moreover, the use of a FIT for the fault simulation prevents permanent damage to the CUT by introduction of a physical metal short and also enables the operation of the CUT without any performance degradation in the normal mode. When FIT is inactive, CUT operates in normal mode while CUT work in test mode, when FIT is activated without affecting the overall operation of the circuit.

4. DESIGN CONSIDERATION OF BICS

In I_{DDQ} testing, the BICS embedded in series with VDD or GND lines of the CUT checks whether the quiescent current is below or above a threshold level. The existence of fault without performance degradation of CUT is indicated by proposed BICS. For effective use of internal testing, the BICS must minimize the effect of capacitance and voltage drop and achieve minimum disturbances in the CUT [17]-[19].

In the present work, a simple design of a BICS is presented to detect short faults and open faults on CMOS OTA as shown in Figure 3. Current mirror circuit is an essential element of the proposed BICS in which the reference current in one branch of the circuit is accurately reproduced in the other branch, in a constant current stage. BICS's ability to detect abnormal current due to physical defects depends on performance of current mirror. It consists of a current differential amplifier (M12, M13), two current mirror pairs (M11, M12 and M13, M14) and an inverter. The n-MOS current mirror (M11, M12) is used to mirror the current from the constant current source which is used as the reference current IREF for the BICS. The current mirror (M13, M14) is used to mirror the difference current (IDEF-IREF) to the current inverter, which acts as a current comparator. The differential pair (M12, M13) calculates the difference current between the reference current IREF and the defective current IDEF from the CUT. The W/L size of the n-MOS current mirrors (M11, M12) is set to 3.03/.18 and (M13, M14) is set to 8.1/.18. The constant reference

current is set to approximately the same value as the quiescent state current when the BICS in Test Mode. Any external voltage or current source is not required in the proposed BICS [20].

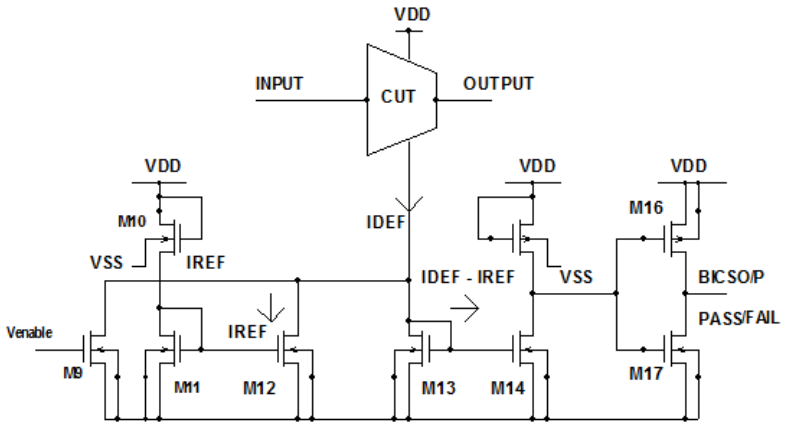

Figure 3. CMOS Built-in Current Sensor (BICS) with the CUT

The CUT works in two modes: the normal mode and the test mode. In the normal mode, the BICS is totally isolated from the CUT so that the operation of CUT is not affected by the BICS. In the test mode, the CUT is connected to the BICS. The Venable signal which is applied to the gate of transistor M9 decides the mode of operation of CUT. During the normal mode, the 'VENABLE' signal is at logic '1' and all the IDD current flows to ground through M9 (enable transistor) whereas during the test mode, the 'VENABLE' signal is at logic '0', the quiescent current from the CUT is diverted in to the BICS and compared with reference current to detect the presence of the fault. When the quiescent state current is greater than the reference current, the output signal PASS/FAIL is set to 1, which indicates the existence of fault in the circuit. When the quiescent state current is less than the reference current, the output signal PASS/FAIL is set to 0, which indicates the nonexistence of fault [21]-[24].

The built-in current sensor of the present work requires less area and is more efficient than the conventional current sensors. It is shown that with the use of a novel fault injection technique, combined with a built-in current sensor design, has significantly improved the testing of mixed signal integrated circuits.

5. SIMULATION RESULTS AND DISCUSSION

The fault coverage is achieved by the I_{DDQ} test approach based on the simulated results obtained from PSPICE (Cadence PSPICE A/D Simulator) simulations. SPICE level 7 MOS model parameters used in simulation. The CUT is simulated using 0.18µm n-well CMOS technology. Figure 4 shows the simulated output of CUT without BICS. When CUT is given a pulse signal of 1.5V and 1V peak-to-peak, the output obtained is a pulse wave of 1.8V peak-to-peak. The simulated output response of CUT with BISC when fault are not activated i.e. when fault free circuit with BICS is in normal mode is shown in Figure 5. Since the output of CUT is 1.5V peak-to-peak, we can see that there is no performance degradation of the CUT with BICS. In the present work, seven bridging faults viz., short between gate and drain of M3 transistor (XFIT1 1-M3GDS), drain-source short of M4 transistor (XFIT2-M4DSS), drain-source short of M6 transistor (XFIT3-M6DSS), gate-drain short of M2 transistor (XFIT4-M4GDS), drain-source short of M7 transistor (XFIT5-M7DSS), drain-source short of M5 transistor (XFIT6-M5DSS), gate drain short of M5 transistor (XFIT7- M5GDSS) and one open fault of M7 transistor (XFIT8-M7) have been introduced in CUT with BICS as shown in Figure 6. During the test mode, the 'Venable' signal is at logic '0' and fault injected transistor are activated using error signal Ve1, Ve2, Ve3, Ve4, Ve5, Ve6, Ve7 and Ve8 respectively. The value of W/L of FIT is taken as 3.5/0.18. The load capacitance is assumed to be 3pF.

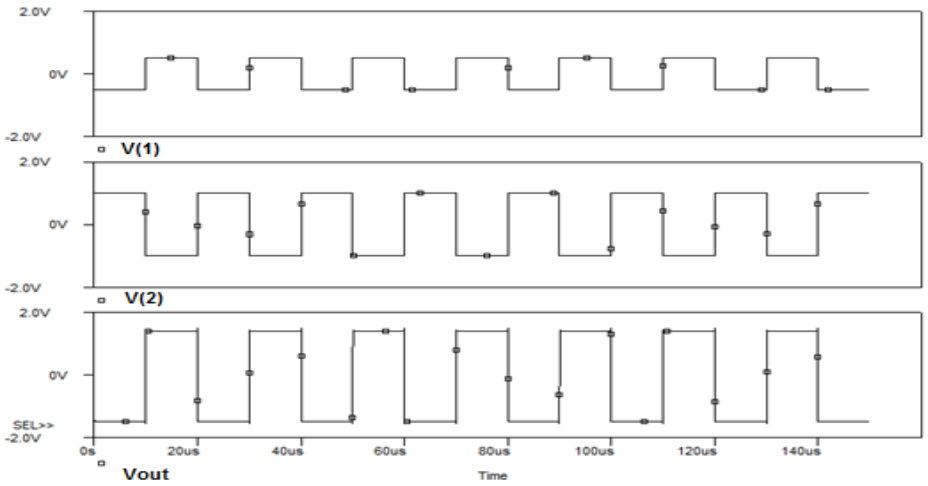

Figure 4. Simulated input and output response of Two stage CMOS OTA without BICS

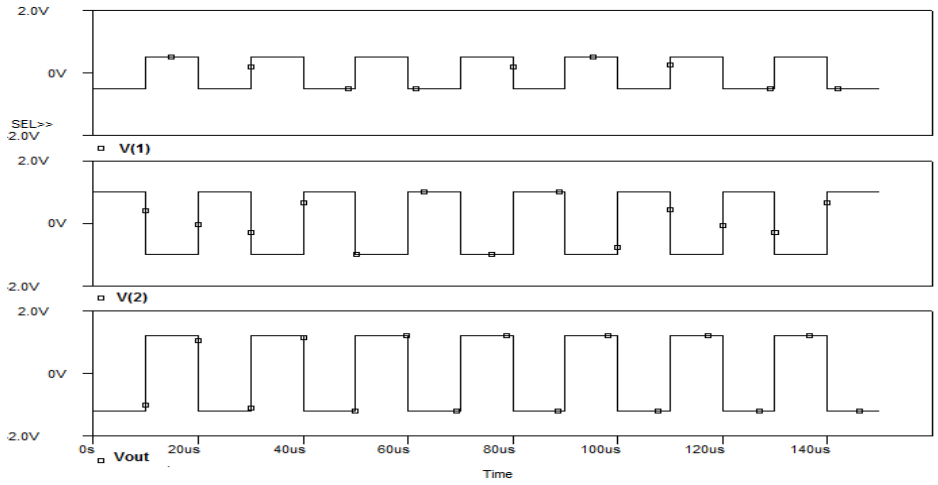

Figure 5. Simulated input and output response of CUT with BICS (Without Fault)

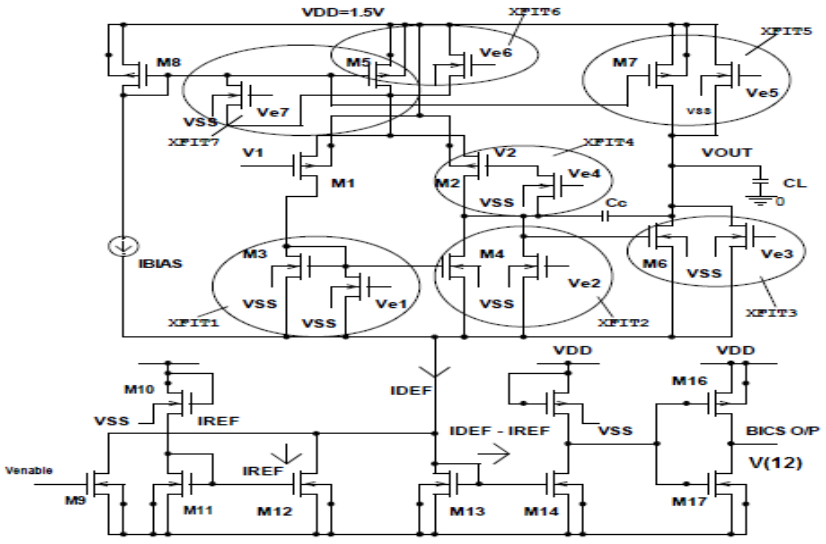

Figure 6. Schematic diagram of CMOS OTA with BICS and Seven FITs

The simulated BICS output when the fault XFIT1 is activated with Venable signal low and Ve1 high i.e. when CUT is in test mode is shown in Figure 7. We can see that BICS output PASS/FAIL is at logic '1' during the period when fault XFIT1 is activated and thus the fault XFIT1 is detected. Similarly Figure 8 to Figure 14 shows the simulated BICS outputs when faults XFIT2, XFIT3, XFIT4, XFIT5, XFIT6, XFIT7 and XFIT8 are activated with Venable signal low and Ve2,Ve3, Ve4,Ve5, Ve6, Ve7and Ve8 high respectively. We can observed from the results that except faults XFIT2, XFIT3 and XFIT8, all the other faults have been detected by proposed test methodology providing high fault coverage. From the simulated result, since the output signal PASS/FAIL is 1 only when faults are activated with Venable signal at logic 0, we can observed that the proposed BICS detects the faults. Consequently, we know the proposed BICS detects perfectly a defective circuit.

The average power dissipation, the propagation delay time and transition time are also analyzed to compare the performance of the CUT without BICS and the CUT with BICS. Table 1 lists the simulation results of the power dissipation, propagation delay time and the transition time. The average power dissipation of CUT without BICS and with BICS is 1.1mW and 1.3mW, respectively. Therefore, the average power dissipation overhead is about 15.38% due to the inclusion of the proposed BICS. The low-to high-level transition time of CUT without BICS and CUT with BICS are 0.5ns and 0.9ns, respectively, while the high-to-low-level transition time without BICS and with BICS are 1.5ns and 1.6ns, respectively whereas 3ns and 3.2 ns respectively are the average propagation delay time of CUT without BICS and with BICS. Therefore, we can conclude from the simulations results that the performance degradation is negligible.

Table 1. Simulation Result of each Parameter

Parameters	CUT without BICS	CUT with BICS
P_D	1.1mW	1.3mW
t_{PD}	3ns	3.2ns
t_{TLH}	0.5ns	0.9ns
t_{THL}	1.5ns	1.6ns

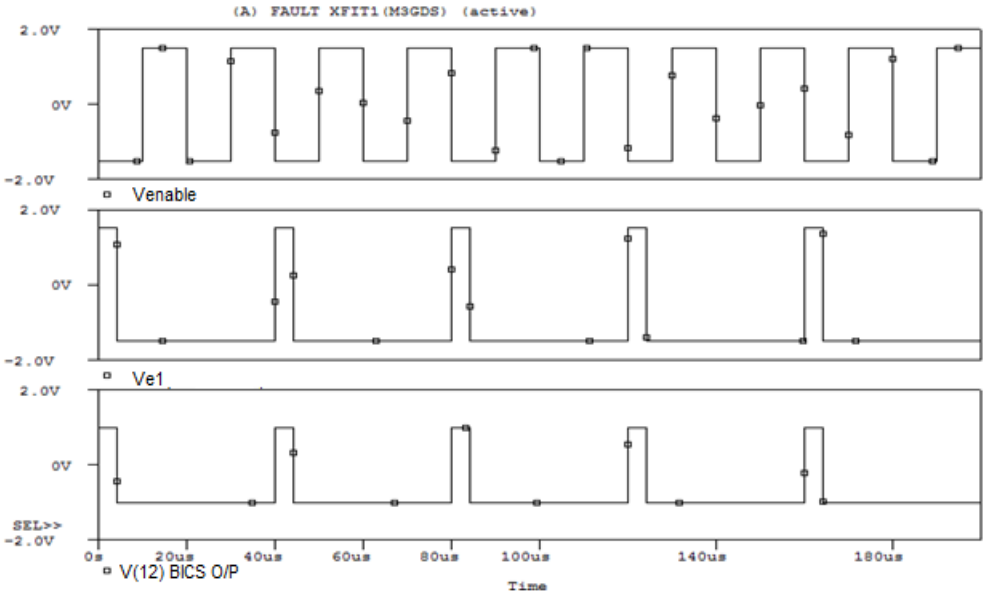

Figure 7. Simulated BICS O/P of CUT when error signal 1(Ve1) for fault XFIT1 (M3GDS) is activated

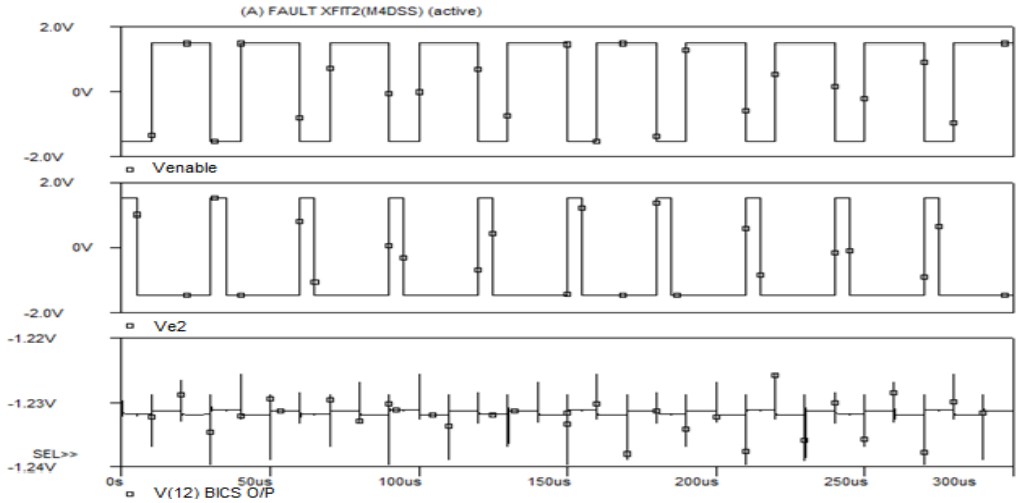

Figure 8. Simulated BICS O/P of CUT when Error signal 2 (Ve2) for fault XFIT2 (M4DSS) is activated

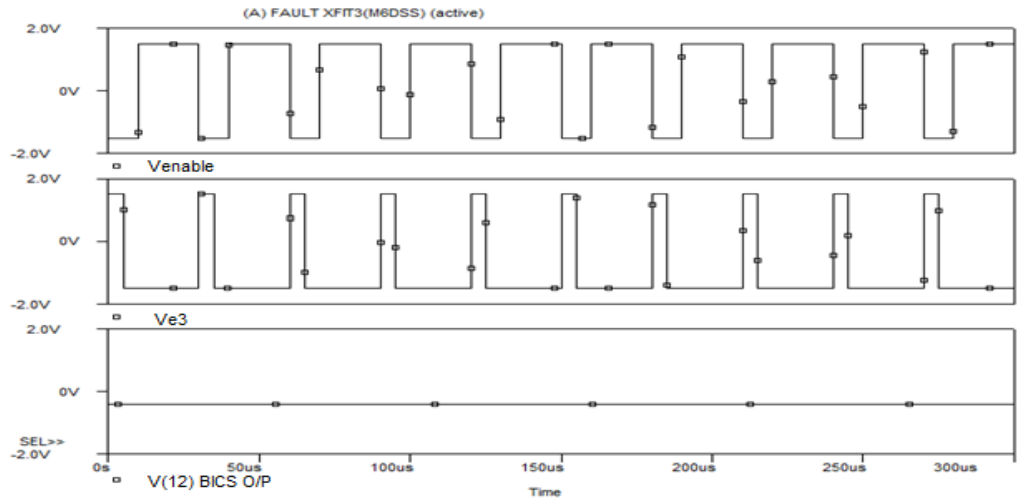

Figure 9. Simulated BICS O/P of CUT when Error Signal 3 (Ve3) for fault XFIT3 (M6DSS) is activated

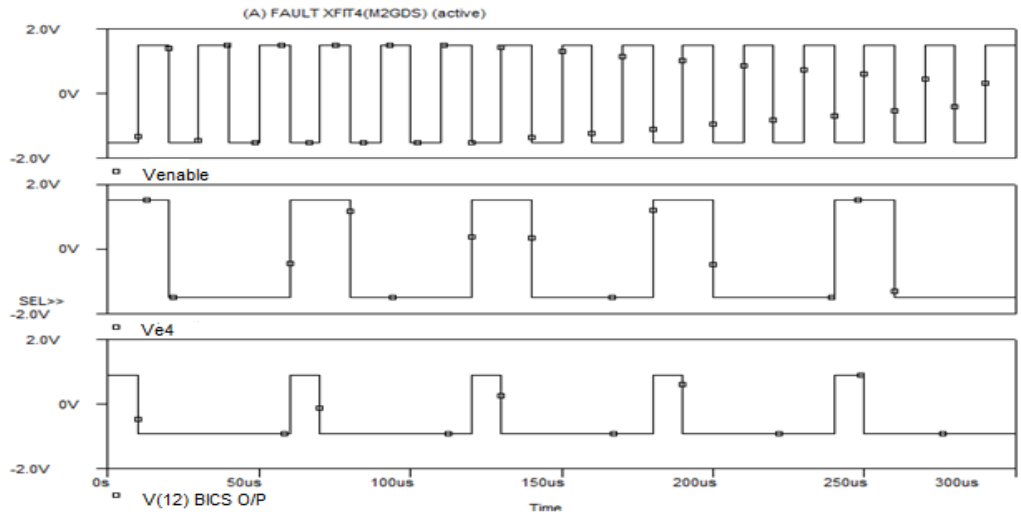

Figure 10. Simulated BICS O/P of CUT when Error Signal 4 (Ve4) for fault XFIT4 (M2DGS) is activated

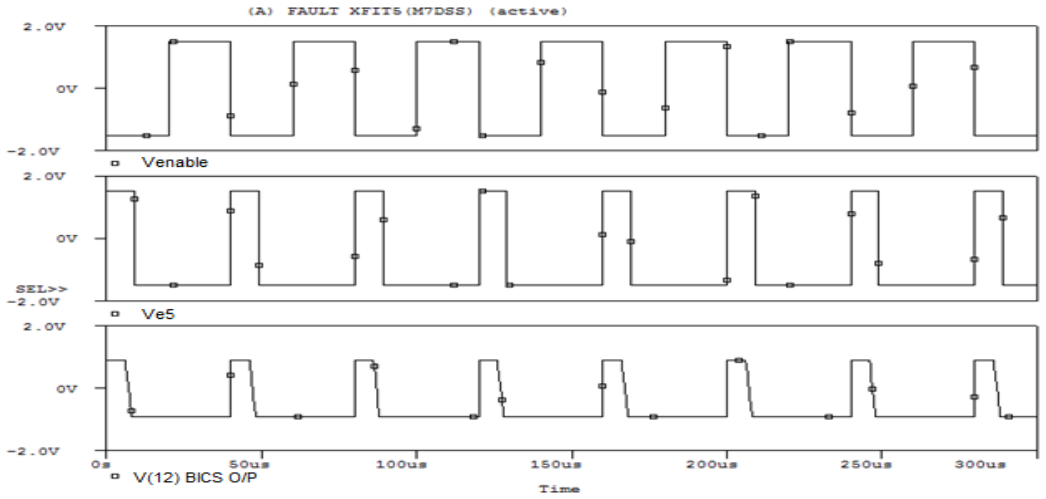

Figure 11. Simulated BICS O/P of CUT when Error Signal 5 (Ve5) for fault XFIT5 (M7DSS) is activated

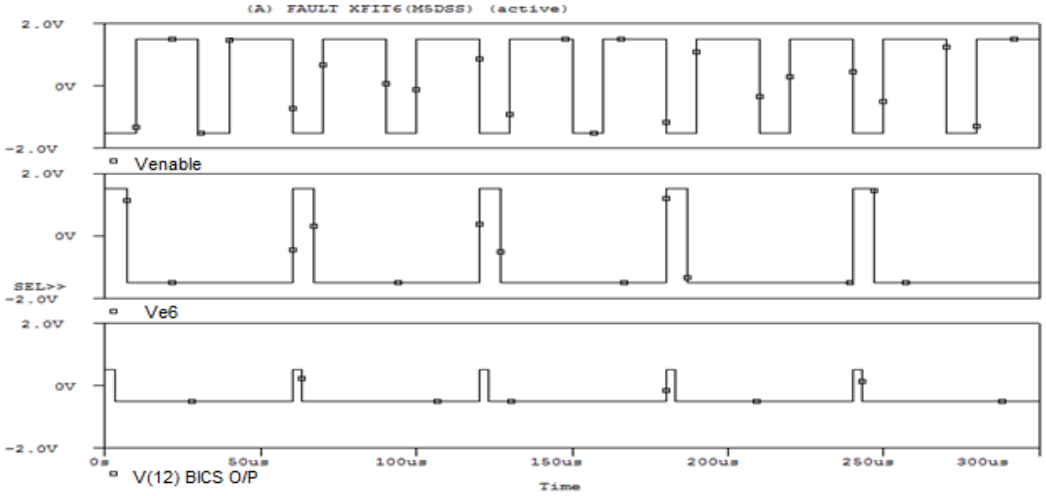

Figure 12. Simulated BICS O/P of CUT when Error Signal 6 (Ve6) for fault XFIT6 (M5DSS) is activated

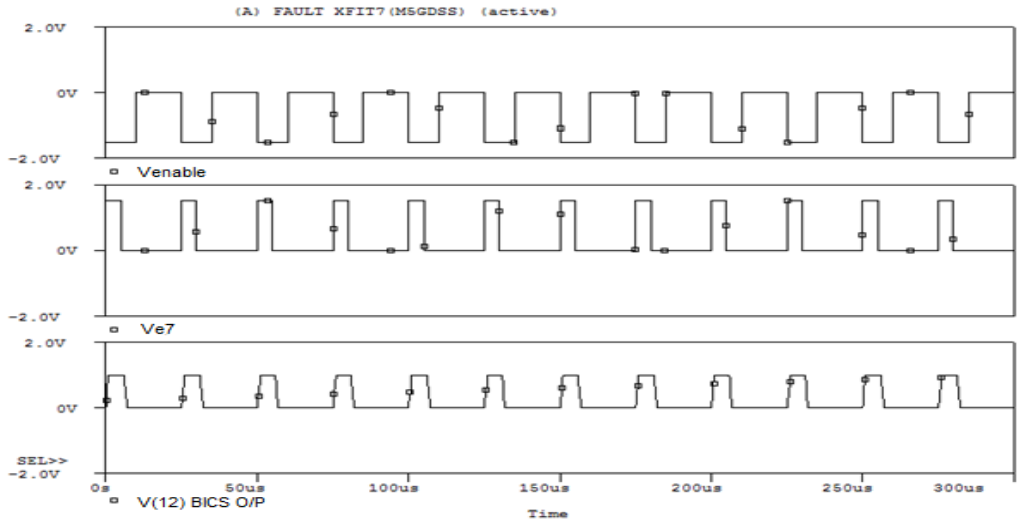

Figure 13. Simulated BICS O/P of CUT when Error Signal 7 (Ve7) for fault XFIT7 (M5GDS) is activated

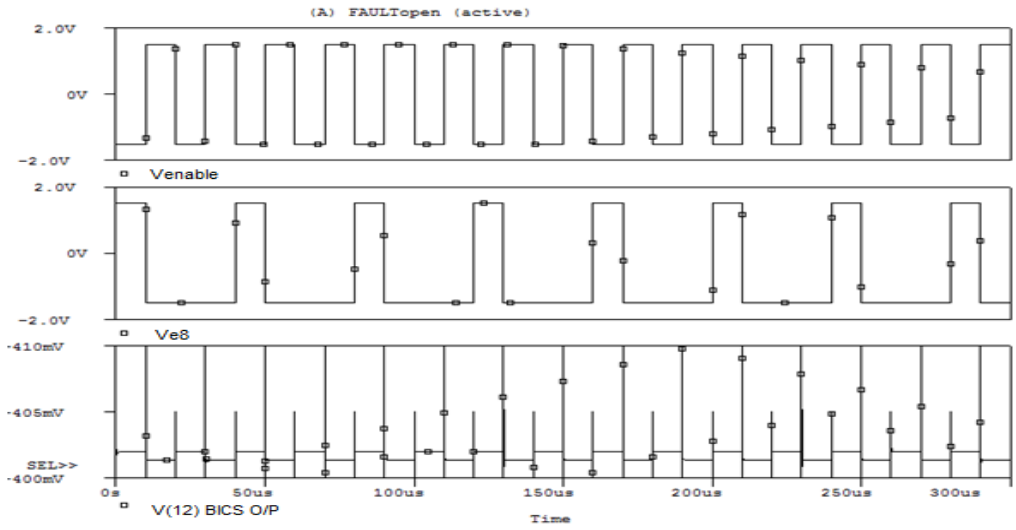

Figure 14. Simulated BICS O/P of CUT when Error Signal 8 (Ve8) for Open fault XFIT8 is activated

Table 2 shows the simulated fault coverage by I_{DDQ} test methodology. It is concluded from the results that total fault coverage is 62% which includes seven short and one open fault.

Table 2. Simulated Fault Coverage of I_{DDQ} Testing

Fault Type	Total Fault Injected	Fault Detected	Fault Coverage (%)
Short	7	5	71
Open	1	0	0
Total	8	5	62

Table 3 summarizes the comparison of the proposed BICS and the previous published BICS. Although a direct comparison cannot be made because the BICS are designed in different technologies, some important results can be drawn from the table. The proposed BICS requires the least devices, i.e., seven transistors and one inverter, among all designs. The BICS does not require any clock signal as well as an external voltage reference or a current source. Hence, the BICS has negligible performance degradation. Furthermore, mode selection is provided which is more economical than other designs. Consequently, it is obvious that this design is competitive with previously proposed BICS's.

Table 3. Comparison of the Proposed BICS and Previous published BICS

	Number of Elements	Technology Used	Clock Signal	Mode Select	Control Pin	Voltage Degradation	Output Pin
Nigh's Design [17]	Transistor: 10 Inverter: 2	3 µm	Two Phase Clock	Y	3	Exists	1
Maly's Design[18]	Transistor: 10 Inverter: 2 NAND:1	2 µm	Single Clock	Y	5	Exists	1
Shen's Design [19]	Transistor: 1 Diode:1	2 µm	Two Phase Clock	N	3	Exists	1
Miura's Design [20]	Transistor: 16 R: 2 C:1	0.35 µm	Not Used	Not Reported	3	Reduced due to using more than one supply voltage	1
Tang's Design [21]	Transistor: 10 Inverter: 2 NAND:1	0.8 µm	Single Clock	N	3	Reduced using OP AMP to adjust supply of CUT	1
Ahmed Design [22]	Transistor: 48	0.25 µm	Not Used	N	-	Negligible	-
Proposed Design	Transistor:7 Inverter: 1	0.18µm	Not used	Y	2	Negligible due to presence of two modes of operation	1

6. CONCLUSION

In this paper, I_{DDQ} testing technique has been explored on low voltage two stage CMOS operational transconductance amplifier using PSPICE. The proposed BICS design converts the current difference between a faulty current and the reference current to a voltage that differentiates between faulty CUT and fault free circuit. During the normal mode, the bottom of the CUT is connected to ground bypassing the BICS. Therefore, a level shift or disturbance on the output during normal mode of the CUT is avoided. The simulation and test results show that the proposed BICS functions correctly with negligible performance degradation of CUT, requires less area, no external reference source and provides high fault coverage. Hence, the proposed BICS is superior to other BICS's. Out of eight faults which include seven bridging and one open fault, five faults have been detected by this test methodology. Thus, I_{DDQ} testing methodology is a valuable tool to achieve high fault coverage and also improve reliability and quality of analog and mixed-signal CMOS integrated circuits without incurring significant test development cost. It is concluded that I_{DDQ} testing is very effective in detecting short faults. However, it may not detect an open fault.

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