Identification of Radiation Induced Dark Current Sources in Pinned Photodiode CMOS Image Sensors

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***Abstract*—This paper presents an investigation of Total Ionizing Dose (TID) induced dark current sources in Pinned PhotoDiodes (PPD) CMOS Image Sensors based on pixel design variations. The influence of several layout parameters is studied. Only one parameter is changed at a time enabling the direct evaluation of its contribution to the observed device degradation. By this approach, the origin of radiation induced dark current in PPD is localized on the pixel layout. The PPD peripheral shallow trench isolation does not seem to play a role in the degradation. The PPD area and an additional contribution independent of the pixel dimensions appear to be the main sources of the TID induced dark current increase. This study also demonstrates that applying a negative voltage on the transfer gate during integration strongly reduces the radiation induced dark current.**

***Index Terms*—Image Sensors, CMOS Image Sensors, CIS, Active Pixel Sensors, APS, Monolithic Active Pixel Sensors, MAPS, Pinned Photodiodes, PPD, Ionizing Radiation, Total Ionizing Dose, TID, Dark current, Leakage current, Charge Transfer, Transfer Gate, Shallow Trench Isolation, STI, Deep Submicron Process, DSM, Radiation Hardening, RHBD.**

I. Introduction

PINNED PHOTODIODES (PPD) [1]–[3] are widely used in state-of-the-art CMOS Image Sensors (CIS) for high and low end commercial applications such as cellphone where the market trend goes to decrease the pixel size as much as possible. These photodetectors are optimized for pixel pitches as small as 1 μm and are not always usable for scientific applications that require larger photodetector sizes (most often between 5 and 15 μm) for improved sensitivity. This is one of the reasons why many scientific applications still use the classical CMOS PN junction based pixel (also called 3T-pixel in its simplest form), but the benefit of pinned photodiode leads to a growing number of high performance scientific CIS based on these devices [4]. However, the behavior of PPD based sensors in ionizing radiation environment is not well understood today and this can limit their use in applications such as nuclear and particle physics, space applications or medical imaging.

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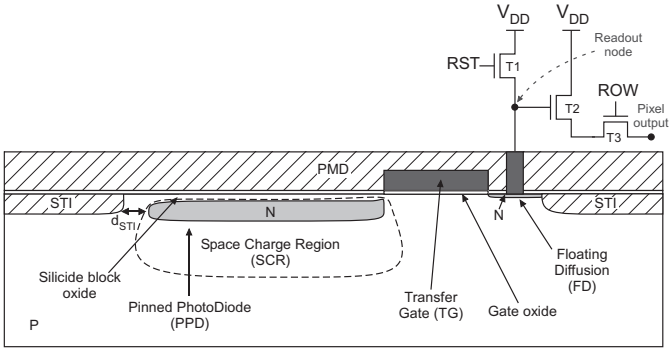

Fig. 1. Pinned photodiode pixel cross-section with a 4T-pixel architecture. The P+ pinning layer, the Pwell and STI sidewall passivation doping profiles are not represented for the sake of clarity..

Only few papers [5]–[9] have been published on the radiation tolerance of the pinned photodiode and its associated Transfer Gate (TG). All these studies pointed out that ionizing radiation induces a dark current increase in PPD sensors as in classical PN junction based pixels. From these studies, it cannot be clearly inferred what the main sources of this dark current increase are in such pixels. Shallow Trench Isolation (STI) and the TG are often suggested to be the main sources of radiation induced dark current [5], [7], [9], but there is no unquestionable evidence of these conclusions in well designed (i.e. with STI far enough from the PPD [5], [10]) and well biased pinned photodiode (i.e. with the TG completely accumulated during integration [11]). Moreover, since the radiation induced dark current sources are still not precisely localized on the pixel layout, efficient radiation-hardening-by-design guidelines cannot be established for PPD pixels.

In this paper, we present an investigation of Total Ionizing Dose (TID) induced dark current sources in PPD-CIS based on pixel design variations. The influence of several layout parameters is studied. Only one parameter is changed at a time enabling the correlation between the observed degradation and each parameter independently. The purpose of this work is to localize the radiation induced dark current sources in PPD CIS. Such identification is necessary to improve the radiation hardness of PPD and also to improve the reliability of CIS radiation tests.

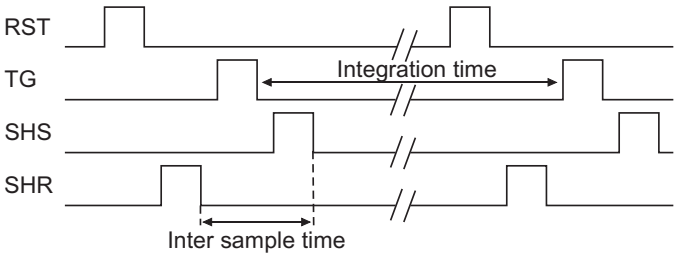

Fig. 2. 4T PPD pixel timing diagram illustration showing the integration time and the inter-sample time.

TABLE I
SUMMARY OF THE STUDIED PIXEL LAYOUTS. PERIM. STANDS FOR PERIMETER, W_{TG} FOR TG WIDTH AND CVF FOR CONVERSION FACTOR.

Name	PPD Area	PPD Perim.	W_{TG}	FD Perim.	CVF $\mu V/e^-$
Com	20 μm^2	39 μm	1.6 μm	3.5 μm	75
Area1	40 μm^2	39 μm	1.6 μm	3.5 μm	75
Area2	60 μm^2	39 μm	1.6 μm	3.5 μm	75
Area3	82 μm^2	39 μm	1.6 μm	3.5 μm	75
Perim1	20 μm^2	33 μm	1.6 μm	3.5 μm	75
Perim2	20 μm^2	25 μm	1.6 μm	3.5 μm	75
Perim3/Ref	20 μm^2	18 μm	1.6 μm	3.5 μm	75
TG1	20 μm^2	39 μm	1.6 μm	29 μm	16
TG2	20 μm^2	39 μm	5.8 μm	29 μm	16
TG3	20 μm^2	39 μm	10.0 μm	29 μm	16
TG4	20 μm^2	39 μm	14.0 μm	29 μm	16
FD1	20 μm^2	39 μm	1.6 μm	29 μm	16
FD2	20 μm^2	39 μm	1.6 μm	29 μm	23
FD3	20 μm^2	39 μm	1.6 μm	29 μm	35

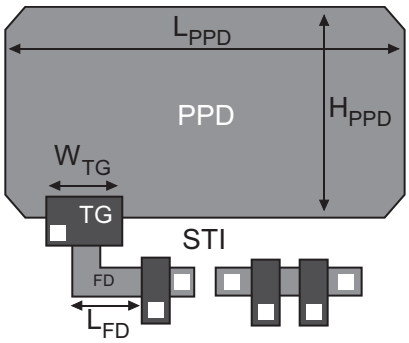

Fig. 3. Pinned photodiode pixel layout illustration with the parameters of interest in this work (PPD dimensions, TG width and FD perimeter).

II. SPECIFICS OF PINNED PHOTODIODES

A cross-section of a typical pinned photodiode is presented in Fig. 1. As can be seen in the figure, the simplest pixel architecture based on pinned photodiode uses one more transistor than the well-known three-transistor-per-pixel design (3T-APS). This architecture is very often called 4T-PPD-CIS or 4T-PPD Active Pixel Sensors (APS). It is important to note that the pinned photodiode in more-than-four-transistor-PPD-pixels will behave the same as in a 4T-PPD pixel, therefore understanding the 4T-PPD behavior in ionizing environment will help understanding the behavior of any pixel architecture based on PPD. In this figure, one can identify the three transistors used in 3T-pixel for resetting the floating diffusion, selecting the pixel and amplifying the collected charge converted into a voltage [12]. This conversion occurs in the Floating Diffusion (FD), which corresponds to the photodiode in a 3T-pixel except that it is a shallow N+/Pwell junction instead of an Nwell/Pepi (i.e. the P-type epitaxial layer) photodiode. The two major differences with the 3T architecture are the pinned photodiode itself and the transfer gate. The pinned photodiode can be described as a volume of N-doped region surrounded by a P doping. In this configuration, an optimized pinned photodiode is fully depleted and under non-equilibrium conditions, at the beginning of integration, acting as a potential well for photo-generated electrons. The surface P-doping concentration is high enough to prevent the space charge region of the photodiode to reach the top oxide and the Pwells prevent the depleted region from reaching the STI sidewalls. It should be emphasized that, contrary to 3T pixels, the space charge region of an optimized PPD does not touch any oxide, which should lead to extremely good ionizing radiation hardness. At the end of integration (see Fig. 2 for a detailed timing diagram[1]), the photo-generated electrons collected by the PPD potential well are transferred to the FD for readout. The FD is reset before the transfer and its value is sampled thanks to the SHR digital signal. Another sample is taken after the transfer (thanks to SHS), and the difference between these two samples allows the recovery of the amount of collected charges.

TABLE II
DESCRIPTION OF THE STUDIED ALTERNATIVE PPD LAYOUTS.

Name	Description
Round	Round PPD (no corner)
RadTol	Radiation tolerant design based on [6]
STI 0.5	PPD with $d_{STI} = 0.5$ μm
STI 0.75	PPD with $d_{STI} = 0.75$ μm
STI 1.0	PPD with $d_{STI} = 1$ μm

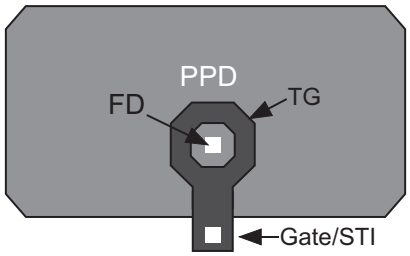

Fig. 4. Pinned photodiode layout illustration of the radiation tolerant structure based on the concept proposed in [6].

III. EXPERIMENTAL DETAILS

The studied sensors, divided into 32x32-pixel-regions, have been manufactured using a $0.18\mu m$ CMOS process dedicated to CIS. The selected pixel size is 10×20 μm^2 to allow the design of all the layout variations used in this study. The details of the manufactured pixels with geometric variation are presented in Tab. I. The geometric layout variations used for the study are presented in Fig. 3. Among these structures, pixel Perim3 will be used as a reference pixel since its photodiode dimensions are close to what can be found in a realistic

[1]A timing diagram as simple as possible has been voluntarily used to simplify the interpretations.

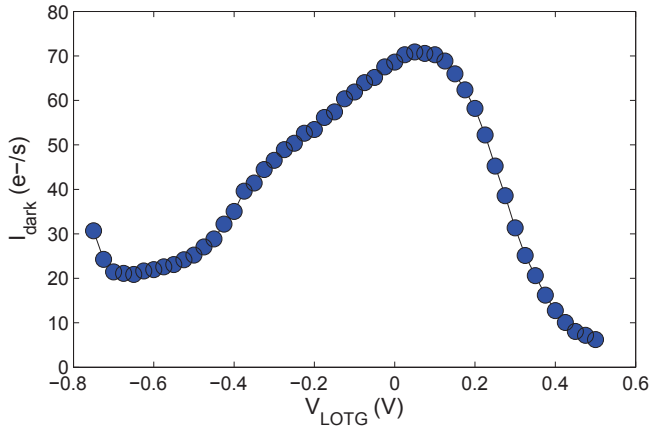

Fig. 5. Reference pixel (pixel Perim3) dark current evolution with transfer gate off voltage (V_{LOTG}) before irradiation.

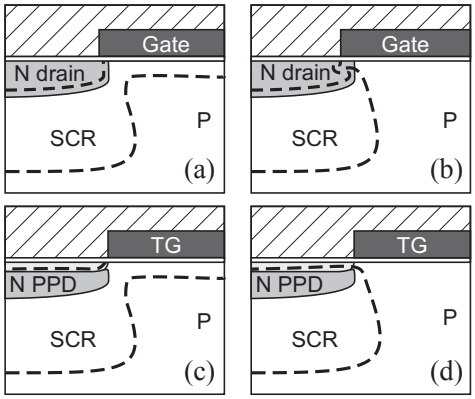

Fig. 6. Illustration of the similarities between a gated diode and a pinned photodiode. (a) Gated diode in depletion regime. (b) Gated diode in accumulation regime. (c) Pinned photodiode with TG in depletion regime. (d) Pinned photodiode with TG in accumulation regime.

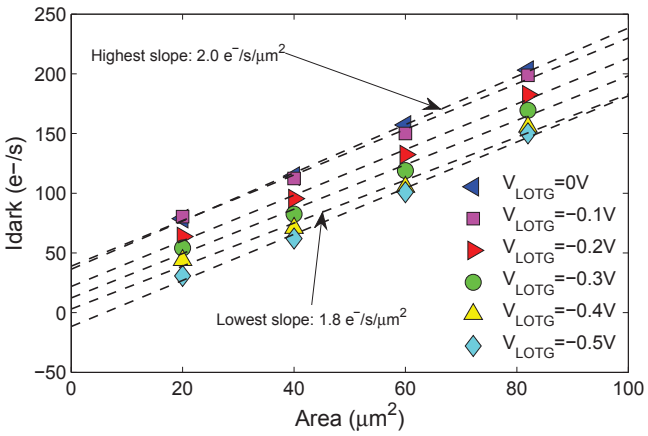

Fig. 7. Dark current variation with photodiode area for several V_{LOTG}, before irradiation (pixels Com, Area1, Area2 and Area3).

6 μm-pitch 4T-PPD pixel. In addition to these pixels, five alternative layouts have also been tested. They are described in Tab. II. A radiation tolerant pinned photodiode layout has been previously proposed in [6]. The RadTol pixel of Tab. II is based on this radiation tolerant design, as illustrated in Fig. 4[2]. The photodiode of the Round pixel has no corner. The layout of pixels STI 0.5, 0.75 and 1.0 are the same as the reference pixel (Perim3) but with STI recessed 0.5, 0.75 and 1.0 μm away from the photodiode layer (instead of 0.3 μm for all the other structures). These recess distances correspond to the distance d_{STI} shown at the top left of Fig. 1.

Dark current measurements were performed at 22°C regulated temperature, with no illumination. The dark current extraction was realized by averaging one hundred dark frames for several increasing integration times (between ten and fifty points in the linear region), and by computing a linear regression of the dark frame voltage as a function of integration time[3]. Some non-linearities were observed at the highest TID levels. In this case, the worst case dark current was used for the study (i.e. the linear regression was performed in the maximum slope region).

The test devices were exposed grounded to 10 keV X-rays, at CEA-DIF, thanks to an ARACOR model 4100 semiconductor X-ray irradiator. All the pins were grounded thanks to conductive foam. The absorbed TID ranges from 10 krad(SiO_2) to 150 krad(SiO_2) and the dose rate was about 100 rad(SiO_2)/s.

IV. Results and Discussion

A. Extraction of geometric contributions

During integration, the transfer gate is biased to V_{LOTG}, which is designed to turn it off. The value of V_{LOTG} has a strong influence on dark current as shown in Fig. 5 and as discussed in [11], [13], [14]. At zero voltage, the depletion region of the transfer gate merges with the depletion region of the PPD (Fig. 6c), leading to an intense dark current due to interface states located below the transfer gate. At negative voltage (in the $-0.5; -0.7$ V range), the transfer gate is in accumulation regime leading to the disappearance of the TG depleted region (Fig. 6d) and preventing the PPD space charge region to reach the oxide interface. Despite the intrinsic differences between a pinned photodiode and a conventional CMOS diode, this effect corresponds well to what is observed in a gated diode [15] as illustrated in Fig. 6. When the TG voltage is too low (i.e. below -0.7 V), it leads to an Electric Field Enhancement (EFE) of the leakage current [16]. It has been concluded in [17], that this EFE is a Trap Assisted Tunneling (TAT) effect as usually observed in MOSFETs [18] when a voltage much lower than the threshold voltage is applied on the gate (once again, as in a classical gated diode). The optimal accumulation voltage selected for this study is -0.6 V since it leads to the minimum dark current with a limited TAT EFE effect.

The PPD dark current can be decomposed in several contributions:

[2]Since the layout was not described in the original paper (only the cross-section was), the pixel layout used in this study may differ in some points from the layout used in [6].

[3]It should be emphasized that by doing so, the real dark current value is extracted (i.e. the rate at which dark electrons are generated), and the dark signal offset is suppressed. Indeed, if only a single integration time is used to study the dark current, the dark signal offset will be included in the measured value possibly leading to erroneous dark current value estimations.

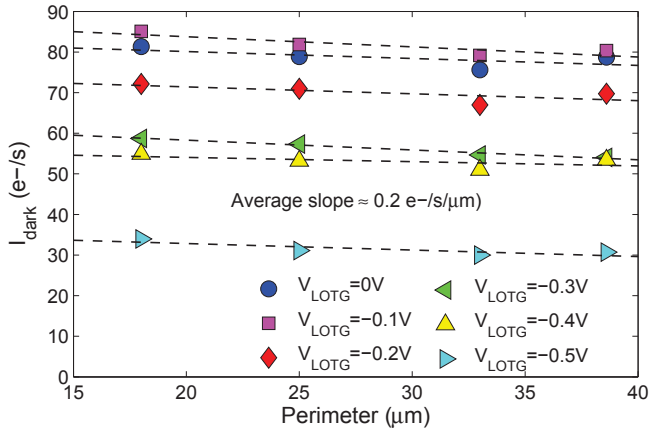

Fig. 8. Dark current variation with photodiode perimeter for several $\mathrm{V_{LOTG}}$, before irradiation (pixels Com, Perim1, Perim2 and Perim3).

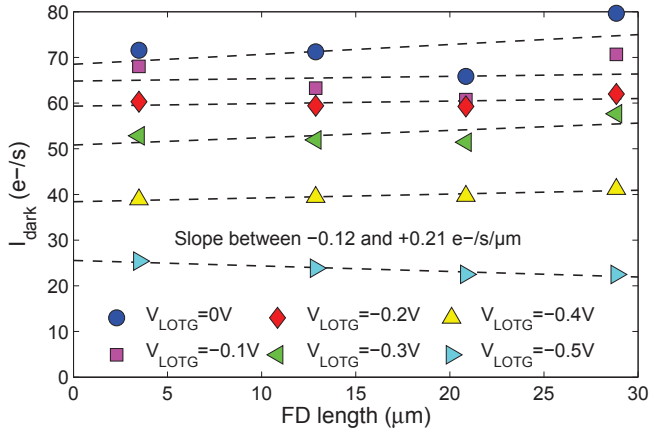

Fig. 9. Dark current variation with floating diffusion perimeter for several $\mathrm{V_{LOTG}}$, before irradiation (pixels Com, FD1, FD2 and FD3).

$$I_{\mathrm{dark}} = J_a A_{\mathrm{PPD}} + J_p P_{\mathrm{PPD}} + J_{\mathrm{TG}} W_{\mathrm{TG}} + J_{\mathrm{FD}} P_{\mathrm{FD}} + I_0 \quad (1)$$

with A_{PPD} the PPD area, P_{PPD} its perimeter, W_{TG} the transfer gate width, P_{FD} the floating diffusion perimeter and I_0 the remaining contribution which is not a function of the other parameters. In order to discriminate the different contributions, the evolution of dark current with each of these parameters is presented, before irradiation, in the following figures.

Fig. 7 shows the evolution of dark current with the PPD area and for several $\mathrm{V_{LOTG}}$. A clear correlation between the PPD area and the dark current appears and is quantified by the slope, J_a, of the linear regression (dashed line) between the area and the dark current. It is important to notice that the TG off voltage does not have any significant influence on the area contribution J_a which remains approximately equal to 1.9 $\mathrm{e^-.s^{-1}}.\mu\mathrm{m^{-2}}$. This area contribution is most likely dominated by the diffusion current coming from the silicon neutral volume surrounding the PPD depletion region.

Contrary to the area current source, Fig. 8 shows that there is no significant contribution from the PPD perimeter ($|J_p| < 1$ $\mathrm{e^-.s^{-1}}.\mu\mathrm{m^{-1}}$). Hence, the peripheral STI does not seem to play an important role in the pre-irradiation dark current in these devices. Exactly the same conclusion can be drawn on the influence of the FD perimeter ($|J_{FD}| <$

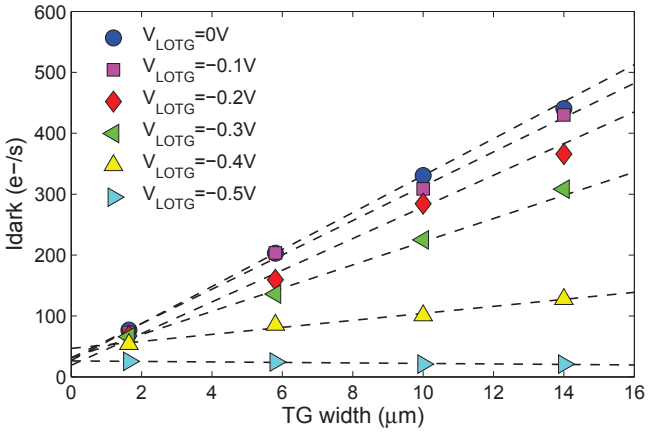

Fig. 10. Dark current variation with transfer gate width for several $\mathrm{V_{LOTG}}$, before irradiation (pixels TG1, TG2, TG3 and TG4).

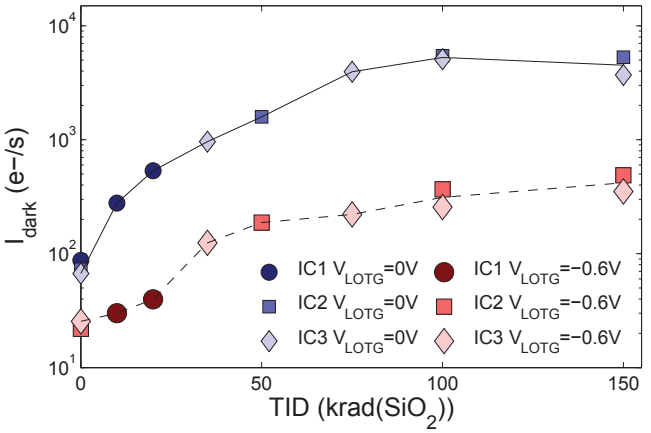

Fig. 11. Reference pixel dark current evolution with TID (pixel Perim3). The figure also shows how many devices have been used and which TID has been received by each device. In the following figures, only one value is given by TID level (the average value).

0.3 $\mathrm{e^-.s^{-1}}.\mu\mathrm{m^{-1}}$), as shown in Fig. 9. This last result could have been expected from the timing diagram (Fig. 2). Indeed the dark current is by definition the evolution of the output voltage with integration time. Since the FD is reset just before the transfer, only the charge generated in the FD during the inter sample time can contribute to the measured voltage. As this inter-sample does not change with integration time, the FD contribution and cannot be seen (it is suppressed when the slope of the dark signal with the integration time is extracted). Moreover, since the inter-sample time is small (a few μs), the FD contribution to the output dark voltage should not be significant. The conclusion would be different in a snapshot PPD pixel in which the sampled signal is stored on a floating diffusion for a significant amount of time before being read. In this case, the dimension of the floating diffusion used to store the signal would have a large impact on the resulting dark signal.

As regards the TG contribution J_{TG}, it can clearly be seen in Fig. 10 that it is very dependent of $\mathrm{V_{LOTG}}$, as expected [11], [13], [14]. At $\mathrm{V_{LOTG}} = 0$, this contribution is very large

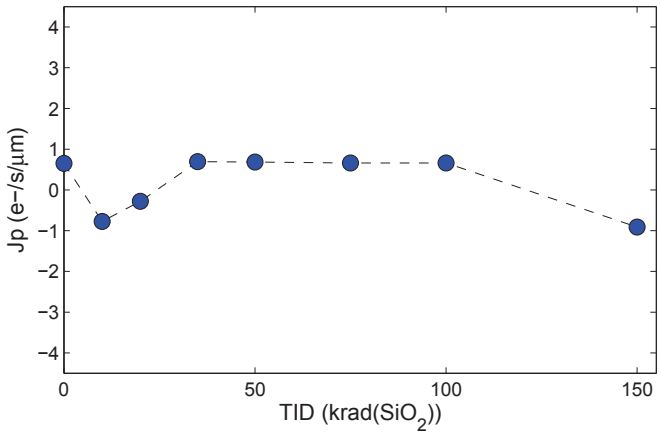

Fig. 12. Perimeter dark current linear density J_p as a function of total ionizing dose.

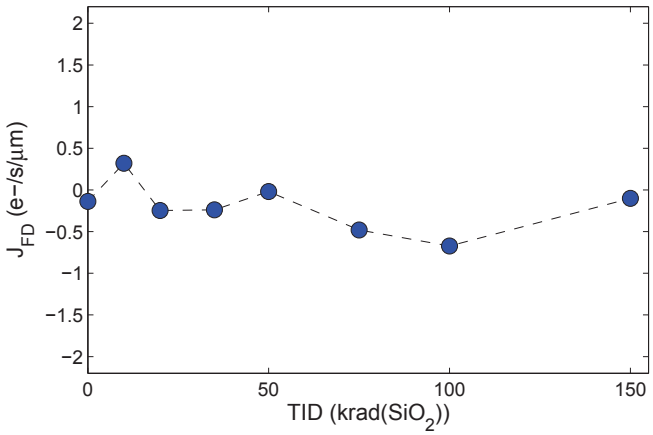

Fig. 14. Floating diffusion dark current linear density J_{FD} as a function of total ionizing dose.

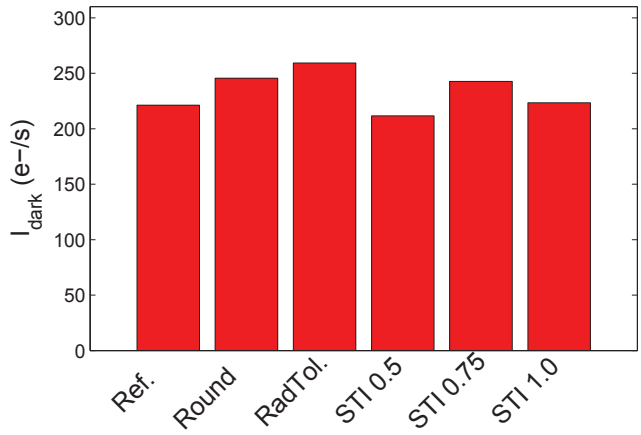

Fig. 13. Dark current of the alternative photodiode layouts after 75 krad(SiO_2) with $V_{\mathrm{LOTG}} = -0.6$ V. The differences between structures are small enough to be attributed to device mismatches and measurement errors.

($J_{\mathrm{TG}} \approx 30$ e$^-$.s^{-1}.μm^{-1}) whereas it tends to zero when the TG approaches the accumulation regime.

We have seen that when the TG is accumulated, the only contribution dependent of the photodiode dimension is J_a. Thus the I_0 contribution is simply determined by extracting the y-axis intercept (for an area $= 0$ μm^2) in Fig. 7. It can be seen that I_0 is negligible before irradiation.

B. Evolution with irradiation

Fig. 11 presents the evolution of dark current with TID of the reference pixel (Perim3) with two V_{LOTG} biasing conditions: depleted ($V_{\mathrm{LOTG}} = 0$ V) and accumulated ($V_{\mathrm{LOTG}} = -0.6$ V) during integration. The average dark current increases with TID in both cases (and a slight saturation effect can be observed at the highest TID level when the TG is depleted). However, about one order of magnitude of reduction is achieved when the TG is accumulated during integration. Further insight into this degradation is given by looking at each contribution separately. It should also be noticed that this figure shows how many IC have been used per TID level during this study. In the following, when more than one device was irradiated at a given TID level, the average dark current value is provided.

The perimeter contribution (in which the peripheral STI contribution is included) stays in the uncertainty of the slope extraction process even at 150 krad(SiO_2) (Fig. 12). Hence, in opposition to what is generally inferred, the peripheral STI does not seem to have any influence on the radiation induced dark current[4] (in this TID range). This conclusion is confirmed by the dark current measured on the structures with larger STI recess distance d_{STI}, as illustrated in Fig. 13. Indeed, it can be seen in the figure that there is no significant difference between the dark current measured after irradiation on the reference pixel (with $d_{\mathrm{STI}} = 0.3$ μm) and the dark currents measured on the pixels with a larger recess distance ($d_{\mathrm{STI}} = 0.5$, 0.75 and 1.0 μm). Similar conclusions can be drawn on the FD contribution to the overall dark current as can be seen in Fig. 14.

As regards the area contribution, Fig. 15 shows that J_a does not change significantly up to 75 krad(SiO_2). At 100 krad(SiO_2), a slight increase is observed. It is confirmed by a much larger rise at 150 krad(SiO_2). The only source of TID induced dark current that can be a function of the PPD area is the top oxide interface (silicide block oxide interface in Fig. 1). There are two possible mechanisms that can explain this observation: 1) The radiation induced trapped charge density becomes large enough to change the

[4]It agrees well with the results presented in [9] (which show no effect of the photodiode length, between 1 and 9 μm, on the radiation induced dark current) but seems to contradict the conclusion drawn on PPD with very small pixel pitches [19] (around 1 μm). Indeed, in this last study, the authors suggest that one of the radiation induced dark current source comes from the perimeter of the PPD. This discrepancy with the work presented here is attributed to two main factors: 1) The dark current is so low (well below 1 e$^-$/s at room temperature) in these small pitch state-of-the-art devices that it can reveal other dark current sources that are not visible here. 2) in small pitch (below 2 μm) PPD, the pixels are drawn by using the minimum sizes that bring good performance before irradiation. It means that, for example, the recess distance d_{STI} between the PPD and the STI is likely to be shorter than the 0.3 μm used in our work. This distance might be tuned to the optimum value that leads to the minimum dark current before irradiation. However, this minimum distance might be too small to mitigate the influence of the peripheral STI on the overall PPD dark current after irradiation in these small pitch pixels.

electrostatic potential distribution above the pinned photodiode (by reducing the effective doping concentration of the P+ pinning layer), leading to the extension of the PPD depletion to the top oxide interface (as explained in [20]). 2) The large amount of interface states generated in the top oxide/silicon interface by the ionizing radiation induce a large diffusion current contribution that becomes larger than the diffusion current contribution coming from the silicon neutral volume. This phenomenon is further discussed in [19] and can be illustrated by the following simplified analytical development. Let consider the continuity equation [21] in one dimension with an x axis from the top of the depletion region to the Si/SiO_2 interface above the PPD:

$$D_n \frac{\partial^2 n(x)}{\partial x^2} - \frac{n(x) - n_i^2/N_A}{\tau_n} = 0 \ , \tag{2}$$

with the following hypothesis:

- every electron (minority carrier) that reaches the depletion region is instantaneously collected by the electric field:

$$n(0) = 0 \ , \tag{3}$$

- the current density at the Si/SiO_2 interface is determined by the recombination velocity s_0 [21]:

$$qD_n \left.\frac{\partial n}{\partial x}\right|_{x=x_{\mathrm{SiO2}}} = -qs_0 \left[n(x_{\mathrm{SiO2}}) - n_i^2/N_A\right] \ , \tag{4}$$

with $s_0 = \sigma_n v_{\mathrm{th}} N_{\mathrm{it}}$.

The x axis represents a vertical axis in Fig. 1, placed in the middle of the PPD, from the substrate to the PMD oxide with $x = 0$ being the depletion region top boundary and x_{SiO2} the interface location on the x axis. Solving this equation with these conditions leads to the following expression of the electron current density at the top boundary of the PPD depletion region (i.e. for $x = 0$):

$$J_n(0) = \frac{qn_i^2}{N_A} \times \frac{\frac{D_n}{L_n}\sinh\left(\frac{x_{\mathrm{SiO2}}}{L_n}\right) + s_0 \cosh\left(\frac{x_{\mathrm{SiO2}}}{L_n}\right)}{\cosh\left(\frac{x_{\mathrm{SiO2}}}{L_n}\right) + s_0 \frac{L_n}{D_n}\sinh\left(\frac{x_{\mathrm{SiO2}}}{L_n}\right)} \ , \tag{5}$$

whit $L_n = \sqrt{D_n \tau_n}$. Further simplifications can be achieved by considering two additional realistic assumptions (as proposed in [19]): 1) the distance between the interface and the PPD depletion region is much smaller than the diffusion length (i.e. $x_{\mathrm{SiO2}} \ll L_n$) and 2) the generation process at the interface is more intense than the recombination process in the P+ pinning layer (i.e. $s_0 \gg x_{\mathrm{SiO2}}/\tau_n$):

$$J_n(0) = \frac{qn_i^2 \sigma_n v_{\mathrm{th}}}{N_A} \times \frac{N_{\mathrm{it}}}{1 + \frac{x_{\mathrm{SiO2}} \sigma_n v_{\mathrm{th}}}{D_n} N_{\mathrm{it}}} \ . \tag{6}$$

This simplified development shows that if the interface state density N_{it} at the Si/SiO_2 interface above the PPD increases, the minority carrier (electron) diffusion current density from the top interface increases also until reaching a saturation level when the interface state density becomes very high[5]. If this top interface contribution becomes large enough to dominate the overall dark current, the dark current would be proportional to the PPD area as observed here. It should be emphasized that both proposed mechanisms (depletion of the Si/SiO_2 interface and increase of the diffusion current from this interface) cannot occur simultaneously since once the interface is depleted, there is no more diffusion current (it becomes a pure generation current in a depleted region).

[5]i.e. when $N_{\mathrm{it}} \gg D_n/(\sigma_n v_{\mathrm{th}} x_{\mathrm{SiO2}})$

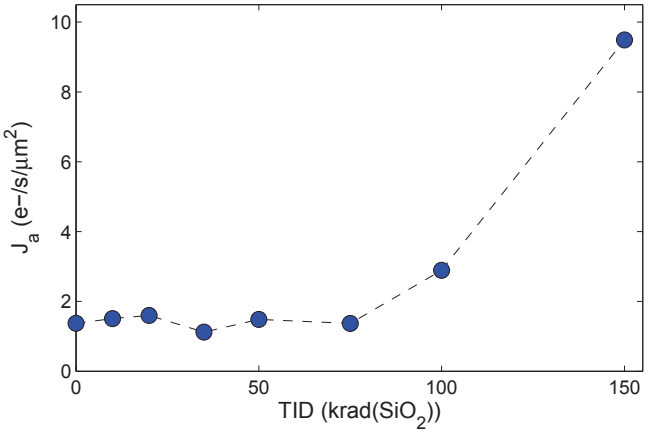

Fig. 15. Dark current area density J_a as a function of total ionizing dose.

If the TG is biased into accumulation, it can be seen in Fig. 16 that the ionizing radiation does not increase the J_{TG} contribution whereas a huge rise can be seen in the case where $\mathrm{V_{LOTG}} = 0$ V. This large increase is most likely due to the interface states generated in the depleted region of the transfer gate (interfaces with the gate oxide and/or the STI sidewalls).

The most surprising result is presented in Fig. 17. This figure shows that the contribution I_0, independent of the design variations, increases much with TID in both $\mathrm{V_{LOTG}}$ bias conditions. However, this radiation induced parasitic current can be reduced by about a factor of ten when the TG is biased in accumulation during integration. This last result demonstrates that this contribution is directly influenced by the TG voltage. The possible origin of I_0 is discussed in sec. V-A. It is also interesting to notice the decrease of dark current at 150 krad(SiO_2). This effect seems correlated with the increase in area contribution J_a and could also possibly be linked to the change of electrostatic potential distribution (due to a degradation of the P+ pinning layer).

Now that each dark current source has been de-correlated, it is interesting to look at their contribution relative to each other. This is what is presented in Fig. 18 and Fig. 19. In these bar charts, each color represents a dark current source and the total bar height is equal to the total dark current measured. The dark current source contributions have been evaluated by using (1), the previously determined values and the area and perimeter of the reference pixel (Perim3) given in Tab. I.

When the TG is biased to 0 V during integration, it can clearly be seen that before irradiation, the two main contributors are the transfer gate linear current density J_{TG} and the dark current area density J_a. After the first irradiation step, I_0 becomes the main source of dark current. The dark current attributed to the TG width also rises significantly and contributes between 15 and 40% of the total radiation induced dark current. The area dark current remains negligible

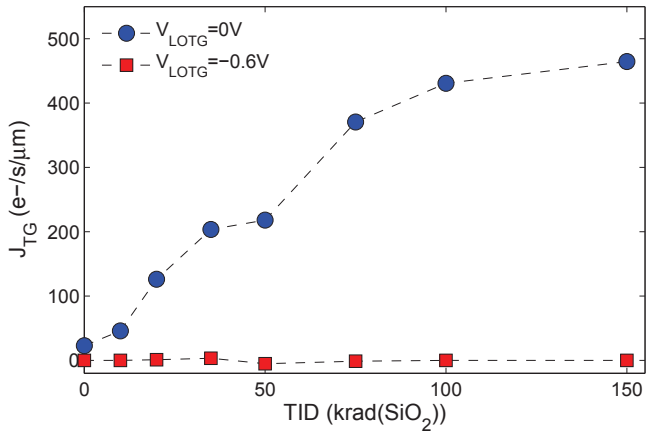

Fig. 16. Transfer gate dark current linear density J_{TG} as a function of total ionizing dose.

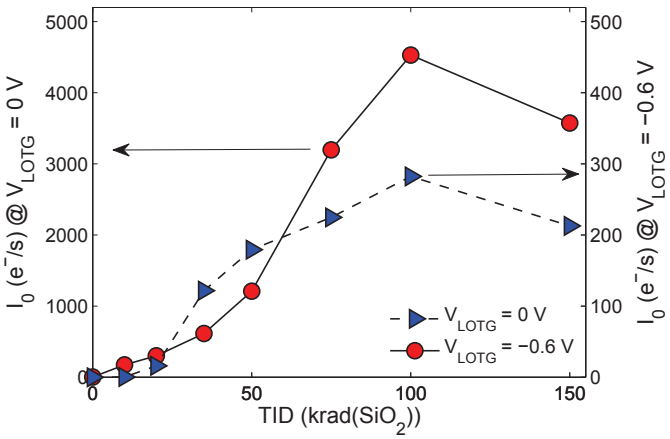

Fig. 17. Dark current offset I_0 as a function of total ionizing dose.

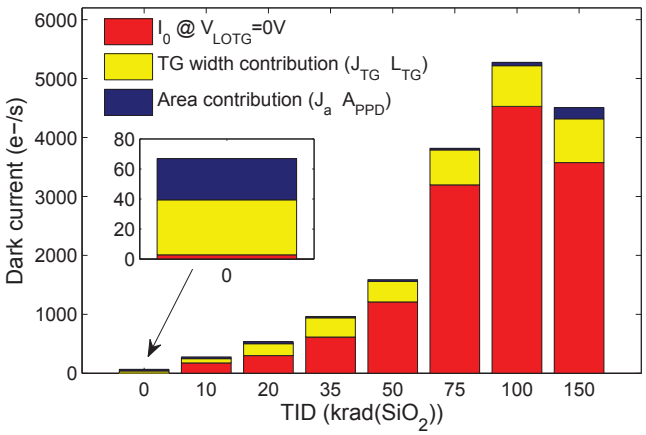

Fig. 18. Reference pixel (Perim3) dark current for $V_{\mathrm{LOTG}} = 0$ V showing the contribution of each dark current source to the total current.

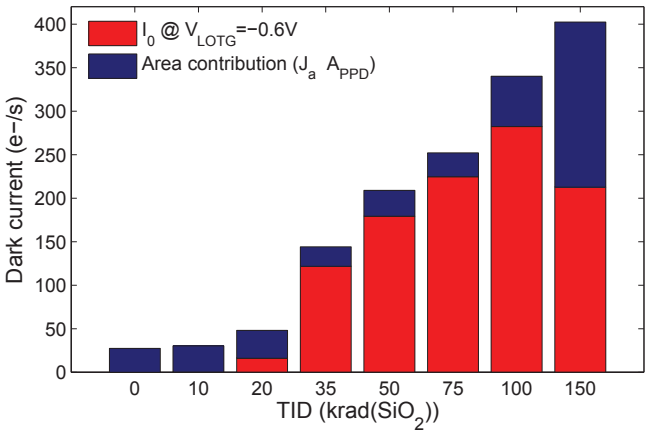

Fig. 19. Reference pixel (Perim3) dark current for $V_{\mathrm{LOTG}} = -0.6$ V showing the contribution of each dark current source to the total current.

in this biasing condition, despite a noticeable increase at 150 krad(SiO_2).

When the TG is biased into accumulation during integration, the dark current from the TG width disappears and the current from the area dominates up to 20 krad(SiO_2). As already mentioned, this last contribution stays constant up to 100 krad(SiO_2). The I_0 source begins to appear in this regime at 20 krad(SiO_2) and dominates the total current from 35 krad(SiO_2) to 150 krad(SiO_2). It should be emphasized that at this last TID level, the area contribution represents about 40% of the total current whereas it was below 15% at the previous step. It suggests a strengthening of the area contribution over the I_0 source at higher TID levels.

V. Discussion

A. Possible origins of I_0 and consequences on RHBD

The main contribution, I_0, to the TID induced dark current rise is a current source which is not dependent of the design variations studied in this work. By looking at Fig. 3, one can see that the two parts of the photodiode layout that are common to all the pixels listed in Tab. I are: 1) the corner of the PPD and 2) the lateral edges (perpendicular to the PPD area) of the TG. The PPD corners cannot be the source of I_0 because I_0 is strongly dependent of V_{LOTG} whereas the corners of the PPD area are too far from the TG to be influenced by its voltage. This is confirmed by the measurements performed on the Round diode, which are presented in Fig. 13. Indeed, removing the corners by drawing a completely round PPD does not change the total current, which is dominated by I_0 at this TID (see Fig. 19).

As regards the TG lateral edges, one can see in Fig. 3 that it can be divided into two regions. The first is the part of the TG that is located over the active area (i.e. with no STI). The second is the part of the TG that is placed over the STI, to allow the formation of the contact via. Once again, Fig. 13 allows us to go a little further. The measurements performed on the RadTol structures show no significant improvement on the TID induced dark current generation[6]. By comparing Fig. 3 and Fig. 4, it can be noticed that the TG edge located over the PPD region changes much between the two layouts: this part of the TG is longer in the case of the RadTol design and there are also more TG corners than in the standard design of Fig. 3. On the other hand, the part of the TG that overlaps the STI is pretty similar in both cases. These results suggest that

[6]This could be due to a slight difference between the layout used in [6] and the one used here.

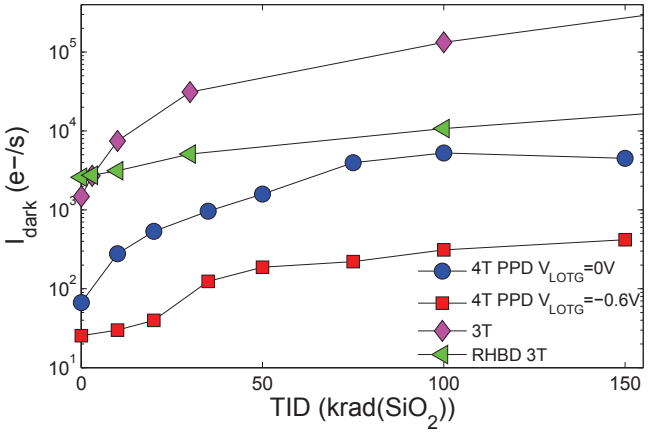

Fig. 20. Dark current evolution with TID: comparison between a conventional 3T pixel, a Radiation-Hardened-By-Design (RHBD) 3T pixel (surround P+ [22]) and the reference 4T PPD pixel (Perim3). The equivalent pixel pitch is about 6 μm. The 3T pixel results, measured on 2×5 μm^2 photodiodes [22], are normalized to the reference pixel pinned photodiode size (4.5×4.5 μm^2) assuming a direct proportionality of 3T pixel dark current with photodiode perimeter (as demonstrated in [23]).

the source of I_0 could be due to the design of the TG in the transition region where the TG approaches the STI.

Based on these results, it is inferred that the main source of dark current comes from the TG region, near the STI. If this hypothesis is validated, changing the design of the TG in this specific region should have a strong impact on the I_0 source and mitigation techniques could probably be found. As regards the radiation induced area contribution that arises above 100 krad(SiO$_2$), there is apparently no way of mitigating it by design (except by reducing the area). If the increase of the area contribution is confirmed at higher TID levels (especially on other devices and technologies), it could be a serious limitation for the use of 4T PPD in high TID applications.

B. Comparison between 4T-PPD-CIS and 3T-CIS

Radiation hardness of CIS is pretty difficult to compare from one work to another. Among the numerous reasons for that, one can cite: the different dimensions, the different processes and technology nodes used (and the associated differences in pre-irradiation dark current values), the different designs, the differences in measurement conditions and measurement units with most often no way of extrapolating correctly the results (due to the absence of photodiode layout dimension). Moreover, since, to our knowledge, the influences of all the dimensions of the PPD on the radiation induced dark current were never de-correlated before, it was difficult to extrapolate the results achieved on one PPD layout to the values measured on another imager. What is very often done is to express the dark current in an area current density unit (e.g. nA/cm^2), usually referred to the pixel pitch (instead of the PPD area), and then it is extrapolated to another pixel pitch by assuming direct proportionality to the pixel pitch. This work demonstrates that such technique would lead to wrong interpretations on 4T-PPD-CIS.

Fortunately, the devices studied in this work have been manufactured with the same process as the work performed on 3T-CIS presented in [22]. Moreover, it is well-known [24], and it is regularly confirmed (e.g. as shown in [23]), that radiation induced dark current in 3T-CIS mainly comes from the photodiode perimeter. Therefore, the results presented in [22] can directly be compared to the measurement performed on the studied 4T-PPD pixels only by multiplying the 3T-CIS results by the perimeter ratio of the 4T-PPD-CIS and 3T-CIS. Such comparison is shown in Fig. 20. It can clearly be seen that, as expected from the lower pre-irradiation dark current values of 4T-PPD-CIS compared to 3T-CIS, the TID induced dark current increase of pinned photodiodes is more than one order of magnitude below the standard 3T design. It can even be more than two orders of magnitude lower when the TG is accumulated during integration. It is interesting to notice that both 3T-CIS and 4T-PPD-CIS dark current trends with TID appear pretty similar (despite the difference of order of magnitude). Moreover, the relative increase (i.e. the dark current increase divided by the dark current level before irradiation) is almost the same between the two sensor technologies. It should also be emphasized that the gap between the two technologies is significantly reduced when a 3T radiation hardened design is used and more work is needed to determine if 4T-PPD-CIS will still exhibit the best behavior at a higher TID level. Furthermore, dark current increase is the main reported degradation but more studies are necessary to determine whether the other 4T-PPD-CIS characteristics are degraded by ionizing radiation.

C. Comments on the biasing conditions during irradiation

It is well known [25] that the worst case degradations of MOSFETs are achieved when these transistors are biased during irradiation (and so when the electric field in the MOS oxide is maximum). In the case of a PPD, biasing the photodiode during irradiation should not have a strong influence on the TID induced dark current increase since the electric field lines originating from the PPD do not penetrate the surrounding oxides. Indeed, the surrounding P layers are biased to 0V. Therefore, this work conclusions related to the PPD (about area and perimeter contributions) should not change with biasing conditions during irradiation. However, MOSFET may be degraded more rapidly if the sensor is biased during irradiation. As shown previously on a similar technology [23], transistors from the FD to the sensor output do not contribute to the dark current (which is the only parameter of interest in this study). The sole transistor that plays a role in the TID induced dark current increase is the TG MOSFET. Its contribution could be enhanced by biasing the sensor during irradiation. Nevertheless, the physical mechanism should not change and this study conclusion should remain valid in biased devices, even for the TG contributions (i.e. the influence of V_{LOTG} on dark current, and the discussion about I_0). Validating these hypotheses will be the subject of future work.

VI. Summary

The localization of dark current sources before and after exposure to ionizing radiation has been investigated in Pinned

Photodiode CMOS Image Sensors. The contributions of the area, the perimeter, the transfer gate width and the floating diffusion length to the TID induced dark current have been decorrelated for the first time in PPD-CIS. It has been shown that up to 150 krad(SiO_2), the PPD perimeter and the FD perimeter do not contribute to the overall dark current. The TG width does not contribute to the radiation induced dark current either if the TG is biased in accumulation (i.e. $V_{\mathrm{LOTG}} < 0$ during integration). The remaining radiation induced dark current sources are: a contribution from the area of the PPD, most likely coming from the top oxide radiation induced defects and a contribution independent of the tested pixel design variations but strongly dependent of TG bias. The results presented here suggest that the latter dark current source is related to the region of the TG that is located near the STI, for allowing the contact via formation. Changing the design of the TG in this area is thus expected to change the radiation hardness of the devices. This identification of degradation sources in PPD CIS will help improve our understanding of irradiated PPD behaviors and will help find efficient radiation-hardening-by-design solutions.

This study has also demonstrated that applying a negative voltage on the TG during integration strongly reduces the radiation induced dark current. Therefore, such biasing condition should always be used for improved radiation hardness of PPD-CIS (at least from the dark current point of view).

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