Identifying dielectric and resistive electrode losses in high-density capacitors at radio frequencies

M.P.J. Tiggelman, K. Reimann*, J. Liu*, M. Klee**, W. Keur**, R. Mauczock**, J. Schmitz, and R.J.E. Hueting

University of Twente, MESA+ Institute for Nanotechnology
Department of Semiconductor Components, 7500 AE Enschede, The Netherlands
Telephone: +31 (0)53-4892644, Fax: +31 (0)53-4891034
Email: m.p.j.tiggelman@ewi.utwente.nl

*NXP Semiconductors, 5656 AE, Eindhoven, The Netherlands

**Philips Research, 5656 AE, Eindhoven, The Netherlands

***Abstract*— A regression-based technique is presented which distinguishes the dielectric loss from the resistive loss of high density planar capacitors in a very wide bandwidth of 0.1–8 GHz. Moreover, the procedure yields useful results if the capacitor deviates from a lumped element model and indicates when the used approximations break down or whether size-dependent loss mechanisms exist.**

I. INTRODUCTION

Reconfigurable passive building blocks can reduce system area and costs in handheld applications. Tunable technologies based on micro-electro-mechanical-systems (MEMS) [1], [2], varactor diodes [3], liquid crystals [4] or ferroelectrics [5] support the continuous miniaturization of microwave electronics. We optimize ferroelectric capacitors on silicon as a potential key component for microwave frequency agile applications. The requirements of a low loss tangent $\tan\delta$ (high unloaded quality factor Q) and a high tunability are evident for tunable capacitors at radio frequencies (RF) especially in passive circuits where no active circuitry is present that compensates for dissipation. Fast processing and characterization cycles are desired for the material development of complex ferroelectrics for high density planar capacitors.

We present an easy-to-implement, but still accurate enough, electrical material characterization technique, which distinguishes the dielectric loss from the resistive electrode loss of simple metal-insulator-metal (MIM) test devices. Our technique even provides for a partial compensation of distributed effects and indicates graphically when the used approximations break down or whether size-dependent loss mechanisms exist. In this paper we make use of the geometry, sheet resistance, measured series equivalent capacitance and frequency behavior of more than 2 circular shaped test structures to separate the aforementioned losses at a given frequency. The resistive electrodes, and the inductance overcompensation during a 1-port short-open-load (SOL) calibration have an effect on the measured equivalent capacitance and loss tangent. The loss separation technique is fully exploited in the latter section. It enables the process engineer to gain a swift and better understanding in how to optimize the process flow to improve RF performance.

II. TEST STRUCTURES

We employ circular shaped ground-signal-ground (GSG) capacitor test structures of which only the top electrode is patterned [6] (see Fig. 1).

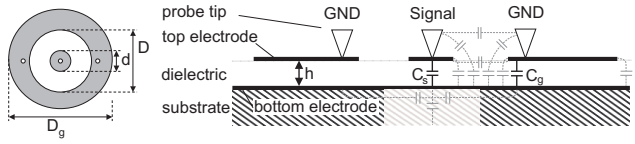

Fig. 1. A top view with 3 probe landing spots and a cross section of the test device. The bottom electrode and the dielectric layer are not patterned. The parasitic capacitances are indicated with striped grey colors.

The top electrodes consist of a Pt-Au stack and the bottom electrode of Pt. The sheet resistance of the top electrodes is $R_{\mathrm{s,t}} \approx 70\,\mathrm{m\Omega/\square}$ and the sheet resistance of the bottom electrode is $R_{\mathrm{s,b}} \approx 1.4\,\Omega/\square$. A ferroelectric insulator of barium strontium titanate (BST), with a relative permittivity $\varepsilon_{\mathrm{r}} = 170$ and a thickness $h = 110\,\mathrm{nm}$, is sandwiched between the parallel electrodes. The diameter d of the signal path varies from $8\,\mu$m to $88\,\mu$m. The bottom electrode and dielectric layer are both homogeneous and unpatterned. The capacitance of the signal (center) path C_{s} is in series with the much larger ground capacitor C_{g} with an outer ring diameter of $D_{\mathrm{g}} = 600\,\mu$m and an opening of $D = 100\,\mu$m. The measured equivalent series capacitance is therefore approximated by C_{s}.

The parasitic capacitances through the air, the dielectric and silicon are also indicated in Fig. 1. An assessment is made on the capacitance contributions to the test structures. Starting with the capacitance from the signal path to the bottom electrode

$$C_{\text{par,signal path}} = \epsilon_0 \varepsilon_{\mathrm{r}} (\pi d) \left(\frac{2\ln(2)}{\pi} - \text{underetch} \right) \qquad (1)$$

we use conformal mapping [7], [8] to get an estimation of the parasitic capacitance, which is lower than 2.1% of C_{s}, assuming the underetch equals zero. The capacitance from the ground top electrode to the bottom electrode is negligible, because of the very large ground capacitance. The capacitance

from the signal path to the ground path through the dielectric is also neglected. The distance between the contact paths is in the μm-range, while the dielectric thickness is in the nm-range, so the electric field is screened by the bottom electrode.

The capacitance between the ground and signal probes and paths is simulated in the planar full-wave electromagnetic program Sonnet [11](more details about the simulations are given in section IV-B). The permittivity of air is set to 1×10^{-4}, then to 1 and the measured equivalent series capacitance is compared. The simulation results show that the additional capacitance is in the low fF-range and is hence negligible. The capacitance from the middle of the bottom electrode downwards into the 675 μm substrate has a very small ratio of the area to the dielectric thickness and is estimated in the fF-range. The capacitance parallel to the bottom electrode through the silicon substrate is determined by performing Sonnet simulations without a bottom electrode. We obtained less than 20 fF for a capacitor with an inner diameter of 40 μm. Since the influence of all parasitic capacitances compared to our high density capacitors differ individually a factor 100 or more we can neglect all these parasites.

III. MODELING

The electrode resistance is modeled to be able to separate the measured dielectric loss from the measured resistive loss. We model the ferroelectric capacitor with an R_s–C_s series equivalent model (see Fig. 2).

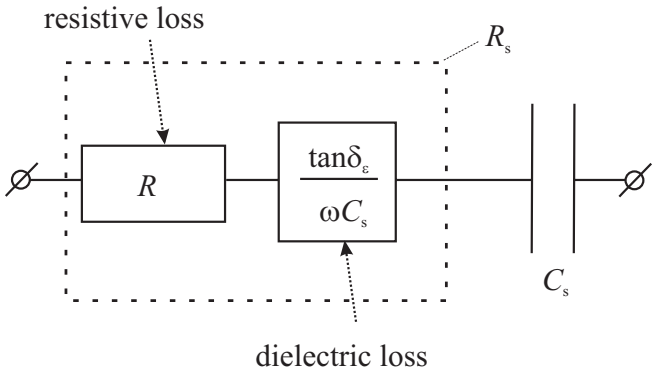

Fig. 2. The measured series R_s–C_s equivalent capacitor model.

with the equivalent series resistance R_s=$\Re(Z_{11})$, the modeled electrode resistance R, the dielectric loss $\tan\delta_\varepsilon$ [9]., and the equivalent series capacitance C_s.

The measured loss tangent then follows

$$\tan\delta = \frac{1}{Q} = \frac{\Re(Z_{11})}{|\Im(Z_{11})|} = \tan\delta_\varepsilon + \omega C_s R \qquad (2)$$

The latter term represents the additional resistive electrode loss at RF. The geometry of the electrodes determines the resistance R [6], [10]. For a lumped element case R is approximated by the sum of the resistance of the center (signal) path (see Fig. 1 and 3)

$$R_{\text{center}} = \frac{R_{s,t} + R_{s,b}}{8\pi} \qquad (3)$$

and the resistance of the bottom electrode between the signal and ground path

$$R_{\text{ring}} = \frac{R_{s,b}}{2\pi} \ln\left(\frac{D}{d}\right) \qquad (4)$$

and the resistance R_{outer} of the connection to the ground probes. A schematic circuit is depicted in Fig. 3.

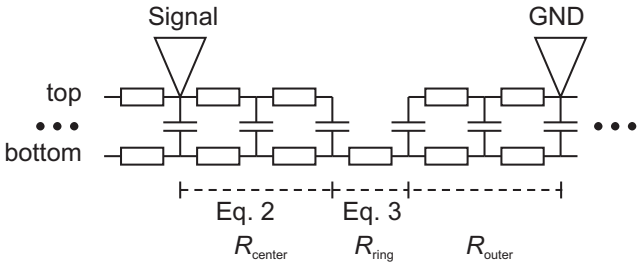

Fig. 3. Any lumped capacitor becomes a distributed R-C chain at RF. The capacitances corresponding to the electrical fields through air and substrate (not drawn) are still negligible small with respect to the large capacitances of the MIM capacitor.

R_{outer} can be neglected in our case because of the larger diameter $D \gg d$. The contact resistance of the electrodes at the probe tip is measured on an unpatterned top electrode with $R_{\text{short,top}} \approx 0.1\,\Omega$ and is hence negligible. We therefore write the resistance

$$R \approx g_R R_{s,b} \quad \text{with} \quad g_R = \frac{1}{2\pi}\left(\frac{1+\eta}{4} + \ln\frac{D}{d}\right) \qquad (5)$$

$$\text{and} \quad \eta = \frac{R_{s,t}}{R_{s,b}}$$

as a product of the sheet resistance $R_{s,b}$ of the bottom electrode and an electrode geometry factor g_R. The sheet resistance ratio η is negligibly small for the typical choice of well conducting top electrodes.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

1-Port S-parameter were measured with an Advantest R3767CG vector network analyzer (VNA) in the frequency range of 300 kHz–8 GHz, and an Infinity GSG probe (probe pitch = 125 μm). All measurements were performed at zero bias with an RF power of $P_{\text{RF}} = -10$ dBm at room temperature using the built-in short-open-load calibration on a CS-5 calibration substrate of GGB Industries. A small error is made in the inductance measurements because of a zero short inductance parameter in the calibration kit. A port offset could be used to account for the finite probe inductance, but was avoided for the sake of simplicity. The data analysis used here is insensitive to the inductance calibration error (see

below).

A. Capacitance with frequency

The measured ferroelectric capacitance decreases with frequency due to dielectric relaxation and distributed effects. Relaxation effects cause a delay in ionic polarization decreasing the relative dielectric constant linearly on a logarithmic frequency scale. The decrease is independent of the diameter and is relatively small compared to the much stronger decrease due to distributed effects from a few hundred megahertz onwards (see Fig. 4).

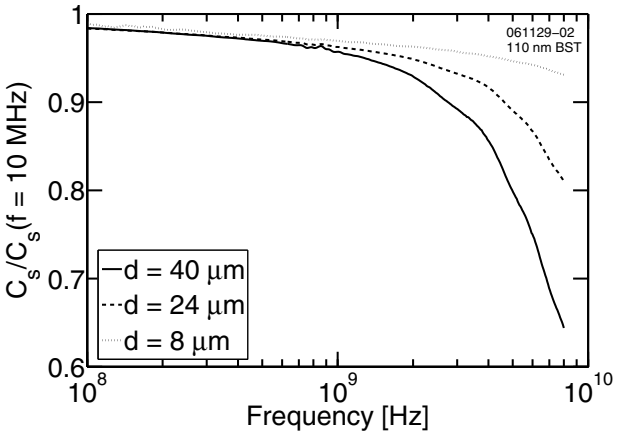

Fig. 4. The normalized capacitance declines above $f = 400\,\mathrm{MHz}$ for the largest capacitor due to the distributed nature of the capacitor.

A lumped capacitor becomes distributed with increasing frequency due to the resistivity of the electrodes (see also Fig. 3). At RF the R–C chain leads to a voltage drop at the edges of the capacitor, which acts as if the area of C_s would be reduced. A reduced R_center is accompanied by a reduced C_s (deviation from the linear decline in capacitance in Fig. 4). To confirm this assumption simulations were setup in the planar 3D full-wave electromagnetic simulation program Sonnet [11]. All possible coupling mechanisms are included in the electromagnetic analysis.

B. Capacitor modeling

A simulation in Sonnet starts with defining the mesh and the dimensions of a box. A box consists of 6 grounded and lossless boxwalls in which a test structure is designed. Our complete capacitor stack is visualized in Fig. 5.

The planar dielectric and metal layers are surrounded by grounded boxed walls. The capacitor electrodes are isolated from the grounded sidewalls, similar to the measurements. The ground-signal-ground (GSG) probe pins are simulated in a relatively simple way by three $4\,\mu\mathrm{m} \times 4\,\mu\mathrm{m}$ lossless vias from the top boxwall to the top electrode of the signal and ground path as depicted in Fig. 5 and 6.

The signal via port is placed at the center of the via and both separate ground vias are connected to the top box wall. Our planar circular capacitive test structures are approximated by a regular octagon.

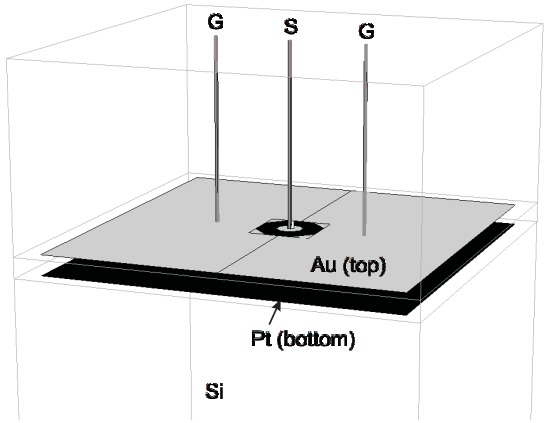

Fig. 5. A 3D image of the planar layers of a MIM capacitor test structure with vias as GSG probe tips inside a Sonnet design box.

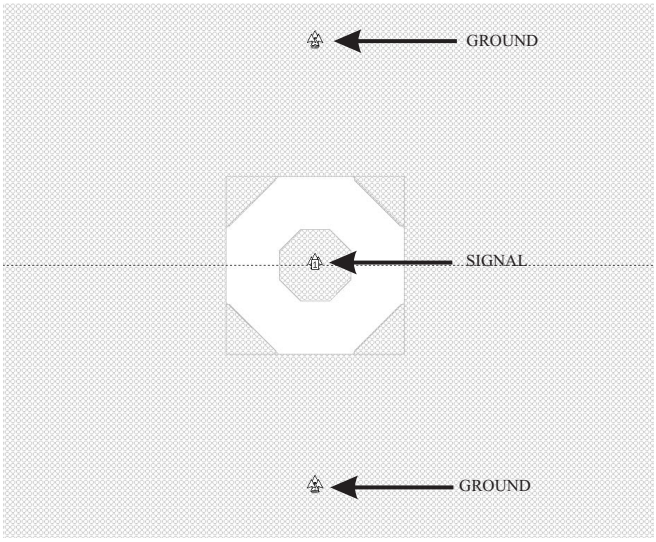

Fig. 6. A zoomed-in top view of a capacitor in Sonnet with an inner signal path diameter of 40 μm, three vias act as probe pins of a GSG probe and a 50 Ω signal port is situated in the center of the DUT.

The MIM capacitors are modeled by 3 planar dielectric layers with material parameter values as given in TABLE I with the relative permittivity ε_r, the relative magnetic permeability μ_r and the dielectric conductivity σ. These values are constant and were chosen to match the measured values at 200 MHz.

Layers	Thickness	ε_r	μ_r	$\tan\delta$	σ
air	1 μm	$1{\cdot}10^{-4}$	$1{\cdot}10^{-4}$	0 %	0 S/m
BST	0.11 μm	170	1	1 %	0 S/m
Si	675 μm	11.9	1	0.04 %	5 S/m

TABLE I
LAYER PROPERTIES OF THE DIELECTRIC LAYERS IN SONNET.

The non-physical parameter values of the air layer

minimize the parasitic capacitance and inductance caused by the lossless vias. We therefore do not need to simulate separate calibration or de-embedding structures at the cost of neglecting a part of the device capacitance and inductance. The resistive electrode layers are defined by the measured sheet resistance as mentioned in section II.

1) Modeling distributed effects: The capacitor stack is simulated with lossless and lossy electrodes. The 1-port response of the simulated C_s and $\tan\delta$ at different frequency points are depicted in Fig. 7.

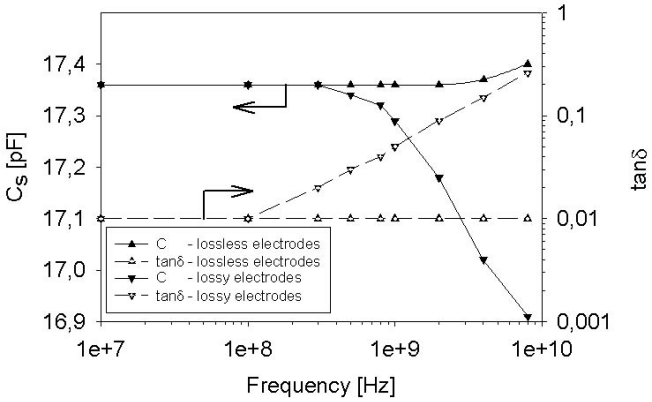

Fig. 7. Planar electromagnetic simulations in Sonnet [11] show the capacitance of a test structure with an inner diameter of 40 μm with lossless and lossy electrodes. No relaxation effects are included in the simulations.

The strong frequency dependent influence of the resistive electrodes on the C_s and $\tan\delta$ is confirmed. The amount of electrode resistance of a high density capacitor determines the extent of the distributed effects, and therefore the resistive electrode loss. This result points out the importance of good conducting electrodes to obtain a low loss tangent at RF.
Furthermore, measurement uncertainty also affects the measured capacitance as described in [10], [12]. The short and load calibration standards are not ideal standards. They also contain parasitic inductances, which add up to the impedance of the standards. This causes inaccuracies in the measurement data if the user-defined calibration kit within the VNA is not adjusted properly, or if no correction factor is taken along in the parameter extraction program. In our case no quantified correction terms by the calibration kit manufacturer are known since our probe dissents from the advised one. An additional inductance caused by an incomplete impedance compensation of the short and load standard affects the measured capacitance with frequency. A manual correction by including an inductance L to the impedance parameters changes the reactive part of the impedance and therefore the capacitance as depicted in Fig. 8.

In our case the VNA assumes zero inductance for the combination of the GSG probe and the short or load measurement where is fact it should be around 10 pH. Adding the missing inductance to the measured impedance of

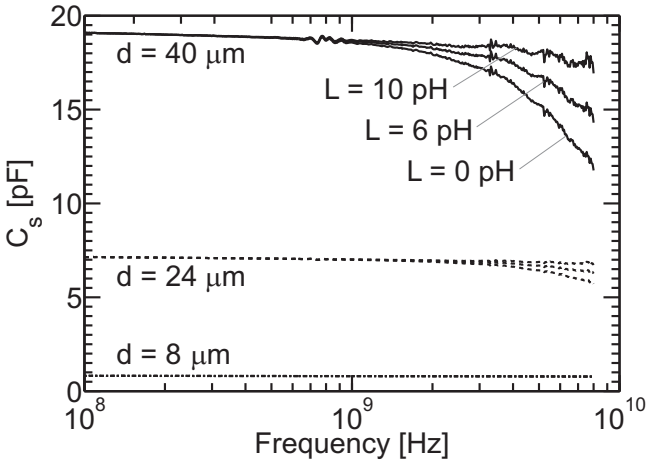

Fig. 8. The effect of an additional inductance of L = 0, 6 and 10 pH on the measured equivalent capacitance with frequency for devices under test (DUT)s with an inner diameter of d = 40, 24, and 8 μm.

$$Z_{11} = R - \frac{i}{\omega C_{\mathrm{s,L=0}}} + i\omega L, \quad \text{with } C_\mathrm{s} = \frac{-1}{\omega \Im(Z_{11})} \tag{6}$$

To distinguish the dielectric from the resistive loss a separation technique is proposed in the following section with partial compensation of distributed effects and inductance miss calibration.

C. The loss separation technique

The loss separation technique uses at least three circular shaped test structures with different inner diameters. No additional de-embedding structures are required. Distributed effects are partially compensated by plotting $\tan\delta$ as a function of the *measured* equivalent series capacitance (see Fig. 9). The slope of the curves is equal to $\omega R_\mathrm{s,b}$, as expressed in (2) and (5). The dielectric loss tangent $\tan\delta_\varepsilon$ is determined by a linear extrapolation to the intercept point at $\tan\delta(C_\mathrm{s}g_\mathrm{R})$ in Fig. 9 at f = 8 GHz. A deviation from linearity at small radii would suggest an influence of the edges of the capacitors, e.g., by damage during processing caused by reactive ion etching, increasing the loss tangent. A deviation from linearity at large radii suggests strong distributed effects, which decrease the capacitance and increase the loss tangent.

Employing the same visualization of parameters in Sonnet, the distributed effects for physically large capacitors becomes clearly visible as depicted in Fig. 10.

In Fig. 11 the measured $\tan\delta_\varepsilon$ and the resistive loss are separated across the entire frequency span. The (total) loss tangent of test structures with an inner diameter of 40, 24 and 8 μm is shown. A smaller inner diameter decreases the $\tan\delta$ at RF. To calculate the $\tan\delta_\varepsilon$ the measured total loss is extrapolated to $C_\mathrm{s}g_\mathrm{R} \to 0$ for each frequency using all data from d = 40 to 8 μm and d = 24 to 8 μm.

A graphical outline of the measurement data of more then two capacitors in Fig. 11 can safely and easily separate the

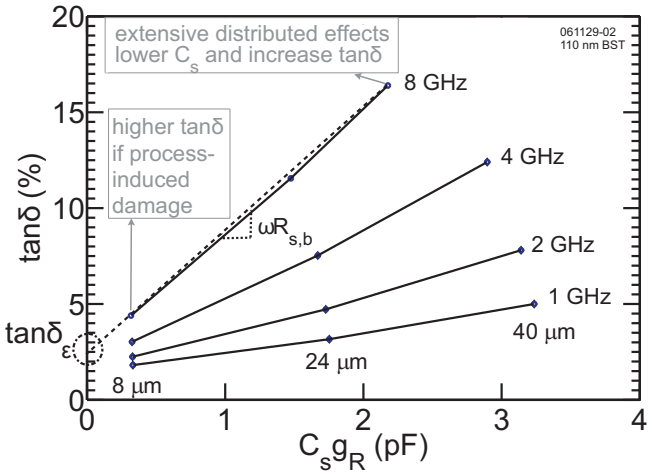

Fig. 9. The measured dielectric and the resistive loss tangent are separated using a linear regression. No inductance compensation is employed after calibration. The Sonnet simulation results at $f = 1$ GHz are indicated by the X-markers and show a close resemblance to the measurement results if $d = 8$ and 24 μm as expected.

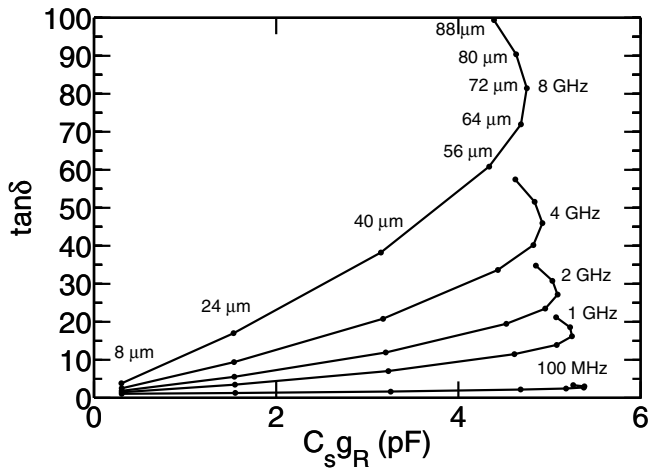

Fig. 10. This Sonnet simulation result shows the influences of distributed effects at multiple frequencies on capacitors with a relatively large inner diameter.

dielectric loss from the resistive electrode loss, as expressed in (2). It is especially suited to measure the frequency dependence of the dielectric loss tangent $\tan\delta_\varepsilon$. The results in Fig. 11 shows a typical ferroelectric behavior of increasing dielectric losses with increasing frequency.

Conclusions

An easy-to-use regression-based technique for characterizing planar high density capacitors is presented. This technique separates the dielectric losses from the resistive losses at $f = 0.1$–8 GHz utilizing three circular test structures. Furthermore, a deviation from the linear regression curve for small radii capacitors would suggest process-induced damage at the edges of the capacitor, and for large radii capacitors the influence of prominent distributed effects. A possible inductance

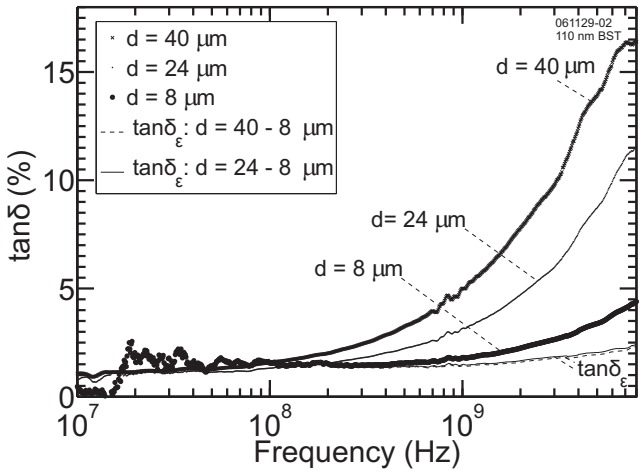

Fig. 11. The measured losses with and without subtraction of the resistive bottom electrode losses.

miss calibration is canceled to a large extent by the analysis technique. The effect of the electrodes on the losses at RF, and the validity of the approximations for the separation are demonstrated.

Acknowledgements

This work is partially supported by the European Commission, project NANOSTAR. M.P.J. Tiggelman would like to thank NXP Semiconductors for financing his research.

References

[1] S. Chang and S. Sivoththaman, *A Tunable RF MEMS Inductor on Silicon Incorporating an Amorphous Silicon Bimorph in a Low-Temperature Process*, IEEE Electron Device Letters, vol. 27, no. 11, pp. 905–907, November 2006.

[2] Th.G.S.M. Rijks, P.G. Steeneken, J.T.M. van Beek , M.J.E. Ulenaers, A. Jourdain, H.A.C. Tilmans, J. De Coster, and R. Puers, *Microelectromechanical Tunable Capacitors for Reconfigurable RF Architectures*, Journal of Micromechanical Microengineering, vol. 16, pp. 601–611, February 2006.

[3] K. Buisman, L.C.N. de Vreede, L.E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X.-d. Liu, and L.K. Nanver, *A Monolithic Low-Distortion Low-Loss Silicon-on-Glass Varactor-Tuned Filter with Optimized Biasing*, IEEE Microwave and Wireless Component Letters, vol. 17, no. 1, pp. 58–60, January 2007.

[4] J.A. Yeh, C.A. Chang, C.-C. Cheng, J.-Y. Huang, and S.S.H. Hsu, *Microwave Characteristics of Liquid-Crystal Tunable Capacitors*, IEEE Electron Device Letters, vol. 26, no. 7, pp. 451–453, July 2005.

[5] N. Setter et al., *Ferroelectric thin films: Review of Materials, Properties, and Applications*, Journal of Applied Physics, vol. 100, no. 051606, September 2006.

[6] Z. Ma, A.J. Becker, P. Polakos, H. Huggins, J. Pastalan, H. Wu, K. Watts, Y.H. Wong, and P. Mankiewich, *RF Measurement Technique for Characterizing Thin Dielectric Films*, IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 8, pp. 1811–1816, August 1998.

[7] S.B. Cohn, *Problems in Strip Transmission Lines*, IEEE Trans. on Microwave Theory and Techniques, vol. 3, Issue 2,pp. 119–126, March 1955.

[8] T.H. Lee, *Planar Microwave Engineering*, ISBN 0521835267, Cambridge University Press, pages 233-237, 2004.

[9] A.K. Tagantsev, V.O. Sherman, K.F. Astafiev, J. Venkatesh, and N. Setter, *Ferroelectric Materials for Microwave Tunable Applications*, Journ. of Electromagnetics, vol. 11, no.1–2, pp. 5–66, September 2003.

[10] P. Rundqvist, A. Vorobiev, S. Gevorgian, and K. Khamchane, *Non-Destructive Microwave Characterization of Ferroelectric Films on Conductive Substrates*, Integrated Ferroelectrics, vol. 60, no. 1, pp. 1–19, February 2004.
[11] (2007) The Sonnet website. [Online]. Available: http://www.sonnetsoftware.com/
[12] P.K. Petrov, N.McN. Alford, and S. Gevorgyan, *Techniques for Microwave Measurements of Ferroelectric Thin Films and Their Associated Error and Limitations*,Meas. Sci. Technol., vol. 16, pp. 583-589, January 2005.
[13] A. Davidson, K. Jones, and E. Strid, *LRM and LRRM Calibrations with Automatic Determination of Load Inductance*, 36th ARFTG Conf. Dig., pp. 57–62, November 1990.