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IGBT Package Design for High Power Aircraft Electronic Systems

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ABSTRACT

This paper will discuss the design of semiconductor packages having integrated air cooled heatsinks for use in high power electronic systems. It will demonstrate how simple models of the heat transfer from the heatsink fins, which are based on empirical correlations, may be utilised in combination with either simple analytical models or two dimensional finite difference (FD) models of the heat conduction from the semiconductor die through the multilayer package structure to the base of the fins. These models allow the rapid evaluation of performance under both steady state and transient overload conditions, and can be used to rapidly explore a wide range of design options before selecting candidate layouts for more detailed evaluation using, for example, 3D FD analysis.

Wind tunnel experiments, which will also be reported, have been carried out to verify the modelling results for different semiconductor device layouts. These trials demonstrate excellent agreement between the models and experimental results.

KEY WORDS: thermal design, heatsink, modelling

INTRODUCTION

Aircraft are increasingly using electronic systems to replace traditional mechanical, hydraulic and pneumatic systems in areas such as power conversion and actuation. For example, the Airbus Industrie proposed super Jumbo civil aircraft, codenamed A3XX, is likely to require a total nominal electrical supply of 600kVA compared to 360kVA for the current in-service A340 aircraft. In addition to the increased functionality and potential for weight saving that increased use of electrical/electronic systems offers, there are a number of other drivers for the adoption of electronic systems such as reliability and serviceability. Power electronic systems contain semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs), which switch high currents and

consequently have high power dissipations. Thermal management is therefore a key issue in the design of such systems.

Traditional high power electronic applications, such as in locomotive traction control systems, are based on industry standard semiconductor package configurations which are then bolted to heatsinks selected for the specific application. This bolted interface creates a significant resistance to heat-transfer and results in a large and heavy installation. An application specific package with an integrated heatsink has the potential to offer greatly reduced size and weight for more demanding applications.

The design case study considered in this paper is for a semiconductor package for use in a power converter where the semiconductor devices are switched at high frequency to ensure good input and output current waveforms. The power dissipated in the semiconductors, and therefore the heatsink weight however increases with the switching frequency, whereas the associated filtering components will be smaller and lighter at higher frequencies. The optimisation of the overall system weight therefore involves a trade-off between the heatsinking and filtering requirements rather than just determining the optimum heatsink design for a specific power dissipation, so it is important to be able to identify the sensitivity of the semiconductor package weight to such design parameters.

Power semiconductor package structures. High power devices such as IGBTs are traditionally packaged using structures such as that shown in figure 1, where the die are soldered to a direct bonded copper (DBC) substrate, which is in turn soldered to the package base. Heat is conducted from the semiconductor device through the various electrically conductive, dielectric and joining layers and then through a bolted interface into a heatsink, which is typically extruded aluminium, although cast and fabricated heatsinks are

increasingly being used in more demanding applications. The heat is then conducted through the heatsink cooling fins which provide a large surface area from which the heat is finally transferred to the cooling medium, principally by convection.

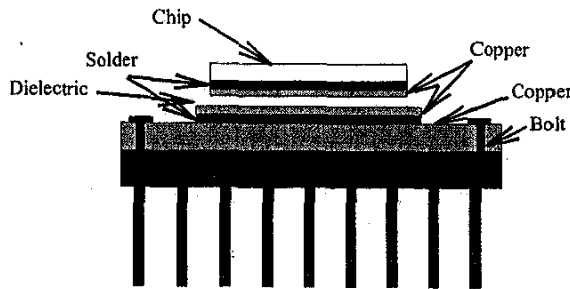


Figure 1 A traditional power semiconductor package and heatsink

In an integrated heatsink design the heat is still conducted through various layers, which may be the same as those in a traditional package (although the opportunity exists to eliminate some of the layers), but the fins are attached directly to the package baseplate as is shown in figure 2.

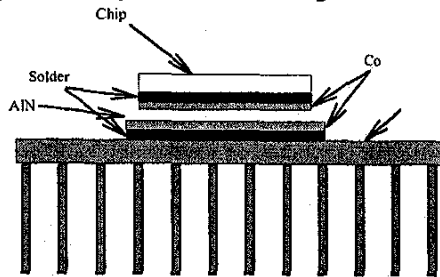


Figure 2 An integrated heatsink power semiconductor package

This type of structure offers the potential for substantial weight savings but the required finning will depend on both the use environment of the package and on the device power dissipation in the specific circuit design, rather than the absolute current rating of the device. The package will therefore be application specific. In the package design discussed here the baseplate material chosen is an Aluminium/Silicon Carbide metal matrix composite (MMC), which has been developed to have a low density, low thermal expansion coefficient and high thermal conductivity [1]. Table 1 shows the key thermal properties of typical materials used in semiconductor packages compared with HIVOLC, a high volume fraction Al/SiC MMC developed by AEA Technology.

Despite its low density HIVOLC also compares favourably with copper in terms of volumetric heat capacity, an important factor in transient thermal performance.

Table 1: Thermo-mechanical properties of some typical semiconductor packaging materials

Material	CTE ($\times 10^{-6}/K$)	C_p (J/gK)	Thermal Conductivity (W/mK)	Density (g/cm ³)
Silicon	3.5	0.77	150	2.33
Copper	17	0.385	385	8.9
Aluminium	23	0.913	200	2.7
Cu-W85	7.0	0.17	197	16.4
Molybdenum	5.2	0.25	150	10.22
Cu-Mo85	6.5	0.275	160	10.0
Be-BeO	8.7		210	2.1
HIVOLC	6.5	0.75	>200	3.21

FIN HEAT TRANSFER MODELLING

In the design of forced air cooling systems for electronic equipment such as computer workstations the air flow is unconstrained within the enclosure and complex 3D fluid flow models must be used to evaluate the air flow distribution within the enclosure and how it interacts with the individual semiconductor device heatsinks e.g. [2]. However, in the type of high power system being considered here, the cooling air flow will be ducted to the heatsink and therefore when designing the heatsink fins consideration need only be given to two things, i.e. the cooling fin dimensions must be selected to obtain sufficient cooling and at the same time the pressure drop through the fins must be kept to a level such that the required air flow can be supplied by the cooling air supply system. As the air flow is a simple ducted flow, empirical correlations can adequately model these parameters, greatly simplifying the design process.

The temperature of the cooling fin surface, T_{fin} , depends on the temperature of the surroundings $T_{ambient}$, the temperature rise of the air as it absorbs heat from the fins, ΔT_{air} , and the temperature rise of the fins above the air in the cooling ducts, $\Delta T_{fin-air}$. Simple empirical relationships have been derived [3] for the plate fin geometry shown in figure 3 which can be used to estimate fin and air temperature rises at any altitude and ambient temperature.

The major simplifying assumptions made in utilising these correlations are that: (a) the air flow is turbulent, (b) the ducts are narrow compared to their height above the base and (c) the

fins are perfectly conducting. In spite of the approximate nature of the relationships, the equations are useful in estimating the cooling capability of a design and studying how changes in fin dimensions will affect performance.

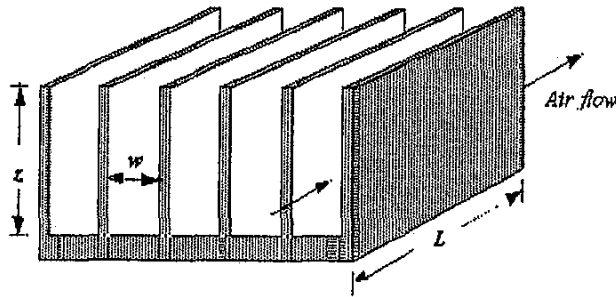


Figure 3 Diagram showing a typical plate-fin heatsink

The fin geometry cannot be selected arbitrarily as it also affects the pressure required to force air through the fins. In a well-designed cooling system, the major part of the pressure drop will be in the cooling fins. The dimensions of the fins affect both the heat transfer and the pressure drop, and any design is a compromise between the two.

An approximate formula for estimating the pressure drop through cooling fins as a function of their dimensions is also given [3] which can be used to determine how changes in fin dimensions will affect the pressure drop.

MODELLING OF CONDUCTION IN THE PACKAGE

An IGBT package will typically contain two or more individual IGBT devices, plus their associated protection diodes. The exact temperatures of each device will therefore depend on the arrangement of the devices within the package and 3D modelling techniques are necessary in order to evaluate the exact temperatures which all of the die will operate at. It is however possible to estimate their temperatures fairly accurately using highly simplified modelling approaches.

One-dimensional models. An analytical model of an IGBT and the required heatsink arrangement has been developed using the relationships discussed in the previous section. The model has been parameterised and incorporated in a spreadsheet allowing the study of the effects of different geometries, materials and air flow rates on the IGBT junction temperature.

For a prismatic slab of material with uniform heat load the basic relationship for one-dimensional heat conduction

between the two faces may be used [4]. In structures encountered in electronic packages however, the area available for conduction along the thermal path is not normally uniform. Relationships have however been derived which allow approximate calculation of thermal resistances in such cases e.g. [5]. Such analytical representations of the heat flow however only approximately represent the spreading of heat in the lateral direction, and some judgement must be used as to how far spreading will occur within each layer of the package. The thermal resistance of the whole package may then be estimated by summing the individual layer resistances.

Two-dimensional conduction models. Analytical heat transfer models, although useful for a quick assessment of the design, are limited in their use, as heat spreading within the different layers is only roughly approximated. It is also difficult to satisfactorily model transient situations. More detailed models are therefore required to carry out further analysis on a selected design and to study the effect of power transients on the die temperature.

Axisymmetric FE modelling is a commonly used technique for the modelling of structures which are symmetric about an axis of rotation and are subjected to axisymmetric boundary conditions. Axisymmetric models have also been shown to be effective for modelling of the displacements in non-rotationally symmetric structures such as semiconductor die attach, although such models do not adequately capture the stresses at the corners of the structure [6]. Axisymmetric models have also been shown to adequately model the thermal resistances of such structures [7]. Axisymmetric models have therefore been used for evaluation of the transient thermal performance. Figure 4 illustrates an axisymmetric representation of an IGBT package structure where each layer is approximated as a cylinder having the same volume as that of the corresponding layer in the real geometry.

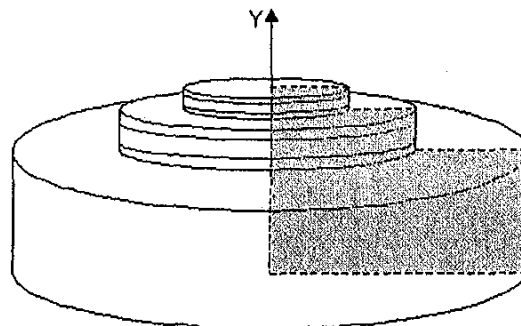


Figure 4 Axisymmetric representation of an IGBT structure

Axisymmetric FE models have therefore been used to provide a more detailed representation of conduction through these multilayer structures whilst avoiding the complexity of a full 3D model. Convective transfer to the environment from the base of the heatsink is approximated through a uniform heat transfer coefficient which takes into account the effect of the extended surface area provided by the fins. Figure 5 illustrates an axisymmetric finite element model of a die mounted onto a baseplate using a DBC structure.

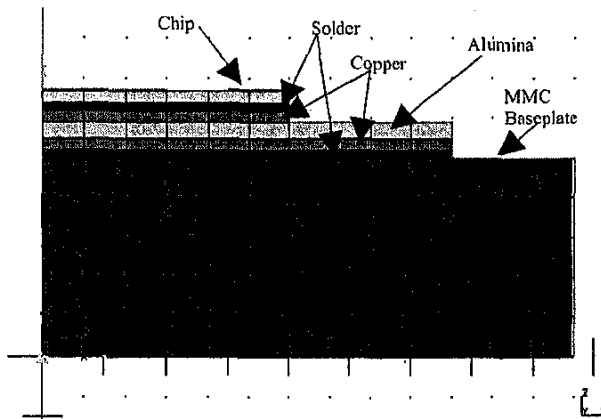


Figure 5 2D axisymmetric FE model of an IGBT heatsink structure

Three-dimensional models. Ultimately, the most accurate representation of a truly three-dimensional (3D) structure is a full 3D FE model. Only with this type of model can the detailed effects of the module layout be established. Manufacturing defects, such as solder joint voids, can also only be satisfactorily modelled using a 3D model. However, this type of model is much more difficult to develop and, due to the far greater number of degrees of freedom within the model, much longer simulation times result. Three-dimensional models are therefore only feasible for detailed evaluation of a particular design, rather than for extensive design trade-off analyses.

MODELLING RESULTS

One-dimensional. A spreadsheet based analytical model of power semiconductor packages has been developed based on the relationships mentioned in the previous section, thereby allowing studies of the effects of different geometries, materials and air flow rates on the thermal performance. This spreadsheet model is divided into two sections. The first calculates the thermal resistances of each layer in the structure and uses these values to estimate the maximum allowable

temperature at the base of the heatsink fins for the specified power and maximum junction temperature. The second part uses this information to calculate the fin height requirements. The number of fins and fin widths, etc. are parameterised so that the effect of different fin configurations can be studied. For each fin geometry, the pressure drop through the fins, and the weight and volume of the subsequent structure is also available in tabular and graphical form to allow the user to select the optimum design. A more detailed explanation and results are given in [8].

The spreadsheet program has been used to estimate the finning requirements for a proposed IGBT/heatsink structure. The total power dissipation is spread equally over a number of IGBTs and their maximum allowable continuous junction temperature is 125°C. Devices are mounted on the package baseplate using an alumina DBC substrate. The heatsink is assumed to be cooled by air at the worst case specified by ARINC-600 [9], i.e. air at 70°C and with a flow rate of 220 kg/hr.kw and at an air pressure of 0.5 atmospheres. It is also assumed that the power is dissipated uniformly over the junction region on the top faces of the IGBTs. Figure 6 shows a contour map of the predicted steady state temperatures within the structure for the expected losses.

Two-dimensional. The axisymmetric modelling technique has been used to study the transient temperature rise in an assembly during overload conditions. The calculated steady-state temperatures, using the nominal 204W load, were used as the initial conditions for the transient simulation and the heat transfer coefficient calculated using the spreadsheet model was applied to the entire lower surface of the model. The module was then subjected to a 5 second transient heat load of 465W.

It was found from these transient simulations that, for this particular structure a peak temperature of 175.8 °C would occur after a 5 seconds overload. This was considered to be an excessive temperature rise and efforts have been made to reduce the maximum junction temperatures to around 150 °C under the specified overload conditions. This task has required careful selection of dielectric material, baseplate thickness and size and also the number of the IGBTs. The number of chips is important as it reduces the power dissipation per device, which in turn reduces the peak temperatures.

Further 2D simulations were carried out to explore the effect of increasing the number of the die and of the baseplate area and thickness. The results for two baseplate thicknesses i.e. 3mm and 5mm are shown in figure 7.

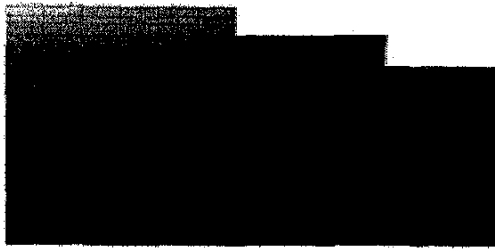


Figure 6 Contour map showing the steady state temperatures within the IGBT heatsink structure

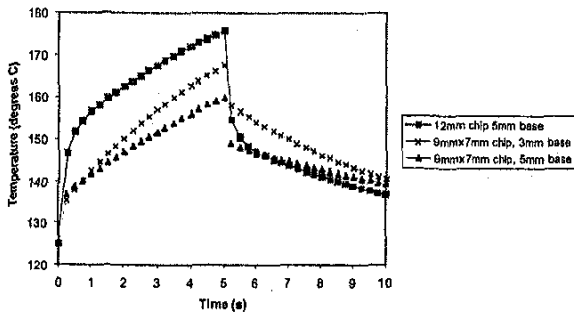


Figure 7 Predicted maximum junction temperature during a transient overload

Figure 7 also shows how the use of 12 smaller (9mmx7mm) chips instead of four 12mmx12mm chips has significantly reduced the peak junction temperature.

A further study was carried out to establish the optimum steady-state base thickness for the package. The results of this study are summarised in figure 8 which shows the maximum junction temperature as a function of baseplate thickness. As expected the junction temperature initially drops with increasing baseplate thickness, due to increased lateral conduction within the base. The junction temperature then starts to rise as an increased thermal resistance is experienced due to the excessive base thickness.

Three-dimensional. Three-dimensional FE models of a number of IGBT layouts have been developed within the I-DEAS/TMG package. Several design layouts using different numbers of standard chip sizes (e.g. 9mmx7mm and 12mmx12mm) and on different baseplate sizes have been considered in an attempt to achieve an optimum thermal performance. The number of IGBTs affects the power

dissipation per chip and baseplate size and thickness govern the thermal mass available for heat dissipation.

As for the 2D models, a heat transfer coefficient is calculated from analytical equations used in the spreadsheet model, which is uniformly applied to the area on the lower surface of the baseplate where the fins are expected to exist.

The results of the analysis on these layouts have led to the following design rules for an improved thermal performance.

- In order to avoid the IGBTs experiencing higher ambient temperatures due to heating of the air as it passes through the fins, the IGBTs should be arranged in a direction normal to the air flow, with only a single chip in any one row along the air flow direction.
- The IGBTs should be fully staggered so that the unpopulated area between the devices is similar. This layout strategy would minimise the spread in the peak temperatures of the IGBTs and hence help with current sharing between the devices.

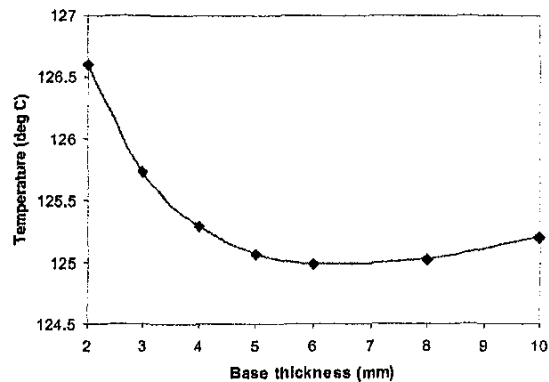


Figure 8 Max steady-state junction temperature as a function of base thickness

The simulation results for an 8-chip in-line arrangement are shown in figure 9. Although this layout has the benefit of ensuring that all the chips experience cooling air of the same temperature, it is however found to lead to a higher spread in the peak junction temperatures of the devices. An improved design, using 12 chips in a fully staggered layout is shown in figure 10. This design has the benefits of both reduced power dissipation per chip and reduced interaction between the adjacent die.

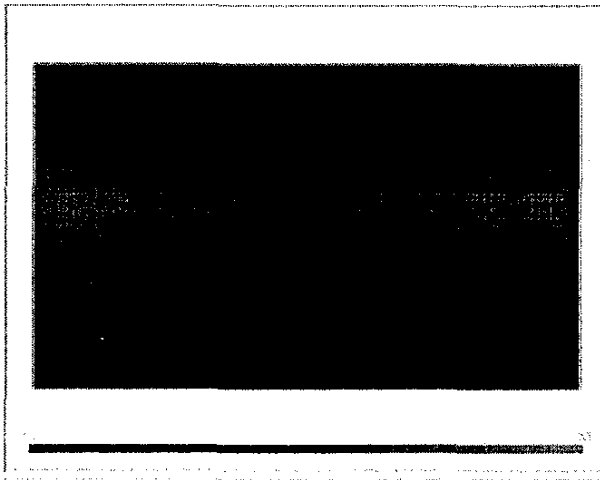


Figure 9 Temperature distribution over a 3D FE model of the 8 chip in line IGBT heatsink structure

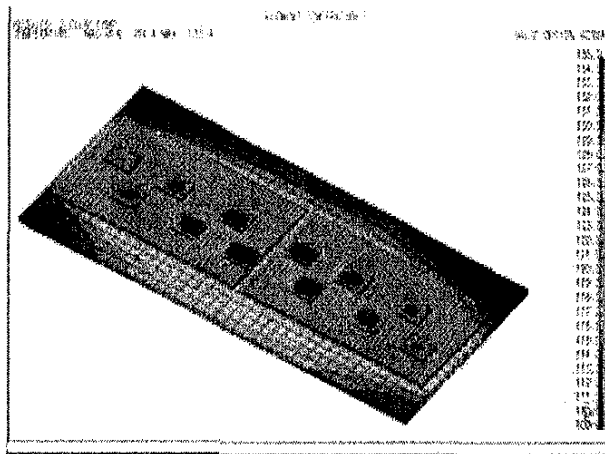


Figure 10 Steady state temperature distribution for a fully staggered 12 chip IGBT heatsink layout

MODEL VERIFICATION

Two different designs of integrated heatsink module were constructed by AEA Technology using HIVOL baseplates and were tested in a purpose built wind tunnel. The results were found to be in good agreement with those from the spreadsheet model as shown in table 2. For the 12-chip module the devices are well spaced out over the available baseplate area and the predicted temperatures are very close to the average temperature measured. For the 8-chip module however the devices are grouped closely together and the degree of heat spreading is therefore limited and there is therefore a greater difference between the predicted and measured temperatures.

Table 2 Comparison of measured and predicted junction temperatures

		Junction temperature (°C)	
		8 Chip Module	12 Chip Module
Measured	Max	80.3	72.6
	Min	74.3	65.7
	Avg	77.1	70.6
Predicted		74.9	71.5

CONCLUSIONS

It has been shown that simple analytical models can be effectively used to carry out rapid design studies on air cooled, high power electronics packages. The steady state results from these models compare favourably with those from wind tunnel testing on prototype modules. These analytical models do not however provide a detailed representation of the effects of package layout on individual device temperatures and more complex 3D models have been developed in order to allow the detailed assessment of the effect of these factors on the actual junction temperatures achieved.

It has been demonstrated that the junction temperatures can be reduced by increasing the number of die and also by fully staggering the chips in a direction normal to the flow. The increase in the size and thickness of the baseplate has also shown to be an effective factor in reducing the junction temperatures under transient overload conditions.

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