III-V/Ge MOS Device Technologies for Low Power Integrated Systems

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ABSTRACT:

CMOS utilizing high mobility III-V/Ge channels on Si substrates is expected to be one of the promising devices for high performance and low power integrated systems in the future technology nodes, because of the enhanced carrier transport properties. In addition, Tunneling-FETs (TFETs) using Ge/III-V materials are regarded as one of the most important steep slope devices for the ultra-low power applications. In this paper, we address the device and process technologies of Ge/III-V MOSFETs and TFETs on the Si CMOS platform. The channel formation, source/drain (S/D) formation and gate stack engineering are introduced for satisfying the device requirements. The plasma post oxidation to form GeO_x interfacial layers is a key gate stack technology for Ge CMOS. Also, direct wafer bonding of ultrathin body quantum well III-V-OI channels, combined with Tri-gate structures, realizes high performance III-V n-MOSFETs on Si. We also

demonstrate planar-type InGaAs and Ge/strained SOI TFETs. The defect-less p^+-n source junction formation with steep impurity profiles is a key for high performance TFET operation.

Index Terms: MOSFET; Tunneling FET; Germanium; III-V semiconductors; Metal-Oxide-Semiconductor; Mobility; Interface states

1. INTRODUCTION

Low power consumption is of paramount importance for advanced CMOS (Complementary Metal-Oxide-Semiconductor)-based logic LSI (Large-Scale Integrated circuits) and integrated systems mainly because of the difficulty in supply voltage (V_{dd}) reduction under realistic CMOS device design. Actually, the V_{dd} lowering is the most effective way in reducing the power consumption of CMOS, P_{consum}, seen in (1).

$$P_{consum} \approx afC_{load}V_{dd}^2 + I_o \cdot 10^{-V_{th}/S} \cdot V_{dd} + I_{leak} \cdot V_{dd} \quad (1)$$

where a, f, C_{load}, I_0, S and I_{leak} are a constant value, the operating frequency, the load capacitance, the drain current at $V_g = V_{th}$, the sub-threshold slope and the additional leakage currents including gate and junction leakages, respectively [1]. Here, the first term corresponds to the dynamic power, while the second and third terms correspond to the static power. In both components, the lowering of V_{dd} can effectively reduce the power consumption.

While the steady progress in suppression of short channel effects and reduction in equivalent oxide thickness can contribute to lowering V_{dd} to some extent, the significant reduction in V_{dd} is difficult for Si CMOS. Here, there are two possible strategies to further reduce V_{dd}. These strategies are schematically shown in Fig. 1. One way is to employ channel materials with higher source injection velocity such as Ge and III-V compound semiconductors. Under ballistic transport limit, on-current, I_{on}, can be simply represented [2-5] by

$$I_{on} = qN_s v_{inj} \approx C_g(V_{dd} - V_{th})v_{inj} \quad (2)$$

where q, N_s, v_{inj}, C_g and V_{th} are elemental charge, surface carrier concentration at source edge, carrier injection velocity at source edge, gate capacitance and threshold voltage, respectively. Since semiconductor channel materials with lower effective mass such as

Ge and III-Vs are known to lead to higher injection velocity, higher I_{on} can be obtained at a given value of V_{dd} [6, 7]. As a result, the III-V/Ge MOSFETs can reduce N_s under a given I_{on} value, resulting in the reduction in V_{dd}, as shown in (2) and Fig. 1. This strategy can contribute to reduction of gate overdrive.

The typical CMOS structures composed of III-V/Ge channels are schematically shown in Fig. 2 [8-10]. Here, Ge with the significantly light hole and light electron effective mass is suitable for p-channel MOSFETs or CMOS applications. In particular, Ge CMOS is plausible in terms of the simplicity of the process/material integration, because the CMOS is composed of a single material. Also, In-based III-V semiconductors such as InGaAs, InAs and InSb with the quite light electron effective mass are suitable for n-channel MOSFET applications, while Sb-based III-V semiconductors such as GaSb, InGaSb and InSb with the light hole effective mass are suitable for p-channel MOSFETs or CMOS applications. Although III-V CMOS is another possible CMOS structure, there can still be many choices of materials for CMOS. This is because III-V materials suitable for n-MOSFETs and p-MOSFETs are different in most cases. Among them, one of the ultimate CMOS structures can be the co-integration of an In-based III-V n-MOSFET and a Ge p-MOSFET [8, 9], because of the superior physical properties including the carrier transport ones as well as the contact resistance with metals.

On the other hand, the other strategy for the reduction in V_{dd} is to introduce devices with steep slope of the channel current change in sub-threshold region. This way can contribute to the reduction in V_{dd} by decreasing the gate voltage swing in the sub-threshold region, as also shown in Fig. 1. Here, the inverse of the slope of the channel current change with respect to gate voltage, V_g, defined as the sub-threshold

slope (S.S.), which is the V_g change necessary to change channel currents by one order of the magnitude, is known to have the minimum value of ~60 mV/dec. at room temperature for conventional MOSFETs dominated by thermionic current in sub-threshold region. Thus, any new device operation mechanisms are needed to realize sub-threshold slope lower than this minimum value.

One of the most promising steep slope devices can be tunneling FETs (TFETs) [11-14], where tunneling probability and resulting tunneling current are modulated by V_g. Typical TFET structures are also shown in Fig. 2. This is because a variety of simulation results have reported the excellent performance of TFETs with the steep slopes [11, 13] and, actually, the device operations with sub-threshold slope less than 60 mV/dec. in a low V_{dd} region typically less than 0.5 V, have already been demonstrated without large hysteresis [15-22]. Also, fabrication of some of TFETs can be regarded as highly compatible with the Si CMOS platform. However, one of the drawbacks in TFETs is the low current drive [11-14], attributed to low tunneling probability. Particularly, Si-based TFETs are known to have the essential limitation in I_{on} and S.S. [11-14], because of the high bandgap energy, E_g, and the indirect bandgap. Thus, III-V/Ge is promising for the materials used in TFETs as well, because of lower E_g, direct bandgap in III-V and various possible combinations of the hetero-structures, which lead to the higher tunneling probability. Here, it is known that the source/channel junctions composed of type-II hetero-structures are effective in enhancing I_{on} of TFETs with maintaining low off current. It has been recognized from this viewpoint that $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ and Si/Ge hetero-interfaces are suitable for advanced TFETs.

As a result, the heterogeneous integration of III-V/Ge with the Si CMOS platform is a promising direction for realizing ultra-low power CMOS and TFETs along More

Moore and Beyond CMOS approaches, respectively, in the 10 nm technology nodes and beyond, where ultra-low power integrated systems are indispensable. In addition, a combination of III-V/Ge-based photonic devices with advanced CMOS can also provide another possible system solution through optical interconnect for minimizing the power consumption of the interconnect under a given system performance, though this aspect is not touched on in this paper.

On the other hand, there are still many critical issues and difficult challenges for realizing III-V/Ge-based CMOS and TFETs on the Si platform [8-10, 14], which are schematically shown in Fig. 3. These include (1) formation of high-crystal-quality Ge/III-V films on Si substrates, where ultrathin body III-V-OI/GOI structures are needed with combination of any carrier transport booster technologies (2) gate stack technologies to realize superior MOS interface quality, leading to MOS gate stacks with ultrathin equivalent oxide thickness (EOT) and low densities of interface states and border traps, high channel mobility and high gate stack reliability including long term threshold voltage (V_{th}) stability (3) the formation of source/drain (S/D) with low resistivity and low leakage current for MOSFETs as well as the steep impurity profiles for TFETs (4) fabrication of ultra-short channel devices, including the optimum channel design and the formation of ultrathin body, Fin or nano-wire (NW) channels with high uniformity of the channel thickness/radius and small surface roughness and (5) total CMOS process integration including an appropriate choice of n- and p-channel MOSFETs and compatibility with the Si CMOS platform.

In this paper, we review the recent progress in device and process technologies of III-V/Ge MOSFETs and TFETs for solving the above critical problems on the basis of our recent research activities. We emphasize the channel formation technologies, MOS

gate stack technologies and channel engineering technologies for III-V MOSFETs. Also, viable technologies for the superior MOS gate stack and the MOSFET performance enhancement are addressed for Ge MOSFETs. Next, we discuss key challenges for TFETs, including the appropriate material choice and the formation of the steep and high quality source junctions, which can provide both high tunneling current and low off current. We mainly present two types of planar TFETs utilizing the InGaAs channels and the Ge/strained Si hetero-structures, where Zn-diffused p^+ InGaAs source junctions and in-situ doping p^+ Ge/sSi, respectively, are employed for realizing steep and defect-less tunnel junction formation.

2. LOW POWER ADVANCED CMOS TECHNOLOGIES

2-1 III-V MOSFET Technologies

The main critical issues of the present III-V MOSFETs for the logic device applications can be high quality III-V channel formation on Si substrates, the fabrication process compatibility with the Si CMOS platform, gate stack reliability including the long term V_{th} stability, realization of high performance III-V p-MOSFETs and establishment of integration scheme as CMOS. For III-V n-MOSFETs, high performance scaled MOSFETs have already been demonstrated at lower V_{dd} for MOSFETs using In-based-channels such as InGaAs and InAs [23-48]. However, most of the devices have been fabricated with the recessed-channel structures on bulk III-V substrates [23, 26-29, 32-37, 40, 42, 43, 46, 48], which are not simply compatible with advanced CMOS logic technologies. While multi-gate III-V MOSFETs have also been demonstrated [25, 26, 37-39, 46-48], no clear evidence of higher performance of fully-scaled NW III-V MOSFETs, strongly expected beyond 10 nm technology nodes,

has been presented yet. Also, the long term reliability of MOS gate stacks on III-V semiconductors can be regarded as a critical issue [49, 50], because of the existence of a large amount of slow traps.

On the other hand, the high performance of III-V p-MOSFETs with high I_{on} and low I_{off} has not been demonstrated yet, which is mainly attributable to the poor MOS interface properties and low material qualities of Sb-based channels. As a result, viable CMOS structures using only III-V channel materials have not been fully identified yet, though several III-V CMOS devices have been reported so far [53-58].

2-1-1 III-V channel formation on Si substrates

Among a variety of difficult challenges in III-V MOSFETs listed above, one of the most difficult ones can be high quality III-V channel formation. One of the promising techniques is direct growth of III-V channels on Si substrates [59-63]. Particularly, the selective growth of limited regions of Si active regions [41, 46, 64-72], called an aspect ratio trapping (ART), is expected to provide a III-V channel formation process compatible with Si CMOS fabrication. Actually, the operation of InGaAs n-MOSFETs fabricated by this ART process has been demonstrated [41, 46, 71]. One of the present problems of III-V channels formed by this selective growth on Si can be inferior quality of materials including buffers, leading to high leakage current and low electron mobility [41].

Another promising approach to form III-V channels on Si is direct wafer bonding of III-V thin films on Si substrates with interfacial insulating layers working as buried oxides (BOX) [24, 30, 53, 56, 73-99]. We have proposed and demonstrated ultrathin body InGaAs-based channel formation by using direct wafer bonding [24, 30, 73-76,

79-85, 87, 89-95, 96]. As ultrathin body (3.2 nm $In_{0.53}Ga_{0.47}As$)/ultrathin BOX (Al_2O_3 (4.4 nm)/SiO_2 (3.3 nm)) channels have been realized with high material quality on Si [24, 76]. Here, the lattice-matched $In_{0.53}Ga_{0.47}As$ channel was epitaxially grown on a 4-inch InP substrate with interfacial $In_{0.53}Ga_{0.47}As$/InP super-lattice layers as etching stop, meaning that the high material quality of the $In_{0.53}Ga_{0.47}As$ channel can be guaranteed. Thin atomic layer deposition (ALD) Al_2O_3 and SiO_2 films were formed on the $In_{0.53}Ga_{0.47}As$/InP substrate and a Si substrate, respectively. The ALD Al_2O_3 layer is suitable for the buried oxide layer of III-V-on-insulator structures, because of the strong bonding property as well as better MOS back interface properties of III-V channel layers. After bonding of the two wafers in air, the InP substrate was selectively etched by HCl, which can provide quite high difference in the etching rate between InP and InGaAs, allowing us to realize ultrathin InGaAs-on-insulator (-OI) structures with high thickness uniformity. We have already confirmed high electron mobility and excellent performance of MOSFETs using InGaAs-OI fabricated by the direct wafer bonding [24, 30, 73-76, 79-85, 87, 89-95, 96].

This wafer bonding process is also applicable to other III-V channels. We have successfully fabricated GaSb-OI structures on Si by employing the similar wafer bonding technology [56, 98, 100]. The process flow and cross-sectional transmission electron microscope (TEM) images of the fabricated GaSb-OI on Si structure are shown in Fig. 4(a) and (b), respectively. Here, GaSb films grown on 2-inch (100) InAs wafers were used as the initial substrate. The Al_2O_3 BOX layers were deposited on both GaSb/InAs and Si wafers by ALD. After manually bonding the wafers in air, the InAs substrates were selectively etched from GaSb, resulting in formation of a 23-nm-thick GaSb/Al_2O_3/Si structure with excellent GaSb thickness uniformity and smooth GaSb

front and back interfaces. We have also confirmed the operation of p-MOSFETs using the bonded GaSb-OI structure on Si [56, 98, 100]. These results suggest the versatility and the effectiveness of direct wafer bonding in terms of high quality III-V channel formation on Si substrates.

On the other hand, one essential drawback of the above process is the limited wafer size, because III-V channel layers are grown on small size III-V substrates like InP and InAs with a diameter of typically 2-4 inch. This limited wafer size makes an essential difficulty in transferring the channel layers to Si substrates with a diameter of 12 inch and beyond. In order to solve this essential problem, we have proposed and demonstrated a fabrication process of InGaAs-OI by wafer bonding of an InGaAs layer grown on a Si donor wafer instead of the one grown on an InP donor wafer [99, 101]. By using III-V channels grown on Si, III-V-OI structures on Si substrates with any available wafer size can be prepared. Recently, the similar technology has also been reported by the other group [44, 102, 103].

Fig. 5(a) shows the process flow of InGaAs-OI wafers by the direct wafer bonding technique newly developed. Here, 4-inch Si wafers were used for the proof-of-concept demonstration of the proposed fabrication process. However, the same process is also applicable to 12-inch Si wafers. First, InGaAs channels were grown on Si wafers with InAlAs/GaAs buffer layers by Molecular Beam Epitaxy (MBE). Here, 50-nm-thick-InGaAs films on Si show Hall electron mobility of 6550 cm^2/Vs at 300 K with an electron concentration of 1.5×10^{17} cm^{-3}, suggesting that the good film quality is obtained even on Si wafers. ALD Al_2O_3 was deposited on the III-V/Si wafers, followed by chemical mechanical polishing (CMP) for the surface smoothing, which is necessary for wafer bonding. After HfO_2 deposition on both Al_2O_3/III-V/Si and Al_2O_3/Si wafers,

the two wafers were bonded to each other. Finally, InGaAs-OI on Si wafers were formed by etching the top Si, the GaAs and the InAlAs buffer layers by tetra-methyl-ammonium hydroxide (TMAH), citric acid and HCl based solutions, respectively. Fig. 5(b) and (c) show cross-sectional TEM images of the bonded InGaAs-OI wafer with body thickness (T_{body}) of 10 nm before and after wafer thinning, respectively. It is found that high quality and uniform 10-nm-thick InGaAs-OI, transferred from a Si donor wafer, can be formed on a Si substrate.

In order to evaluate the electrical properties of MOSFETs using the present InGaAs-OI layers on Si, InGaAs-OI MOSFETs were fabricated with a gate stack composed of 10 nm Al_2O_3 and Ta gate metal and Ni-InGaAs metal S/D. The I_d-V_g characteristics of InGaAs-OI MOSFETs with T_{body} of 9 nm and L_G of 1 μm are shown in Fig. 6(a). Very good transfer curves were obtained with S.S. of 100 mV/dec and I_{on}/I_{off} ratio higher than 10^6. Fig. 6(b) shows the comparison in μ_{eff} of InGaAs-OI MOSFETs at N_s of 10^{12} cm^{-2} between InP and Si donor wafers as a function of T_{body}. InGaAs-OI MOSFETs fabricated from the Si donor wafer exhibit high mobility comparable to that from the InP donor wafer, indicating that the present wafer fabrication process can realize sufficiently-high quality InGaAs-OI on Si wafers with the same level as those obtained from the InP donor wafer. Fig. 6(c) shows the cumulative distribution of leakage current (I_{leak}) of the InGaAs-OI MOSFETs fabricated from both the Si and InP donor wafer at L_G of 1 μm and V_d of 0.05 V. Here, I_{leak} of MOSFETs is very sensitive to the quality of channel layers. It is found that I_{leak} of MOSFETs fabricated from the Si donor wafer is very uniform and even lower than that from the InP donor wafer, indicating low defect density and high material quality of fabricated InGaAs transferred from the Si substrate. These results clearly demonstrates that the proposed direct wafer

bonding from III-V channel layers grown on Si can provide excellent scalability of III-V-OI wafer up to Si wafers with a diameter larger than 300 mm while maintaining high device quality.

2-1-2 III-V MOS gate stack technology

Formation of III-V gate stacks with thin EOT, low interface defects and realization of the sufficient long-term reliability are also quite challenging requirements. Among the long history of III-V MOS interface studies [104, 105], one of the important achievements recently obtained is the formation of better MOS interface properties of III-V channel materials such as GaAs, InGaAs and GaSb with ALD Al_2O_3 and HfO_2 films as gate insulators in terms of the reduction in interface state density (D_{it}) [106-114]. These improved MOS properties have been often attributed to low temperature and soft deposition by the ALD process and the self-cleaning effects of the metal-organic ALD sources on III-V native oxides or III-V surfaces [106-110], though universal understanding of the physical origin of the interface states at III-V MOS structures has not been fully obtained yet. On the other hand, the effectiveness of the ALD process on the III-V gate stack formation can contribute significantly to realizing scaled III-V MOSFETs, because of potential ultrathin EOT, applicability to multi-gate structures and mass-production friendliness.

ALD Al_2O_3 films can be regarded as quite suitable for InGaAs MOS interface stabilization. Thus, HfO_2/Al_2O_3 stack gate insulators have been often used for InGaAs in order to simultaneously realize thin EOT and superior MOS interface properties [37, 41, 114-116]. Since thinner Al_2O_3 thickness is better in this gate stack in terms of EOT, we have studies how thin Al_2O_3 can effectively reduce D_{it} by systematically changing

the thickness of Al_2O_3 in the ALD Al_2O_3/HfO_2 gate stacks [113]. As a result, it has been found that the insertion of only 0.2-nm-thick ultrathin Al_2O_3 interfacial layers (ILs) for HfO_2/InGaAs interfaces can effectively reduce D_{it} down to the level for sufficiently-thick Al_2O_3/InGaAs interfaces [113, 114]. This gate stack allows us to realize HfO_2(2nm)/Al_2O_3(0.2nm)/InGaAs MOS capacitors with capacitance effective thickness (CET) of 1.08 nm and gate leakage current of 2.4×10^{-2} A/cm^2.

On the other hand, the remaining issues on the III-V gate stacks can be (1) the minimum D_{it} values at InGaAs MOS gate stacks with Al_2O_3 ILs are typically still around in lower half of 10^{12} cm^{-2}eV^{-1} order, which are higher than in Si and Ge MOS gate stacks (2) MOS interface properties on Sb-based materials such as GaSb, GaAsSb and InGaSb are still poor (3) MOS gate stack reliability such as PBTI reliability seems not to be able to satisfy the realistic criterion [49-52]. While the examination of the MOS reliability and possible physical origins of reliability degradation is on-going, appropriate choices of gate stacks and treatments are still needed.

For further reduction in D_{it} at InGaAs MOS interfaces, recent studies have revealed that ALD La_2O_3/InGaAs MOS interfaces can provide lower D_{it} than Al_2O_3/InGaAs ones [117, 118], which can provide a new MOS interface engineering scheme. Also, it has been reported that trivalent oxides such as Al_2O_3, Y_2O_3, and La_2O_3 can provide better interfaces with III-V semiconductors than HfO_2, because of the well-arranged chemical bonding and the abrupt interfaces [119]. Thus, we have systematically examined the InGaAs MOS interface properties by using ALD La_2O_3, InGaAs [118]. Fig. 7 shows the comparison in *C*-*V* curves of Al_2O_3 (3.5 nm)/InGaAs, Al_2O_3 (3.5 nm)/La_2O_3 (0.4 nm (10 cycles))/InGaAs and Al_2O_3 (3.5 nm)/La_2O_3 (2.9 nm (40 cycles))/InGaAs MOS gate stacks with Au gate electrodes, where post metallization annealing (PMA) in N_2 at 300

^{o}C for 1 min was performed. Here, La(iPrCp)$_3$ and H_2O were used as the precursors for La_2O_3. The ALD mode deposition rate at 150 ^{o}C was 0.1 nm/cycle with incubation of around 7 cycles.

Fig. 8 shows D_{it} of Al_2O_3 (3.5 nm)/La_2O_3/InGaAs at the surface energy of 0.1 eV from the midgap as a function of the La_2O_3 ALD cycle number, corresponding to the change in the La_2O_3 thickness from 0 nm to 2.9 nm. Here, data of La_2O_3 (2.9 nm (40 cycles))/InGaAs MOS gate stacks without Al_2O_3 has also been added in the Fig. 8. The D_{it} values were determined by the conductance method. It is found that quite low D_{it} of $\sim 3\times10^{11}$ cm^{-2}·eV^{-1}, which is lower than that in the TiN/W/La_2O_3/InGaAs gate stacks reported in [117], is obtained for La_2O_3 (2.9 nm (40 cycles))/ InGaAs MOS. However, the hysteresis of the *C-V* curves becomes larger with an increase in the La_2O_3 thickness, shown in Fig. 7(b), suggesting the existence of a high density of slow traps in La_2O_3. On the other hand, reducing the La_2O_3 ILs can decrease in the hysteresis. Also, D_{it} of Al_2O_3 (3.5 nm)/La_2O_3 (0.4 nm)/InGaAs is lower than that of Al_2O_3/InGaAs, though Al_2O_3 ALD increases D_{it} even for 2.9-nm-thick La_2O_3 IL, presumably due to a reaction of Tri-methyl-aluminium (TMA) with the La_2O_3 ILs. These results indicate that ALD La_2O_3 ILs, combined with Al_2O_3, can compromise the reduction in both D_{it} and slow trap density and, thus, that La_2O_3 can work as a promising high-k IL for InGaAs gate stacks.

From the viewpoint of the realization of III-V p-MOSFETs or CMOS, on the other hand, MOS structures of Antimonide-based channels such as GaSb [30, 96, 120-127], InGaSb [53-55, 88, 100, 125, 128, 129] and InSb [130-132] have stirred a strong interest. While some of the Sb-based devices have shown the high hole mobility, the MOS interface properties are still much poorer than those of InGaAs, which must be a

critical issue for high performance devices. In particularly, Sb-based materials with lower energy difference between the valence band edge and the vacuum level are also promising for the application of TFETs employing type-II hetero-structures, which will be described in the next section. Thus, the improvement in the MOS interfaces of the Sb-based materials is a key issue for realizing high performance of TFETs.

It is known for GaSb gate stacks that ALD Al_2O_3/GaSb MOS interfaces have much higher D_{it} than Al_2O_3/InGaAs ones, suggesting that the effect of the TMA cleaning effect might not be effective for GaSb surfaces. It has been reported [133] that the GaSb MOS Interface properties are sensitive to the ALD temperature, which must be lower than 200 ^oC for obtaining better MOS interfaces. In addition, one of the promising ILs for passivating GaSb surfaces is ultrathin InAs layers [134-136]. Here, the choice of the InAs thickness is important, because too thick InAs can simply work as an InAs channel. In addition, the ultrathin InAs can change from the broken band lineup of InAs/GaSb to the type-II staggered one because of the quantum confinement effect of electrons in the conduction band of InAs, leading to suppression of a leakage path through the broken-gap InAs/GaSb interface [56]. Fig. 9 shows the *C-V* curves of the Al_2O_3/InAs/p-GaSb MOS capacitors with the InAs thickness of 0, 0.5, 1.5 and 3 nm, measured at room temperature. Here, the unintentionally-doped InAs layers were grown on p-type (100) GaSb wafers with carrier concentration (N_A) of ~1×10^{17} cm^{-3} by metal organic chemical vapor deposition (MOCVD). After that, 5-nm-thick ALD Al_2O_3 layers were deposited on the InAs/GaSb wafers at 150 ºC, after the pre-cleaning using an $(NH_4)_2S_x$ solution. The capacitance modulation with changing gate voltage is limited for the MOS capacitors with 0- and 0.5-nm InAs passivation, suggesting large D_{it}. On the other hand, the C-V curves are found to improve with an increase in the InAs thickness

up to 1.5 nm, demonstrating the effectiveness of the InAs passivation on the GaSb MOS interface properties.

Fig. 10 shows the relationship between D_{it} and the surface energy from the midgap energy as a parameter of the InAs thickness of 0, 0.5, 1.0, 1.5, and 2.0 nm. Here, D_{it} was evaluated from the 1 MHz *C-V* curves at 100 K by using the Terman method. The Al_2O_3/InAs (1.5 nm)/p-GaSb MOS capacitors exhibits the lowest minimum D_{it} of ~6.6×10^{12} $cm^{-2}eV^{-1}$ at -0.24 eV, which is reduced by ~50% from that of ~1.4×10^{13} $cm^{-2}eV^{-1}$ in the Al_2O_3/p-GaSb MOSCAPs. These results indicate that InAs ILs with an appropriate thickness can significantly improve the GaSb MOS interface properties, probably due to suppression of GaSb surface oxidation and/or Sb sublimation from the surfaces by the InAs ILs. However, further careful optimization of the gate stack formation process and the demonstration of much lower D_{it} and higher effective mobility are still strongly needed for convincingly proving that GaSb-based MOS devices are really promising for future logic applications.

2-1-3 III-V channel engineering technology

In order to apply III-V channels to the scaled CMOS, suppression of short channel effects (SCE) is mandatory, in addition to high carrier injection velocity. Form this viewpoint, ultrathin body structures as well as multi-gate structures like FinFETs and NW FETs must also be embodied by III-V channels on Si without any degradation of the material and interface qualities. Actually, there have recently been many reports on III-V-channel FinFETs [37, 44], Tri-gate MOSFETs [25, 37-39, 41] and NW MOSFETs [26, 46-48, 71]. We have focused on ultrathin-body III-V-OI structures on Si wafers [8, 24, 30, 31, 38, 39], fabricated by wafer bonding, with thickness below 10 nm. One of

the strong concerns in such thin channels is the mobility reduction with decreasing T_{body}, attributable to the body thickness fluctuation scattering [137, 138]. In order to mitigate this mobility degradation due to thickness fluctuation of a single InGaAs-OI layer, two types of channel structure engineering have been employed [30, 38, 87, 94, 139]. One consists in increasing the In content of main InGaAs channels up to pure InAs and the other is the introduction of MOS interface buffers, where the higher-In-content main channels are sandwiched by lower-In-content InGaAs buffers having front and back MOS direct interfaces. By employing this quantum well (QW) channel structure, the wave function of electrons can be confined more into the center of the channels with higher In content, resulting in higher mobility due to lower effective mass in the InGaAs channel with higher In content, reduction in Coulomb scattering by MOS interface charges and mitigation of the influence of the QW total thickness fluctuation [94, 139]. It has been found that n-MOSFETs with an $In_{0.3}Ga_{0.7}As$ (3nm)/InAs (3nm)/ $In_{0.3}Ga_{0.7}As$ (3nm)-OI channel, fabricated on Si substrates, provides high electron mobility of 3180 cm^2/Vs at 300 K. We have also demonstrated operation of MOSFETs with the channel length (L_{ch}) of 20 nm using this channel structure on Si, exhibiting high I_{on} of 2.4 mA/μm at V_{dd} of 0.5 V [31, 140].

In order to realize high performance InAs MOSFETs with further improved SCE immunity, Tri-gate $In_{0.3}Ga_{0.7}As$ (3nm)/InAs (3nm)/ $In_{0.3}Ga_{0.7}As$ (3nm)-OI QW MOSFETs have been fabricated by narrowing the gate width of the InGaAs-OI channels [38, 39]. Fig. 11 shows the device structure and the schematic process flow. A Fin-like tri-gate channel structure with top gate width (W_G) of down to 36 nm and (111) facet side channel surfaces were formed by chemical wet etching of InGaAs layer. A top view Scanning Electron Microscope (SEM) photograph of a tri-gate MOSFET with a narrow

channel width is also shown in Fig. 11. Here, Ta/Al_2O_3 gate stack and Ni-InGaAs metal S/D were employed.

Fig. 12(a) shows the I_d-V_g characteristics of the $In_{0.3}Ga_{0.7}As$/InAs/$In_{0.3}Ga_{0.7}As$-OI tri-gate MOSFETs with L_{ch} of 20 nm as a parameter of W_G of 40, 50, 140, and 360 nm. Severe SCEs were observed in the MOSFETs with W_G wider than 100 nm, whereas SCEs were effectively suppressed in MOSFETs with narrower W_G. The effect of the tri-gate structure on SCE is more clearly seen in drain-induced barrier lowering (DIBL) of MOSFETs. Fig. 12(b) shows the characteristics of DIBL with different W_G as a function of L_{ch}. While the severe DIBL is observed for the InGaAs-OI tri-gate MOSFETs with wide W_G in L_{ch} less than 100 nm, DIBL becomes much reduced with W_G narrower than 50 nm. These results strongly indicate that the side gate effect with narrow W_G in tri-gate MOSFETs can significantly suppress SCEs in L_{ch} less than 50 nm.

Fig. 12(c) shows I_{on} at V_{dd} of 0.5 V and I_{off} of 100 nA/μm characteristics with different W_G as a parameter of L_{ch}. Here, the gate voltage was shifted from the measured I_D-V_G characteristics so as to provide I_{off} of 100 nA/μm. I_{on} of ~380 μA/μm has been obtained under V_d and V_g of 0.5 V. On the other hand, the saturation behavior of I_{on} in short L_{ch} is attributed to relatively large S/D resistance of 410 Ωμm in the present devices, caused by the long distance between the gate and the pad electrodes, and unintentional thinning of the Ni-InGaAs S/D layers due to over etching of unreacted Ni during the device fabrication. Thus, the optimizations of the device geometry and the process conditions are expected to provide further enhancement of device performance.

Fig. 13 shows a benchmark of I_{on} at V_d of 0.5 V with gate overdrive of 0.5 V, taken from the present $In_{0.3}Ga_{0.7}As$/InAs/$In_{0.3}Ga_{0.7}As$-OI tri-gate MOSFETs [38, 39] and reported advanced InGaAs MOSFETs [25-29, 32, 35-37, 40-48]. Here, V_g has been

shifted so that I_{off} at gate overdrive of 0 V amounts to 100 nA/μm in order to guarantee the suppression of SCEs. The present devices are found to exhibit high level I_{on}, obtained among the advanced InGaAs MOSFETs with shorter L_{ch}.

2-2 Ge MOS Technologies

2-2-1 Ge MOSFET technologies

Ge MOSFETs have been intensively studied in recent years and more mature device technologies have been demonstrated, compared to the III-V ones. In particular, Ge p-MOSFETs seem close to real applications, because good performance of short-channel Ge and high-Ge content SiGe FinFETs have already been demonstrated [141-149]. The relatively high I_{off} can be one of remaining problems as low power applications. Also, higher performance of NW MOSFETs [149-152] would need to be demonstrated for future scaled technology nodes.

In contrast, Ge n-MOSFETs and resulting CMOS are still suffering from lower I_{on} and poorer MOS gate stack reliability, though intensive developments on Ge n-MOSFETs and CMOS have been conducted [153-185]. Here, a key technology to realize high performance Ge n-MOSFETs with high I_{on} is superior MOS interface control and gate stack technologies satisfying the requirements of thin EOT, high channel mobility, low S.S. and high gate stack reliability. Among them, MOS gate stack reliability can also be regarded as a critical problem for Ge p-MOSFETs without any Si passivation. As a result, MOS interface control engineering is still of paramount importance for Ge MOSFETs.

2-2-2 Ge MOS gate stack technology

Among a variety of gate insulators and/or interface control layers on Ge, attention has recently been paid to GeO_2/Ge-based interfaces [150-156, 158-176, 179-183, 185-213], because of the superior interface properties and resulting high carrier mobility in Ge MOSFETs. Particularly, high electron mobility can be obtained only for Ge n-MOSFETs with GeO_2/Ge interfaces [153-156, 158-176, 179-183]. In order to realize low D_{it} and thin EOT at the same time for Ge-oxide-based ILs, we have proposed an IL formation process employing Electron cyclotron resonance (ECR) oxygen plasma to form GeO_x ILs after thin ALD HfO_2/Al_2O_3 stacks [162-164, 166, 204-207]. The basic process flow is shown in Fig. 14. Here, Al_2O_3 serves as a sufficient oxygen barrier that suppresses the growth of unnecessarily-thick GeO_x IL, thanks to its intrinsic oxygen permeability, as well as a passivation layer that prevents Ge MOS interfaces from ECR plasma damages and process damages during the successive fabrication processes.

Figure 15 shows EOT and D_{it} of the Au/HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/Ge MOS capacitors at -0.2 eV from the midgap as a function of the plasma post oxidation time. It is found that high D_{it} of ~10^{12} $cm^{-2}eV^{-1}$ in the HfO_2/Al_2O_3/Ge gate stack without plasma post oxidation rapidly decreases even with a very short term plasma exposure of 5 s and continuously decreases with an increase in the plasma oxidation time. In contrast, EOT increases only from 0.72 to 0.82 nm with the plasma post oxidation of 25 s. As a result, ECR plasma oxidation can sufficiently reduce D_{it} at small expense of the increase of EOT less than 0.1 nm.

It has been observed, on the other hand, that ECR plasma oxidation of HfO_2/Ge direct stacks provides inferior MOS interface properties with high D_{it}, attributed to the inter-mixing of HfO_2 and GeO_x, and the higher Hf content at MOS interfaces. Thus, the insertion of ultrathin Al_2O_3 films is needed as an inter-diffusion control layer against

HfO_2. The results of Fig. 15 indicate that 0.2-nm-ultrathin Al_2O_3 can suppress the inter-diffusion and form GeO_x ILs between Al_2O_3 and Ge, maintaining the effectiveness of ECR post plasma oxidation even for HfO_2-based gate stacks.

One of the remaining critical issues for the Ge MOS gate stacks is the existence of a large amount of slow traps and the resulting poor BTI (bias-temperature instability) characteristics [49, 50, 162, 214], as described above. Fig. 16 shows examples of the influence of slow traps on MOSFET characteristics. The amount of hysteresis in forward and backward scan sweep of I_d-V_g characteristics of Ge n- and p-MOSFETs with Al_2O_3/GeO_x/Ge gate stacks and the time dependence of I_d are shown in Fig. 16(a) and (b), respectively. The larger hysteresis and larger current drift are observed for n-MOSFETs, meaning that a larger amount of slow traps exist near the conduction band edge of Ge than the valence band edge.

While the physical origin of these slow traps is attributable to any structural defects in gate insulators including Ge oxides, Al_2O_3 [49, 50] and/or HfO_2, it has not been identified yet. However, the reduction in the amount of slow traps responsible for BTI and the significant improvement in the reliability lifetime are mandatory for applying Ge MOSFETs to real applications. It has been recently reported that Y-doped GeO_x interface layers fabricated by sputtering can provide the MOS interface properties with small hysteresis and low D_{it} [168, 169, 183, 215]. These results suggest that appropriate doping of Y atoms into Ge oxides and Al_2O_3 near Ge interfaces can reduce the slow trap density and improve the BTI reliability. Thus, we have examined the impact of ALD Y_2O_3 and $AlYO_3$ gate stacks on the slow trap density [216].

Fig. 17 shows C-V curves of 1.5-nm-thick Al_2O_3/GeO_x/p-Ge with plasma post oxidation, 1.5-nm-thick $AlYO_3$/p-Ge MOS capacitors without plasma post oxidation

and 1.5-nm-thick $AlYO_3/GeO_x$/p-Ge MOS capacitors with plasma post oxidation. Here, $AlYO_3$ was deposited as an ALD mode by alternatively supplying $Al(CH_2)_3$ and $(CpMe)_3Y$ cycle by cycle. Since pure Y_2O_3/Ge gate stacks with and without plasma post oxidation were observed in this study to exhibit large hysteresis and thus have no improvement in the slow trap density, the properties of $AlYO_3$/Ge gate stacks were mainly studied. It is observed in Fig. 17 that $AlYO_3/GeO_x$/Ge has smaller hysteresis than Al_2O_3/GeO_x/Ge with plasma post oxidation and 1.5-nm-thick $AlYO_3$/Ge MOS capacitors without plasma post oxidation.

D_{it} and slow trap areal density, ΔN_{fix}, were quantitatively compared among these three MOS interfaces by the conductance method and the hysteresis measurement [49, 50], respectively. Fig. 18(a) shows the energy distribution of D_{it} at the $AlYO_3$/Ge MOS interface before and after plasma post oxidation. It is confirmed that plasma posit oxidation is also effective in reducing D_{it} at the $AlYO_3$/Ge MOS interface down to almost the same level of as that in the conventional Al_2O_3/GeO_x/Ge interfaces with plasma post oxidation. Fig. 18(b) also shows ΔN_{fix} of 1.5-nm-thick $AlYO_3/GeO_x$/p-Ge and n-Ge MOS capacitors and 1.5-nm-thick Al_2O_3/GeOx/n-Ge and p-Ge MOS capacitors as a function of the effective electric field across gate insulators, E_{ox} given by $(|V_{gmin}-V_{FB}|)/$ CET). Here, ΔN_{fix} was evaluated from the amount of hysteresis in C-V curves with changing the minimum gate voltage, V_{gmin}, with keeping the maximum voltage constant, according to [49, 50]. It is found that ΔN_{fix} of the $AlYO_3/GeO_x$/p-Ge interface becomes lower than that of Al_2O_3/GeO_x/p-Ge interface, while the reduction in ΔN_{fix} for n-Ge is small for the $AlYO_3/GeO_x$/Ge interface. These results mean that $AlYO_3$-based gate stack can reduce the amount of slow traps near the valence band of

Ge against the conventional Al_2O_3/GeO_x/Ge interfaces. It is also confirmed that the slow trap density near the conduction band edge is much higher than that that near the valence band edge. Thus, further improvements on the Ge gate stacks are still strongly needed to reduce the slow trap density, particularly, near the conduction band edge.

2-2-3 Ge MOSFET performance improvement

Thanks to the recent progress in Ge gate stack technologies, high mobility and high on-current of Ge n- and p-MOSFETs have been demonstrated by many groups. Among them, the gate stacks with Ge-oxide-based ILs can be regarded as the unique MOS interfaces leading to high electron mobility in Ge n-MOSFETs, attributed to lower D_{it} and interface defects near the conduction band edge. Note that Si-passivation ILs [217-222], well known as effective in high hole mobility in p-MOSFETs, would not seem to work well for n-MOSFETs, because of quite small conduction band discontinuity and no electron confinement at Si/Ge interfaces, though the improvement of Ge n-MOSFETs with Si-passivated MOS interfaces has been still pursued [184]. We have also demonstrated the operation of n- and p-MOSFETs with the $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks, shown in Fig. 16, under EOT of 0.76 nm [164, 166]. Fig. 19 shows I_d-V_g characteristics of (100) Ge p- and n-MOSFET with the HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x (0.35 nm)/Ge gate stack having EOT of 0.78 nm at V_d of 50 and 200 mV. Well-behaving I_d-V_g curves are demonstrated for these MOSFETs, with I_{on}/I_{off} ratio of ~10^4 for both p- and n-MOSFETs. The values of S.S. of the p- and n-MOSFETs are 90 and 85 mV/dec, respectively, indicating the sufficient passivation of interface traps on the GeO_x/Ge MOS interfaces

We have confirmed that high electron and hole mobility are obtained in comparison

with the thick GeO_2/Ge mobility and the Si mobility, particularly in high N_s region, in spite of this ultrathin EOT. The peak electron and hole mobility of 689 and 546 cm^2/Vs have been obtained. These results strongly demonstrate that $HfO_2/Al_2O_3/GeO_x$/Ge gate stacks can realize high performance Ge n- and p-MOSFETs with minimal mobility degradation under aggressive EOT scaling.

Recently, we have found two important factors for further improving the effective mobility of Ge MOSFETs with GeO_x ILs. One is the relationship between the plasma oxidation temperature and MOS interface roughness. TEM analyses and the comparison with the theoretical surface roughness mobility through the experimental MOS interface geometry taken from the real TEM data [164, 170, 173, 223] have revealed that plasma oxidation at room temperature reduces GeO_x/Ge MOS interface roughness, leading to the increase in the effective mobility in high N_s region, where surface roughness scattering is dominant. By lowering plasma post oxidation temperature from 300 ^oC to room temperature, the electron and hole effective mobility at N_s of 10^{13} cm^{-2} have been improved by 20 % and 25 %, respectively, as a consequence of the reduction in the MOS interface roughness.

The other finding is the effectiveness of atomic deuterium (D) annealing on the reduction in D_{it} inside the conduction and valence bands [164, 173] and the resulting increase in the effective mobility [167, 185]. Fig. 20(a) shows the effective and Hall electron mobility in Al_2O_3/GeO_x/Ge n-MOSFETs after post deposition annealing (PDA) at 400 °C, in N_2 ambient or with atomic D, in comparison with the effective mobility reported previously [159, 160, 168]. It is found that the electron effective mobility in the high N_s region is enhanced after the atomic D PDA. On the other hand, the Hall mobility, which is much higher than the effective mobility, does not change with and without

atomic D PDA, indicating that the carrier transport properties and scattering probability do not change with atomic D PDA. Note that the effective mobility determined by the split *C-V* method is affected by trapping of carriers into traps under the inversion condition, while Hall measurements allow us to directly evaluate free electron concentration.

Actually, we can quantitatively evaluate the trapped electron concentration as a function of surface potential by comparing N_s evaluated by the split *C-V* and Hall measurements under an assumption of the Hall factor of unity. Fig. 20(b) shows the energy distributions of D_{it} inside the conduction band, evaluated by Hall measurements for Al_2O_3/GeO_x/Ge n-MOSFETs with PDA in N_2 and atomic D ambient. It is found that a large amount D_{it} exist inside the conduction band, which leads to the significant reduction in the effective mobility in high N_s region. The existence of similar amounts of D_{it} inside the band has been confirmed in the Ge valence band [164, 173] and InGaAs conduction band [224-226], which has been regarded as one of the important mobility degradation factors in high N_s region. It is found that atomic D PDA can reduce the amount of D_{it}, which is the origin of the increase in the effective mobility with atomic D PDA. These results strongly suggest that further deeper understanding of the mechanisms limiting the inversion-layer mobility in Ge MOSFETs or any MOS interface is still necessary, and possible mitigation of these limiting factors is expected to further enhance the performance of Ge MOSFETs.

3. Tunneling FET TECHNOLOGIES

3-1 Importance and critical issues of Tunneling FETs (TFETs)

As described in the introduction, devices enabling steeper slopes than conventional

MOSFETs are also strongly required to realize ultralow power circuit operation with much reduced V_{dd}. Among a variety of the proposals on such steep slope devices, TFETs based on the band-to-band tunneling mechanism can be regarded as one of the most promising ones. This is because the principle of the device operation can promise TFETs to reduce S.S. down to less than ~60 mV/dec. at room temperature, the minimum value of MOSFETs, through the combination of the tunneling distance modulation by gate voltage with the filtering effect of the tunneling electron energy due to the necessity of overlapping the energy distributions of density-of-states (DOS) between the conduction and valence bands of semiconductors [11-13]. In addition to the many simulation results verifying this concept, [11-13, 227] the operations with S.S. less than 60 mV/dec. have been experimentally demonstrated at low V_{dd} (< typically 0.5V) without hysteresis. Also, while many TFET structures have been proposed, the typical ones are composed simply of reversed p-n junctions of homo- or hetero-interface semiconductors with MOS gate stacks, which can be compatible with the present CMOS platform.

However, the present TFETs have still hold many problems and challenges listed as follows; (1) Si TFETs have lower I_{on} because of the comparatively high bandgap and reduced tunneling probability due to indirect tunneling (2) In p-n junction type TFETs, the tunneling distance is not sufficiently small in some cases because of the graded source impurity profiles, leading to lower I_{on} (3) Generation-recombination centers in semiconductors, interface defects at MOS interfaces and tail states within the bandgap of semiconductors, existing in real TFETs, significantly degrade S.S and I_{off} through Shockley-Read-Hall (SRH) carrier generation mechanism and trap-assisted tunneling (TAT). In particular, this issue is serious for any other new materials including III-V/Ge

and 2-dimensional materials than Si. (4) Insensitive and ineffective control of channel potentials at tunneling points by gate voltage due to un-optimized device structures and/or higher MOS interface defects also significantly degrades S.S. The increase in controllability of channel potential by gate potential can be basically realized by similar device engineering as used to suppress SCE in advanced CMOS devices, such as such ultrathin body structures, multi-gate structures and thin EOT of gate stacks.

As a consequence, the drive current level of reported TFETs exhibiting S.S. less than 60 mV/dec [15-22] is still quite low and resulting averaged S.S. over drive current range needed for realistic applications is still too high. Also, TFETs with comparatively high drive current have a tendency to yield higher I_{off} and S.S. values. Note that low I_{off} and high I_{on}/I_{off} ratio are quite critical to ultra-low power applications at which TFETs are aiming. Thus, any-TFET-specific engineering for achieving the optimum materials, device structures and fabrication process must be strongly pursued for simultaneously realizing both low S.S. of sub-60 mV/dec. over a wide range of the current level, low I_{off} and high I_{on}/I_{off} ratio.

Fig. 21 schematically summarized our device/material engineering for solving these critical issues and challenges of TFETs [14]. One of the key issues is the channel material engineering for enhancing tunneling current with maintaining low I_{off}. Since the sufficient tunneling current would not be able to be obtained for Si with the large E_g and the indirect bandgap allowing phonon-assisted tunneling, other semiconductors with narrower bandgaps like Ge, InGaAs and InAs are promising for increasing I_{on}, because of the higher tunneling probability due to narrower E_g and the direct bandgap for III-V semiconductors. On the other hand, one of possible drawbacks with source homo-junction TFETs with narrower E_g is the increase in I_{off} and the degradation in

I_{on}/I_{off} due to the higher generation-recombination rate.

In order to solve this trade-off problem in the bandgap, a type-II hetero-structure source junction is effective in reducing tunneling distance and increasing I_{on} without reduction of the bandgap in the drain junction, which would lead to the increase in I_{off}. Fig. 22(a) and (b) schematically show the band lineup of the type-II hetero-structure and a band diagram of the source p-n junction region composed of the type-II hetero-structure. It is confirmed here that the potential barrier against electrons tunneling from the source semiconductor to the channel semiconductor (effective bandgap), E_{geff}, can be reduced from both bandgaps of the source and channel semiconductors, E_{g1} and E_{g2}, thanks to the valence and conduction band discontinuity in the type-II hetero-structure, ΔE_c and ΔE_v, indicating that higher tunneling probability is expected with maintain low source and drain junction leakage currents, directly associated with E_{g1} and E_{g2}.

The second important engineering issue is to demonstrate a superior MOS gate stack formation yielding thin EOT and low MOS interface defect density at the same time. While this engineering is basically similar to that in advanced CMOS technologies, the realization of such gate stacks is still challenging for semiconductors other than Si. In addition, a novel requirement of the gate stacks specific to TFETs with type-II hetero-structures is to realize thin EOT and low MOS interface defect density for two different materials of the source and the channel such as Ge/Si [19] and GaAsSb/InGaAs [228-232] by employing the same gate stack formation process, which is not trivial under the different MOS interface physics and chemistry of the two semiconductors. Also, the requirement of low MOS interface defect density could be more stringent in TFETs than in MOSFETs, because MOS interface defects can degrade

S.S. and I_{off} through two mechanisms of the reduction of gate potential control over MOS surface potential as well as the increase in TAT and SRH currents via the interface defects.

The third engineering is related to source p-n junction formation, which has peculiar requirements in p-n junction type TFETs. Here, the high steepness of the source impurity profile with low defect density around p-n junctions are strongly required in terms of the thin tunneling distance and low SRH current, which significantly contribute to high I_{on} and low I_{off}, respectively. Finally, the drain junction engineering is also important for suppressing ambipolar current and reducing I_{off}. When gate potential is biased to form the accumulation region near MOS interfaces, the drain/channel junctions can induce tunneling current as the ambipolar current, which limits the I_{off} level. Thus, it is necessary to minimize this ambipolar current for suppressing I_{off} and increasing I_{on}/I_{off} ratio through any optimization of the drain structure and/or graded profiles of drain impurities.

In this paper, we emphasize the channel material engineering and the source junction engineering. For the channel material engineering, we have examined TFETs using an $In_{0.53}Ga_{0.47}As$ channel as a low and direct band gap material [14, 233, 234], and TFETs using a combination of a Ge source and a strained-Si channel [14, 235, 236] as a type-II hetero-junction TFET in order to enhance I_{on}. We have realized these devices as the planar structure, which is still effective in easy fabrication under standard CMOS processes and integration with conventional Si CMOS. We have developed novel source junction engineering for InGaAs TFETs. Diffusion of solid phase Zn diffusion into InGaAs is introduced for realizing source junctions with steep Zn profiles and low defect density.

3-2 InGaAs TFETs

InGaAs can be regarded as one of promising materials of TFETs, because of the high tunneling probability due to the narrow and direct bandgap, and recent progress in InGaAs MOSFET technologies. Here, formation of the source junctions with defect-free and steep impurity profiles is mandatory for InGaAs TFETs. In general, it would not be too easy to form such defect-less p-n junctions with steep impurity profiles by ion implantation, because of the difficulty in complete re-crystallization of ion-implanted III-V semiconductors by thermal annealing without significant impurity diffusion and defect generation. From the viewpoint of these requirements, we have introduced solid-phase Zn diffusion in InGaAs because of the extremely-steep profiles coming from the inherent diffusion property of Zn in InGaAs and the defect-less process [233, 234, 237, 238].

It is known that Zn diffuses in InGaAs as interstitials. Here, the following balance equation holds [238].

$$[\mathrm{Zn}]^- + 2h \Leftrightarrow [\mathrm{Zn_{int}}]^+ + [\text{III vacancy}] \quad (3)$$

where [Zn], h, [$\mathrm{Zn_{int}}$] and [III vacancy] are substitutional Zn concentration, hole concentration, interstitial Zn concentration and column-III-element-vacancy concentration in InGaAs, respectively. As a result, the diffusion constant of Zn is in proportion to $[\mathrm{Zn}]^2$. In order to examine the effect of the [Zn] dependence of the diffusion constant on the profile, the Zn diffusion profiles are simulated for three types of hypothetical diffusion coefficients, which are assumed to be constant, proportional to [Zn] and proportional to $[\mathrm{Zn}]^2$ ones for simplicity.

Fig. 23 shows the calculated Zn profiles under the three diffusion constant models. It is found that the diffusion coefficient proportional to $[Zn]^2$ yields the steepest Zn profile. This abrupt change of the Zn concentration can be easily understood by the sharp decrease of the diffusion coefficient proportional to $[Zn]^2$ with decreasing [Zn], leading to the box-like Zn profile under this diffusion constant. These simulation results strongly suggest that InGaAs p^+-n junctions formed by Zn diffusion have an inherently steep Zn profile. In addition, solid phase diffusion by using Zn-doped spin-on-glass (SOG) films is expected to provide p-n junctions with a low defect density, because of the damage-less nature of this doping process in comparison with ion implantation. As a result, the Zn solid phase diffusion by SOG is promising for the formation of source junctions in InGaAs TFETs.

Zn diffusion from the Zn-doped SOG was driven by rapid thermal annealing (RTA) at 500 ^oC for 1 minute in a N_2 ambient [233, 234]. Be and Zn ion implantation was also carried for comparison [239]. Fig. 24(a) shows the Secondary Ion Mass Spectrometry (SIMS) profiles of diffused Zn and implanted Be atoms. It is found that the steepness of the Zn profile is 3.5 nm/dec., which is much steeper than that of the Be profile formed by Be implantation with the energy of 2 keV and the dose of $1x10^{15}$ cm^{-2}, 36 nm/dec. This result is consistent with the profile calculated using the model that the diffusion constant of Zn in InGaAs is proportional to the square of the Zn concentration, also shown in Fig. 24(a), confirming that the steep impurity profile can be automatically obtained by solid phase Zn diffusion. Actually, the real steepness can be less than 3.5 nm/dec., which could be determined by atom mixing during the SIMS analysis, as expected in the simulation result.

Fig. 24(b) shows the *I-V* characteristics of Zn-diffused, Zn-implanted and

Be-implanted $In_{0.53}Ga_{0.47}As$ p^+-n junctions. Here, Be ion implantation was carried with the energy of 10 keV and the dose of $1x10^{15}$ cm^{-2}, and Zn ion implantation was carried with the energy of 25 keV and the dose of $2x10^{14}$ cm^{-2}. The activation annealing for Be and Zn ion implantation was carried by RTA at 600 ^oC and 650 ^oC, respectively, for 1 minute. The Zn-diffused and Be-implanted junctions show the lower ideal factor of 1.2, while the Zn-implanted diode shows the higher ideal factor of 1.7. Also, the minimum current under the reverse bias condition is lowest for the Zn-diffused junctions. These results mean that the Zn diffusion introduces fewer defects than ion implantation for p-n junction formation.

Planar-type $In_{0.53}Ga_{0.47}As$ n-channel TFETs with source regions formed by the present Zn diffusion process were fabricated on semi-insulating InP substrates [233, 234]. The device structure is shown in the inset of Fig. 25(a). A Ta/ALD Al_2O_3 (3 nm) gate stack and a Ni-InGaAs metal-drain were employed. Fig. 25(a) and (b) show the I_D-V_G characteristics at V_D of 150 mV and the I_D-V_D characteristics, respectively, of the $In_{0.53}Ga_{0.47}As$ TFETs with source regions formed by Zn diffusion at 500 ^oC for 1 min. It is found in Fig. 25(a) that the $In_{0.53}Ga_{0.47}As$ TFETs exhibit the small minimum S.S. of 64 mV/dec. and the high I_{on}/I_{off} ratio of ~$2x10^6$ at the same time as the planar-type III-V TFETs with EOT of 1.3 nm. Also, the good drain current saturation is clearly observed in Fig. 25(b). The comparatively low S.S. values and high I_{on} are also attributable to narrow tunneling distance in the source p-n junctions with the steep Zn profile and resulting high tunneling probability. Also, the comparatively low I_{off} and high I_{on}/I_{off} are attributable to low source junction leakage current coming from the defect-less p-n junctions formed by Zn diffusion process. Actually, similar promising electrical characteristics of InGaAs TFETs with Zn-diffusion sources have recently been

confirmed by another research group [240].

Actually, the low leakage current in the present p-n junctions due to SRH and/or TAT is evident in the temperature dependence of the I_d-V_g characteristics. Fig. 26 shows the temperature dependence of I_d-(V_g-V_{th}) characteristics at V_D of 150 mV of an InGaAs TFET with the source region formed by Zn diffusion at 500 ^{o}C for 1 min from 6 K to 292 K. Here, V_{th} was defined as V_g at I_d of 10^{-7} A/μm. Measurement temperatures were varied from 6 K, 50 K, 171 K, 227 K, 254 K to 292 K. Almost no temperature dependence was observed in the subthreshold region, which means that S.S. is almost free from trap-related SRH and TAT currents. This point is quite important, because many previous works on III-V TFETs have reported that the S.S. values have strong temperature dependence and, thus, have been severely degraded by the existence of defects and traps included in source p-n junctions and MOS interfaces. As a consequence, the result of the temperature dependence also supports the fact that the superior p^{+}-n source junctions suitable for TFETs can be formed by Zn solid phase diffusion in InGaAs.

In addition, the results of Fig. 26 indicate that band-to-band tunneling dominates the current of the present TFETs. We have observed the negative differential resistance under the negative drain bias, which is another evidence of the dominance of tunneling mechanism on the carrier transport. Actually, such a weaker temperature dependence of the drain current can be one of possible advantages of TFETs, particularly for applications requiring device operation under a wider temperature range, in comparison with conventional MOSFETs.

3-3 Ge/strained-SOI TFETs

As emphasized in the section 3-1, the source-channel structures composed of type-II staggered hetero-interfaces, shown in Fig. 22, are quite effective in enhancing the performance of TFETs. Thus, several TFETs using type-II hetero-interfaces such as $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ [228-232] and InAs/Si [20, 241, 242] have been intensively studied. We have recently proposed a novel type-II hetero-interface TFETs using Ge/tensily-strained Si interfaces [235, 236]. Fig. 27(a) shows the schematic band diagram of the hetero-interface of Ge and tensile strain Si. The higher valence band edge (E_V) of the Ge-source and the lower conduction band edge (E_C) of tensile strain Si result in reduction in E_{geff}, leading to the increase the tunneling probability and I_{on} and the reduction in S.S. with maintaining the relatively large E_g of strained-Si in the drain regions, which can suppress the ambipolar leakage current. It has already been reported that pure Ge sources grown on Si have provided Si TFETs with minimum S.S. lower than 60 mV/dec. Also, tensily-strained Si has been regarded as one of the promising materials for TFET channels, because of the smaller bandgap. Actually, tensily-strained Si TFETs with SiGe sources [243, 244] or NW structures [18, 245] have already been reported. Thus, we have combined the Ge source and strained-SOI channels in order to realize the type-II hetero-structure TFETs.

The Ge/strained Si TFET structure, fabricated in this study, is shown in Fig. 27(b) [235, 236]. In order to examine the impact of tensile strain on the TFET performance, unstrained SOI and two types of strained SOI substrates with 0.8 and 1.1 % biaxial tensile strain were employed. In-situ boron-doped Ge layers were grown at 200 ^oC on the source regions of the substrates by MBE. Here, low temperature in-situ doping can lead to steep boron profiles with high boron concentration of as high as 1.3×10^{20} cm^{-3}. A 3-nm-thick Al_2O_3/GeO_x/Ge gate stack with EOT of 2.5 nm was formed by ALD

combined with ECR plasma post oxidation in order to realize the high quality MOS interfaces between Al_2O_3 and Ge [8, 9], as described in the section 2-2-2. Ta was deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. It was found that one of the key processes is PMA at 400 ^oC in N_2 for 30 minutes.

Fig. 28 shows the I_d-V_d characteristics of Ge-source TFETs fabricated on un-strained SOI, 0.8 and 1.1 % strained SOI substrates. It has been found that an increase in strain leads to the increase in I_{on}. It has also be observed that gate current and resulting I_{off} decrease with an increase in the amount of tensile strain, because of the increase in the barrier height in E_C between insulators and strained Si [246], resulting in higher I_{on}/I_{off} with increasing the amount of tensile strain. Here, we have observed that PMA temperature strongly affects the electrical properties of TFETs. PMA at 400 ^oC can maximize the I_{on}/I_{off} ratio, which amounts to 4.4, 2.2 and $3.7x10^7$ for the unstrained, 0.8 and 1.1 % strained SOI TFETs, respectively, and can significantly reduce the S.S. values, which amount to 55, 49 and 29 mV/dec. as the minimum value at room temperature for unstrained, 0.8 and 1.1 % strained SOI TFETs, respectively. This improvement in the TFET performance with increasing PMA temperature is attributed to reduction in D_{it} at the Si MOS interfaces, while D_{it} at the Ge MOS interfaces does not change with PMA [247]. These results mean that the combination of plasma post oxidation through Al_2O_3 and optimized PMA can simultaneously realize the appropriate MOS interface properties for both the Ge source and the strained-Si channel.

Fig. 29 shows a benchmark of the present n-channel TFET performance [233, 234, 236] in terms of I_{on}/I_{off} ratio versus the minimum S.S. value with other reported ones [18-20, 243, 248-254] with a variety of channel materials. It is found that the high I_{on}/I_{off}

ratio under the low minimum S.S. can be obtained for the present InGaAs and Ge/strained SOI n-channel TFETs. Further improved performance of these TFETs can be expected by employing thinner EOT gate stacks, optimized drain junctions and multi-gate/NW channel architectures. As a consequence, the InGaAs and Ge source/strained-Si TFETs can be regarded as ones of the superior TFET structures for realizing low I_{off} and high I_{on} at the same time.

4. CONCLUSIONS

We have addressed critical issues and challenges for enhancing the performance of Ge/III-V MOSFETs and TFETs, which are strongly expected as devices for realizing ultralow power integrated systems. In order to solve these problems, viable technologies have been presented in this paper. For realizing high performance Ge CMOS, GeO_x IL formation by plasma post oxidation and atomic D annealing were developed. $HfO_2/Al_2O_3/GeO_x/Ge$ gate stacks formed by this method have realized high performance Ge n- and p-MOSFETs with EOT of 0.76 nm having D_{it} of ~$3x10^{11}$ $cm^{-2}eV^{-1}$, whose peak electron and hole mobility amount to 689 and 546 cm^2/Vs, respectively. The InGaAs/InAs/InGaAs-OI QW channels combined with Tri-gate structures have been introduced for the technologies enhancing the performance of III-V n-MOSFETs. The InGaAs/InAs/InGaAs-OI QW Tri-gate n-MOSFETs with the Fin width of ~40 nm have offered I_{on} of ~380 μA/μm at V_d and V_g of 0.5 V under I_{off} of 100 nA/μm. A fabrication technique of the InGaAs ultrathin body channels on large size Si wafers has also been demonstrated. Also, the effectiveness of Ge/III-V materials on TFETs through the enhancement of tunneling probability has been demonstrated. Superior junction formation and MOS interface control technologies are key factors to

realize TFETs using Ge/III-V. The p^+-n junction formation in InGaAs using Zn diffusion has realized excellent planar $In_{0.53}Ga_{0.47}As$ n-TFET characteristics, because of the defect-less source junctions with steep Zn profiles. Ge/tensily-strained Si n-TFETs with the type-II hetero-interfaces have also been found to exhibit high I_{on}/I_{off} ratio and low minimum S.S., because of reduction in effective E_g, steep B profiles by in-situ B doping in Ge and improved MOS interface properties with both Ge and strained Si.

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FIGURE CAPTIONS

Fig. 1: Two possible strategies to further reduce V_{dd}.

Fig. 2: Possible structures for advanced MOSFETs and TFETs using III-V/Ge devices on Si platform through heterogeneous integration

Fig. 3: Critical issues for realizing III-V/Ge MOSFETs and TFETs on the Si platform

Fig. 4: (a) Fabrication process of GaSb-OI substrates (b) Cross-sectional TEM images of 23-nm-thick GaSb-OI on a Si wafer

Fig. 5: (a) Fabrication process of InGaAs-OI wafer by direct wafer bonding technique using InGaAs on a Si donor wafer. InGaAs/$In_xAl_{1-x}As$/GaAs layers are epitaxially grown on Si substrates. After Al_2O_3 deposition as a BOX layer, CMP has been carried out for surface smoothing for Al_2O_3/III-V/Si wafer and wafers were bonded each other. Subsequent wet etching thinned the top Si and the III-V buffer layers, resulting in the formation of InGaAs-OI on Si substrates. (b) Cross-sectional TEM image of the bonded Si/III-V/BOX/Si wafer before top Si, III-V buffer etching. (c) Cross-sectional TEM image of InGaAs-OI on Si after top Si, III-V buffer etching. A high resolution image is also shown.

Fig. 6: (a) Measured I_d-V_g characteristics of InGaAs-OI MOSFETs using an InGaAs layer on a Si donor wafer (b) μ_{eff}-T_{body} characteristics of InGaAs-OI MOSFETs on the wafer from an InP and a Si donor wafer (c) Cumulative distribution of the leakage current at L_G of 1 μm and V_D of 50 mV.

Fig. 7: C-V curves of (a) Al_2O_3 (3.5 nm)/InGaAs, (b) Al_2O_3 (3.5 nm)/La_2O_3 (0.4 nm (10 cycles))/InGaAs and (c) Al_2O_3 (3.5 nm)/La_2O_3 (2.9 nm (40 cycles))/InGaAs MOS gate stacks with Au gate electrodes

Fig. 8: D_{it} of Al_2O_3 (3.5 nm)/La_2O_3/InGaAs at the surface energy of 0.1 eV from the midgap as a function of the La_2O_3 ALD cycle number, corresponding to the change in the La_2O_3 thickness from 0 nm to 2.9 nm. Here, data of La_2O_3 (2.9 nm (40 cycles))/ InGaAs MOS gate stacks without Al_2O_3 has also been added

Fig. 9: *C-V* curves of the Al_2O_3/InAs/p-GaSb MOS capacitors with the InAs thickness of (a) 0, (b) 0.5, (c) 1.5 and (d) 3 nm, measured at room temperature.

Fig. 10: Energy distribution of D_{it} of the Al_2O_3/InAs/p-GaSb MOS capacitors with the InAs thickness of 0, 0.5, 1.0, 1.5, and 2.0 nm. The surface energy is taken from the midgap energy of GaSb. Here, D_{it} was evaluated from the 1 MHz *C-V* curves at 100 K by using the Terman method.

Fig. 11: Device structure and the schematic process flow of InGaAs-OI tri-gate MOSFETs using $In_{0.3}Ga_{0.7}As$ (3nm)/InAs (3nm)/$In_{0.3}Ga_{0.7}As$ (3nm)-OI QW channels. A top view Scanning Electron Microscope (SEM) photograph of a tri-gate MOSFET with a narrow channel width is also shown.

Fig. 12 (a) I_d-V_g characteristics of the $In_{0.3}Ga_{0.7}As$/InAs/$In_{0.3}Ga_{0.7}As$-OI tri-gate MOSFETs with L_{ch} of 20 nm as a parameter of W of 40, 50, 140, and 360 nm (b) DIBL characteristics with different W_G as a function of L_{ch} (c) I_{on} at V_{DD} of 0.5 V and I_{off} of 100 nA/μm characteristics with different W_G as a parameter of L_{ch}

Fig. 13: Benchmark of I_{on} at V_d of 0.5 V with gate overdrive of 0.5 V, taken from the present $In_{0.3}Ga_{0.7}As$/InAs/$In_{0.3}Ga_{0.7}As$-OI tri-gate MOSFETs and reported advanced InGaAs MOSFETs. Here, V_g has been shifted so that I_{off} at gate overdrive of 0 V amounts to 100 nA/μm.

Fig. 14: Proposed Al_2O_3/GeO_x/Ge and $HfO_2/Al_2O_3/GeO_x$/Ge gate stack formation process by oxidation using ECR oxygen plasma through a thin Al_2O_3 and a thin

HfO_2/Al_2O_3 layer, respectively, by ALD

Fig. 15: EOT and D_{it} of the Au/HfO_2 (2.2 nm)/Al_2O_3 (0.2 nm)/GeO_x/Ge MOS capacitors with different plasma post oxidation times at 0.2 eV from the midagap

Fig. 16: (a) Hysteresis in forward and backward scan sweep of I_d-V_g characteristics of Ge n- and p-MOSFETs with TiN/Al_2O_3/GeO_x/Ge gate stacks (b) time dependence of I_d of the Ge n- and p-MOSFETs with GeO_x thickness of 0.27 and 1.2 nm at constant V_d and V_g values

Fig. 17: C-V curves of (a) 1.5-nm-thick Al_2O_3/GeO_x/Ge with plasma post oxidation, (b) 1.5-nm-thick $AlYO_3$/Ge MOS capacitors with plasma post oxidation and (c) 1.5-nm-thick $AlYO_3$/GeO_x/Ge MOS capacitors with plasma post oxidation. The measurement frequency was varied from 1 K, 10 K, 100 K to 1 MHz.

Fig. 18: (a) Energy distributions of D_{it} at 1.5-nm-thick $AlYO_3$/Ge MOS interfaces with and without plasma post oxidation (b) Relationship between E_{ox} and ΔN_{fix} of 1.5-nm-thick $AlYO_3$/GeO_x/p-Ge and n-Ge MOS capacitors and 1.5-nm-thick Al_2O_3/GeO_x/n-Ge and p-Ge MOS capacitors.

Fig. 19: I_d-V_g characteristics of (100) Ge p- and n-MOSFET with the $HfO_2/Al_2O_3/GeO_x$/Ge gate stack having an EOT of 0.78 nm

Fig. 20: (a) Effective and Hall electron mobility of Al_2O_3/GeO_x/Ge n-MOSFETs with N_2 and atomic deuterium PDA in comparison with the effective mobility reported previously [159, 160, 168] (b) D_{it} inside the conduction band, evaluated by Hall measurements for Al_2O_3/GeO_x/Ge n-MOSFETs with PDA in N_2 and atomic deuterium ambient.

Fig. 21: Device/material engineering for solving these critical issues and challenges of p-n junction-type TFETs

Fig. 22: (a) Schematic band lineup of the type-II hetero-structure and (b) band diagram of the source p-n junction region composed of the type-II hetero-structure.

Fig. 23: Calculated Zn profiles under the three diffusion constant models, where diffusion coefficients are constant, proportional to [Zn] and proportional to $[Zn]^2$ ones.

Fig. 24: (a) SIMS profiles of diffused Zn and implanted Be atoms in InGaAs. Here, Zn was diffused at 500 ^oC for 1 minute in a N_2 ambient. Be was introduced by Be implantation with the energy of 2 keV and the dose of $1x10^{15}$ cm^{-2}. Also, the solid curve shows the profile calculated using the model that the diffusion constant of Zn in InGaAs is proportional to the square of the Zn concentration. (b) *I-V* characteristics of Zn-diffused, Zn-implanted and Be-implanted $In_{0.53}Ga_{0.47}As$ p^+-n junctions.

Fig. 25: (a) I_d-V_g characteristics at V_d of 150 mV of an $In_{0.53}Ga_{0.47}As$ TFET with source regions formed by Zn diffusion at 500 ^oC for 1 min. Inset is the schematic structure of the $In_{0.53}Ga_{0.47}As$ TFET (b) I_d-V_d characteristics of the $In_{0.53}Ga_{0.47}As$ TFET.

Fig. 26: Temperature dependence of I_d-(V_g-V_{th}) characteristics at V_d of 150 mV of an InGaAs TFET with the source region formed by Zn diffusion at 500 ^oC for 1 min from 6 K, 50 K, 171 K, 227 K, 254 K to 292 K. Here, V_{th} is defined as V_g at I_d of 10^{-7} A/μm.

Fig. 27: (a) Schematic band diagram of the hetero-interface of Ge and tensile strain Si (b) fabricated Ge/strained Si TFET structure

Fig. 28: I_d-V_d characteristics of Ge-source TFETs fabricated on un-strained SOI, 0.8 and 1.1 % strained SOI substrates

Fig. 29: Benchmark of the present n-channel TFET performance in terms of I_{on}/I_{off} ratio versus the minimum S.S. value with other reported ones [18-20, 243, 248-254] with a variety of channel materials

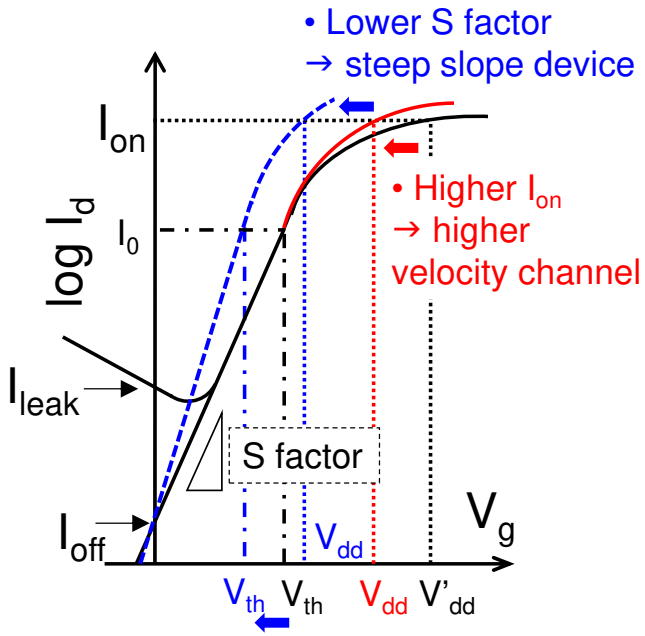


Fig. 1 (S. Takagi)

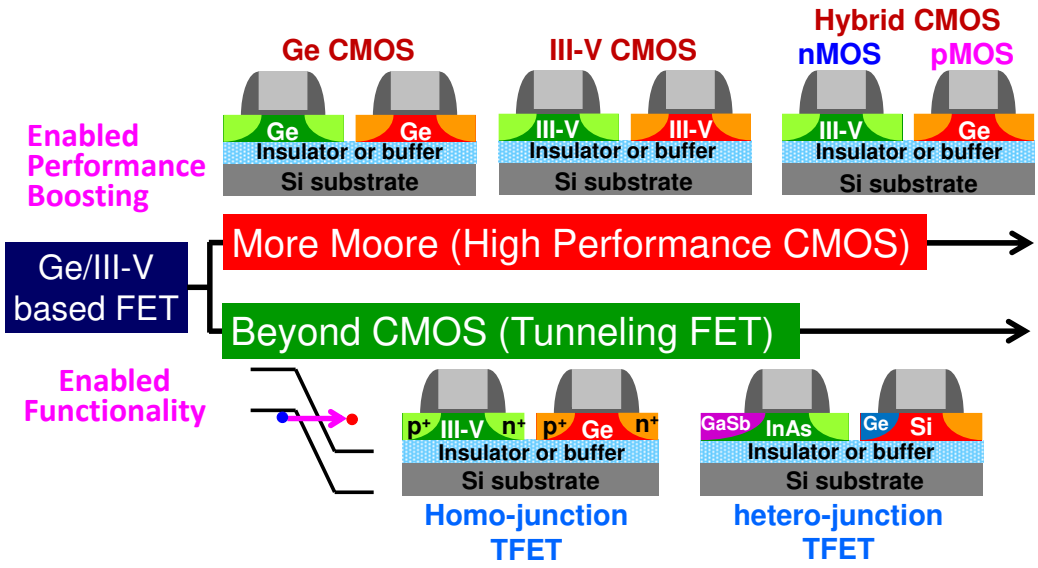


Fig. 2 (S. Takagi)

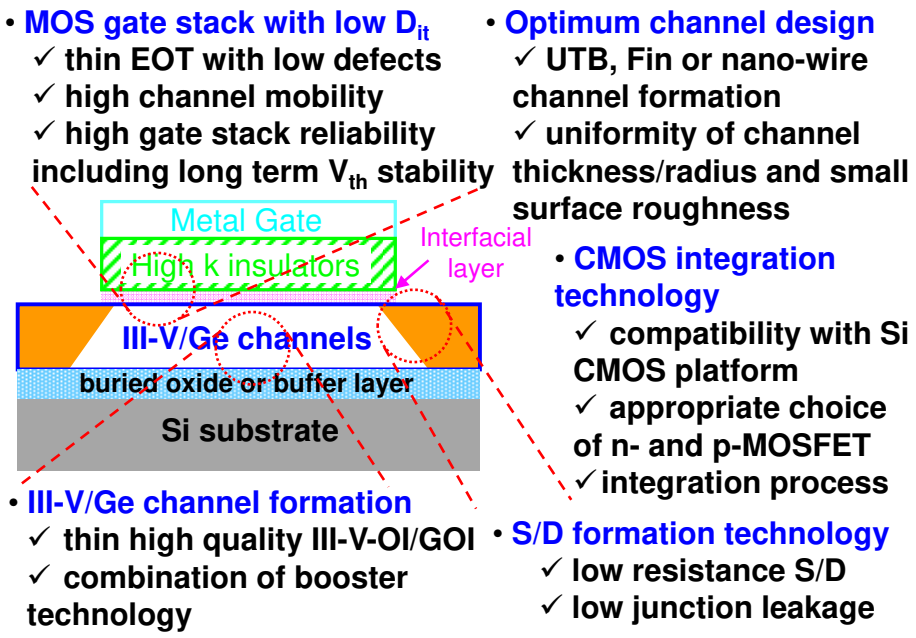
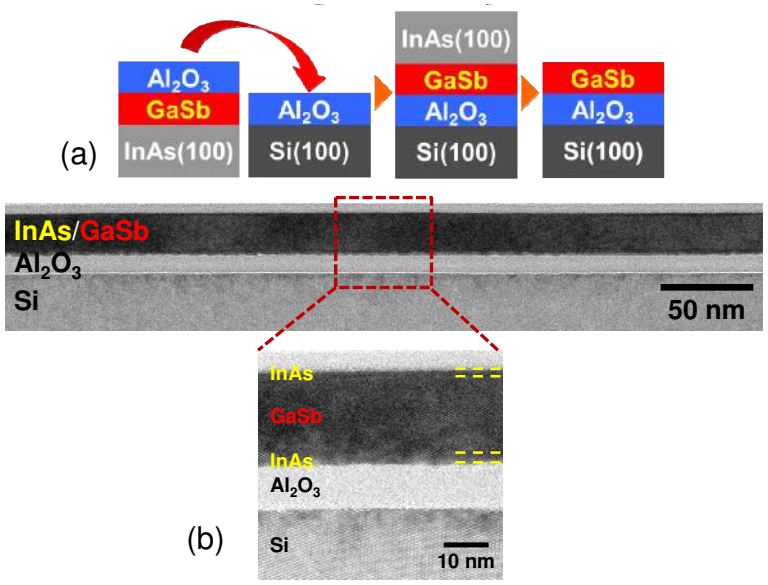


Fig. 3 (S. Takagi)



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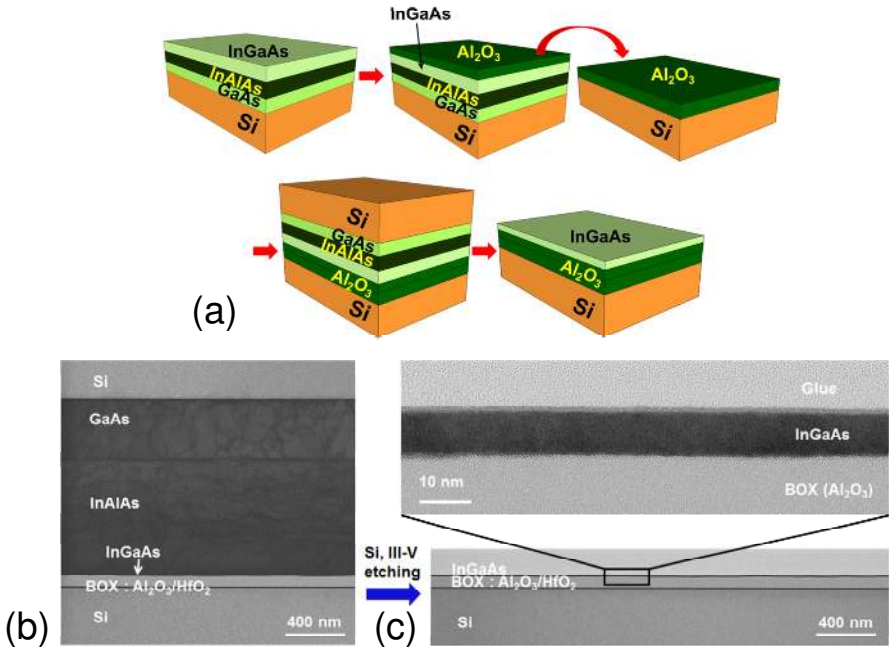


Fig. 5 (S. Takagi)

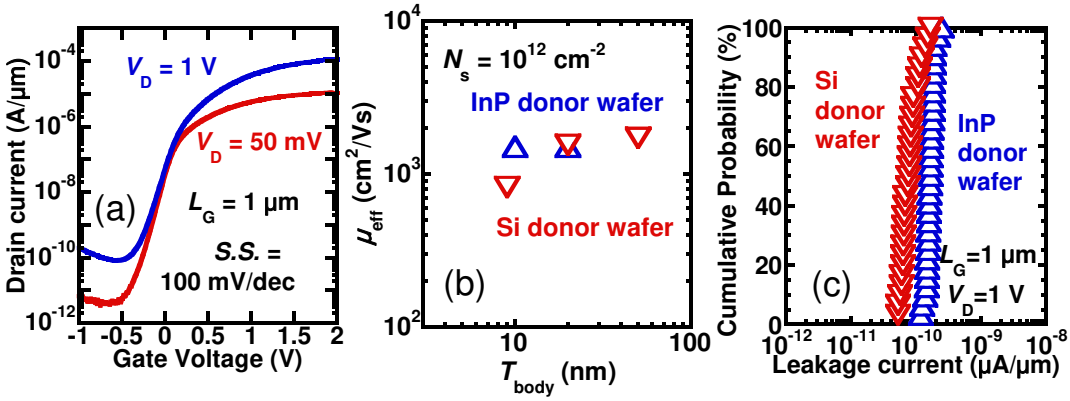


Fig. 6 (S. Takagi)

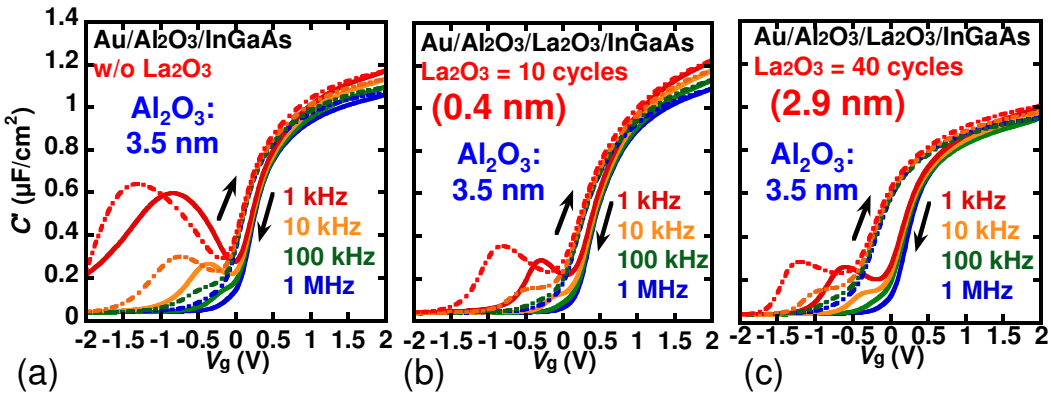


Fig. 7 (S. Takagi)

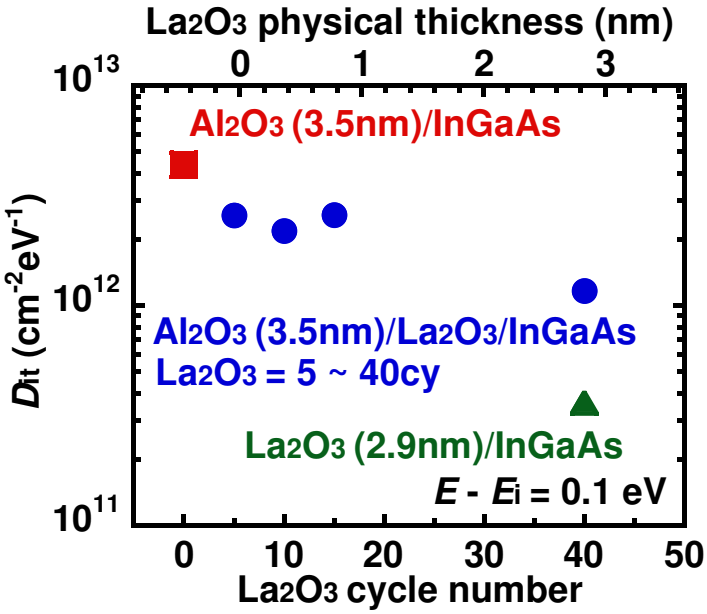


Fig. 8 (S. Takagi)

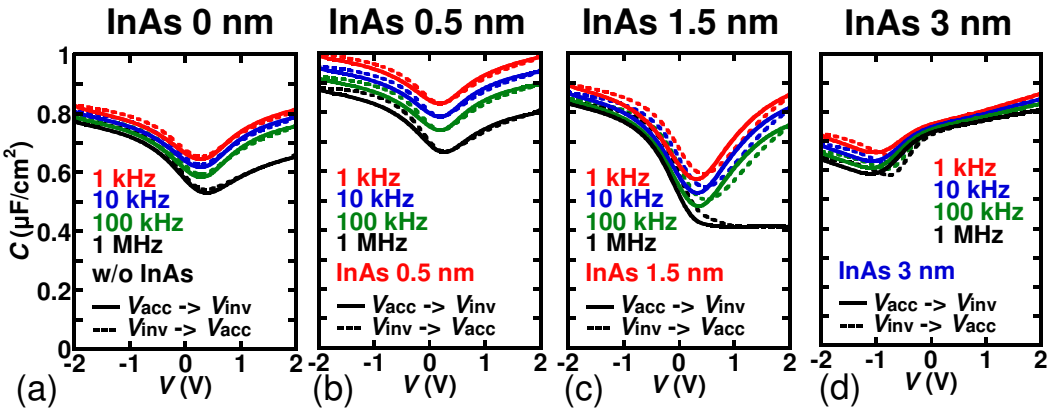


Fig. 9 (S. Takagi)

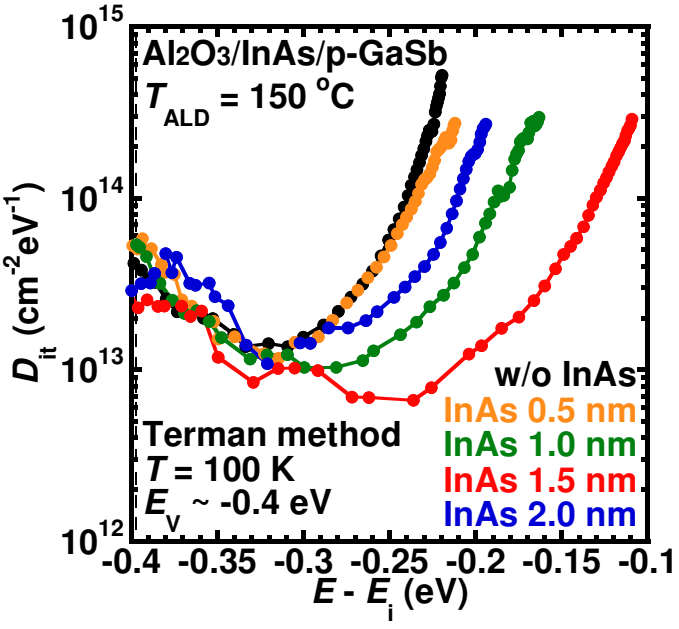


Fig. 10 (S. Takagi)

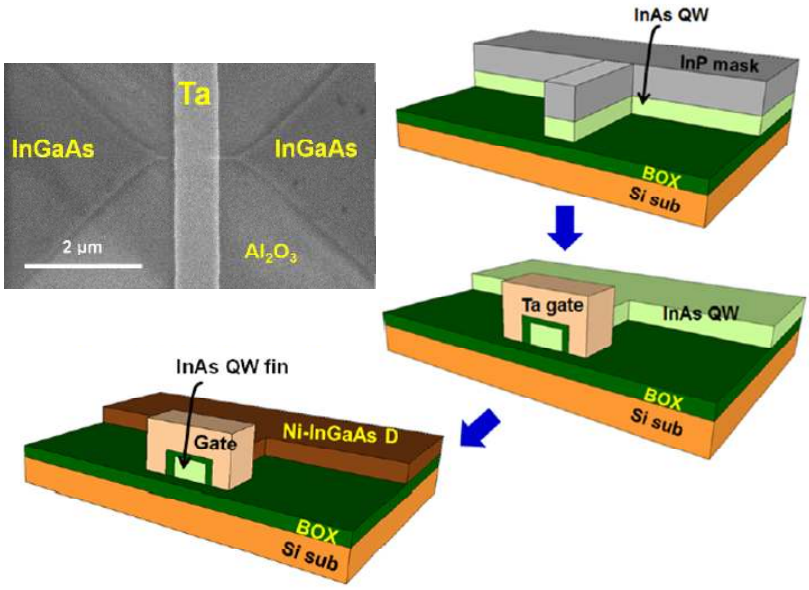


Fig. 11 (S. Takagi)

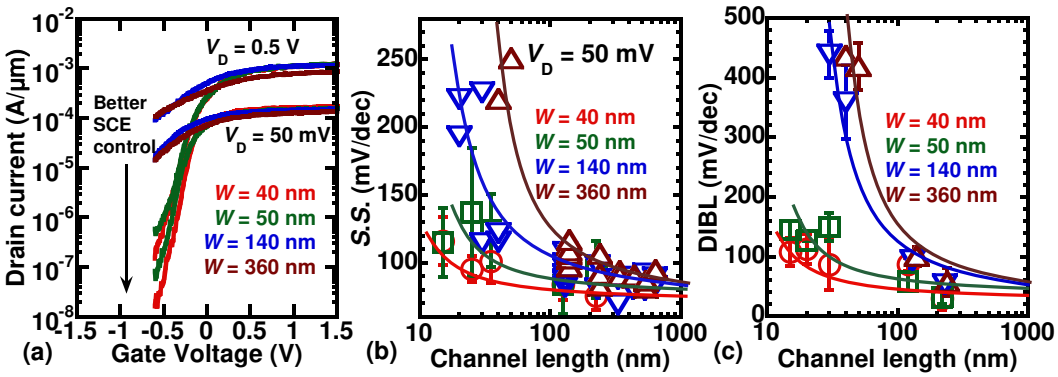
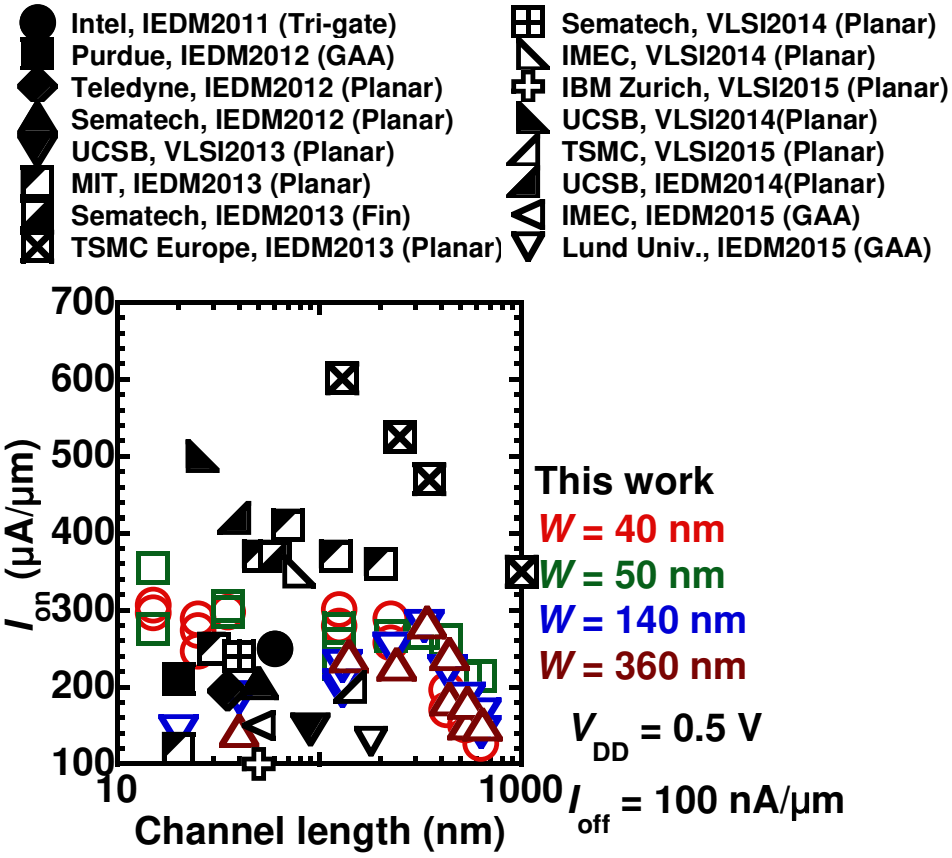


Fig. 12 (S. Takagi)



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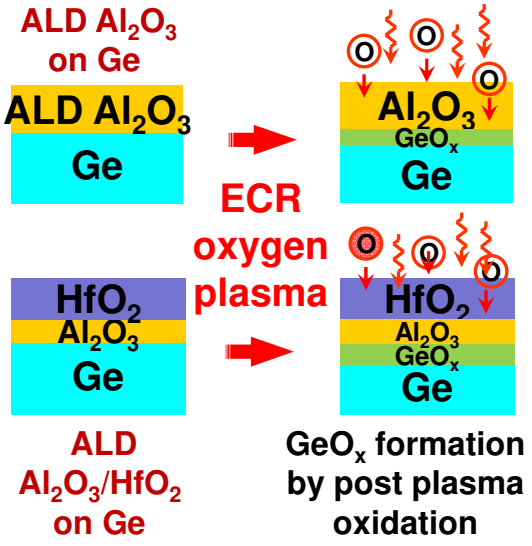

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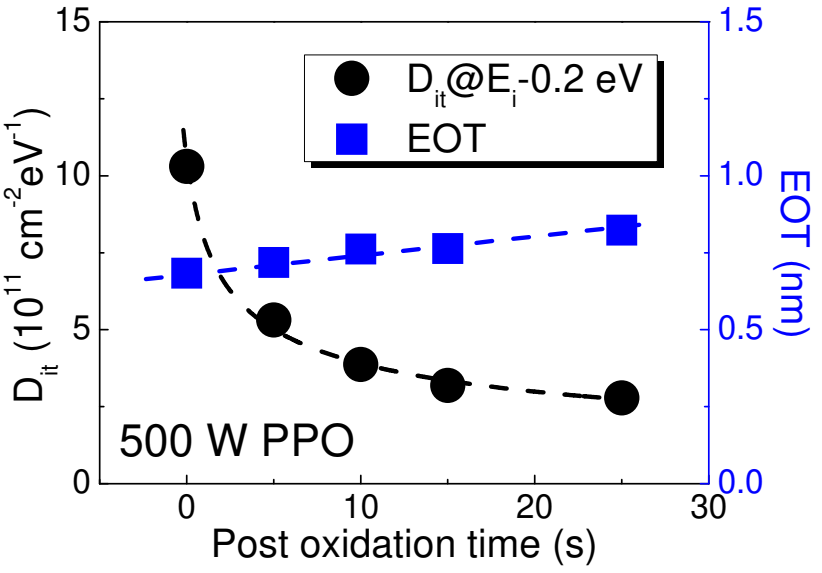

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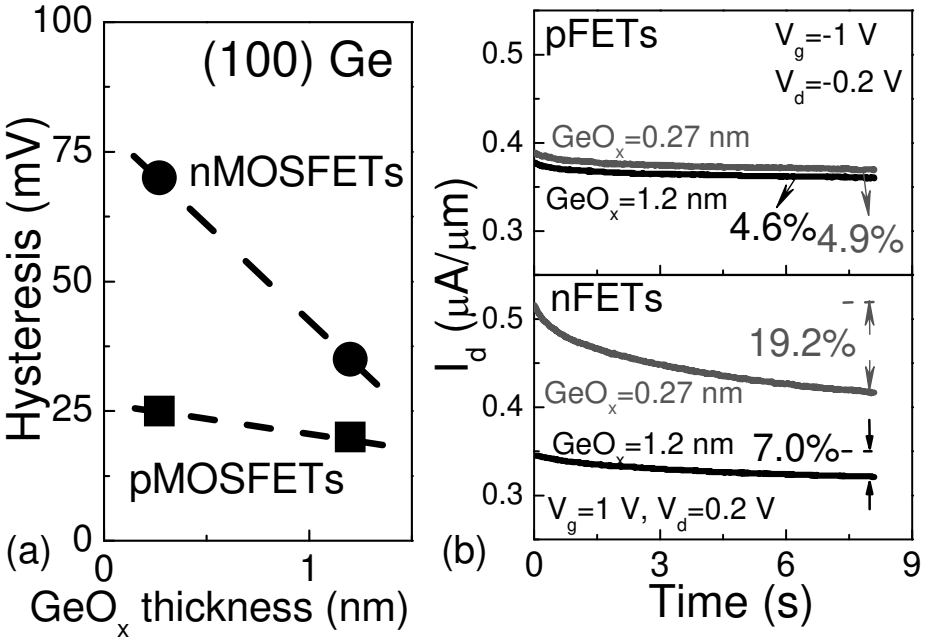

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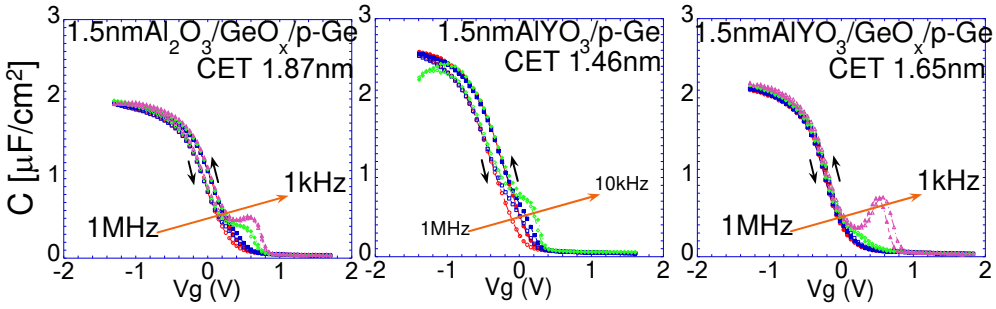
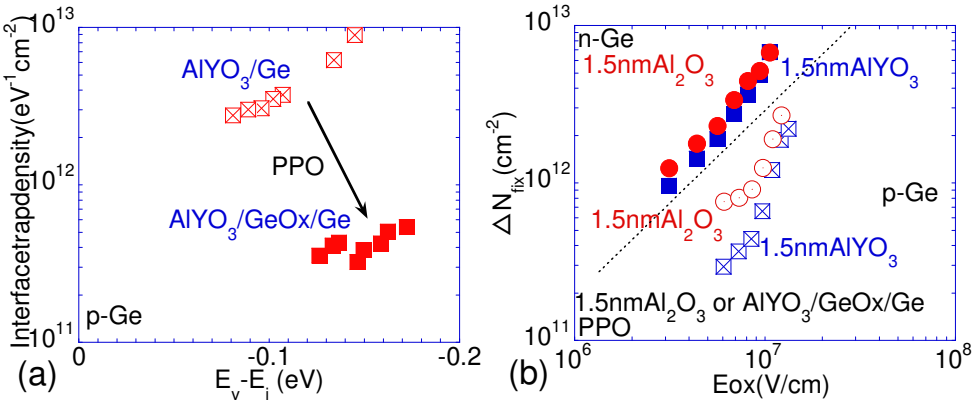


Fig. 17 (S. Takagi)



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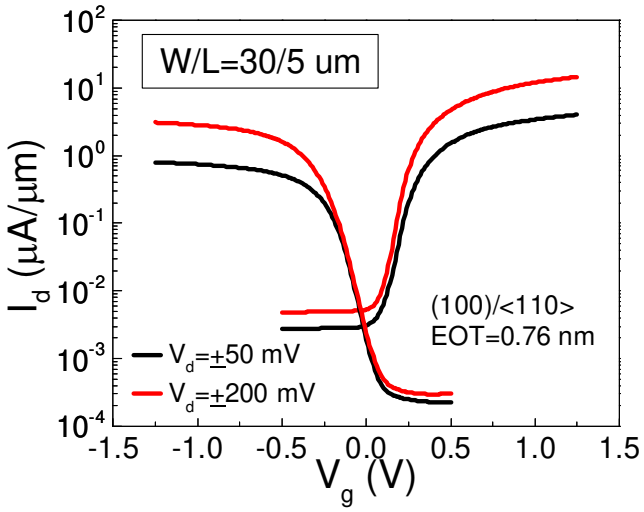

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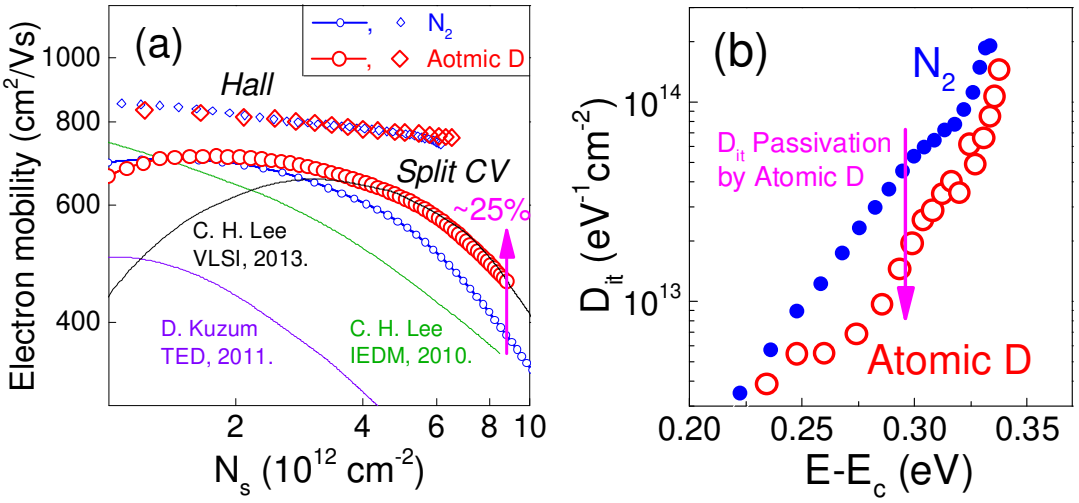

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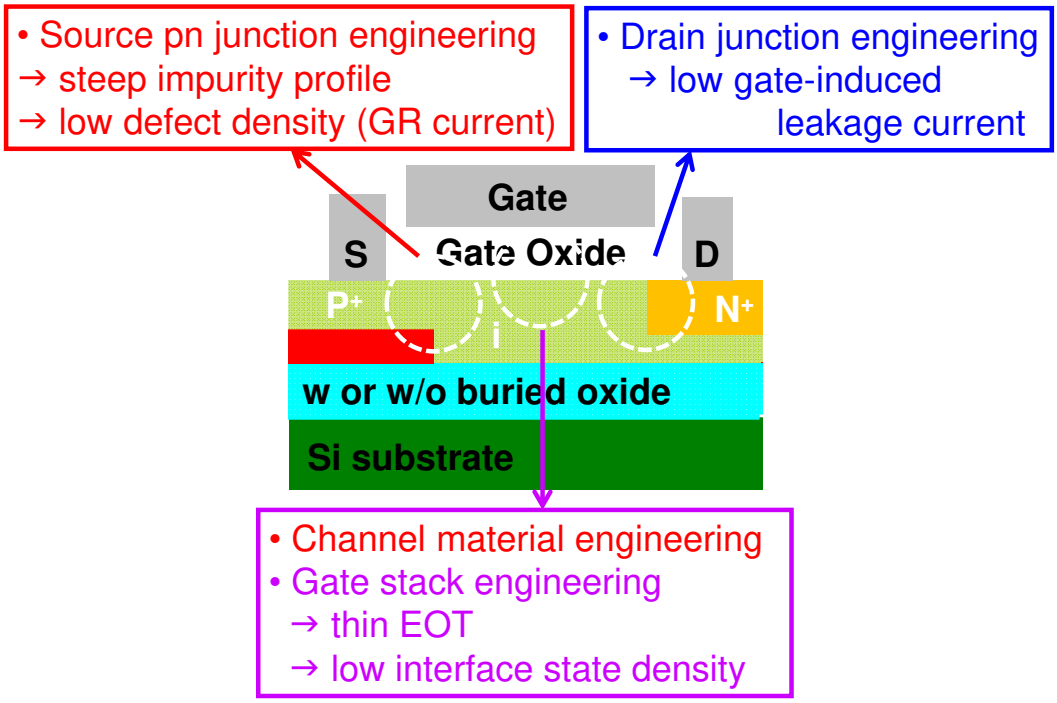

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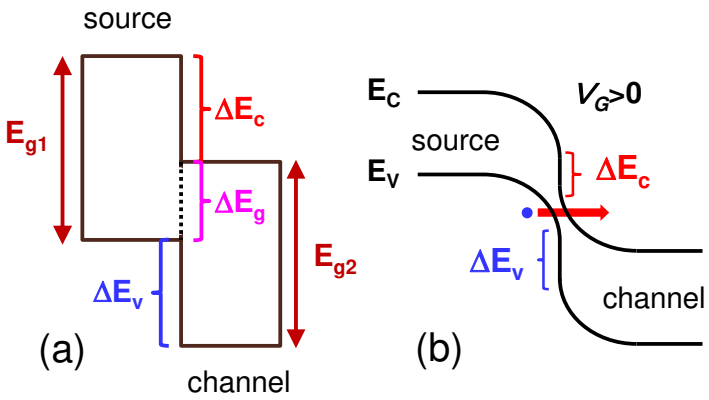

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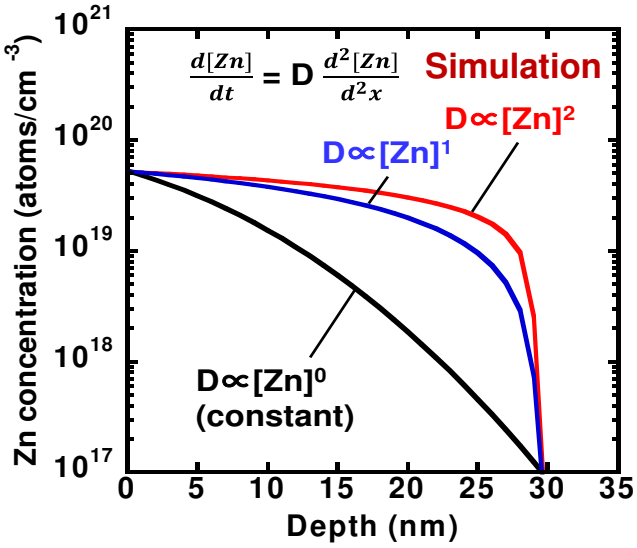

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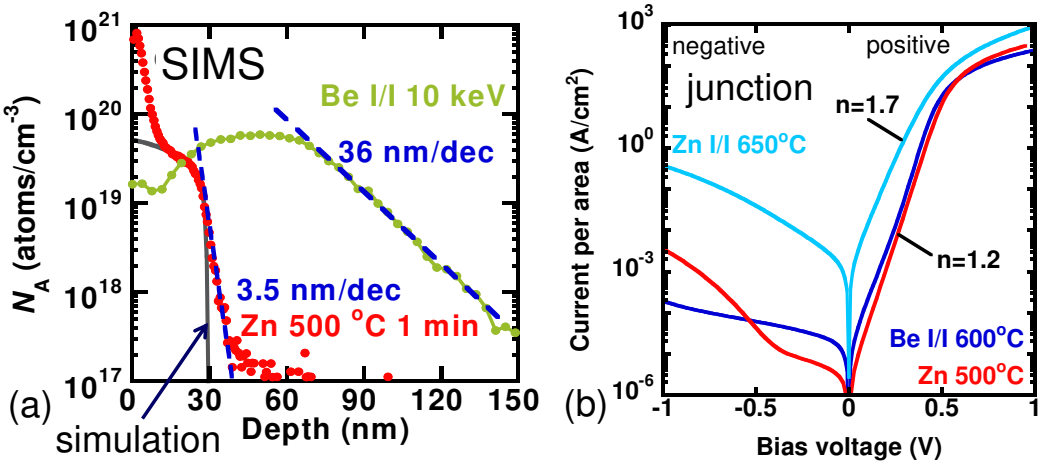

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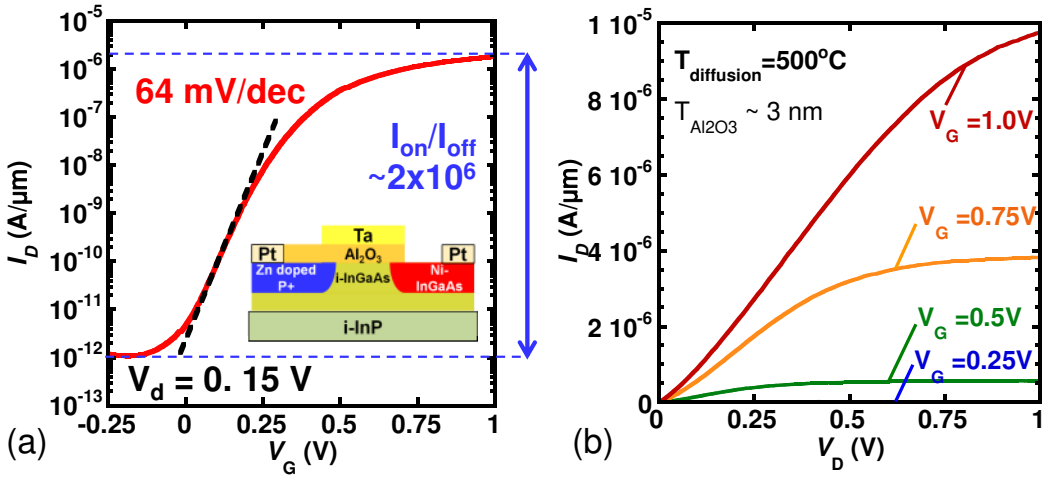

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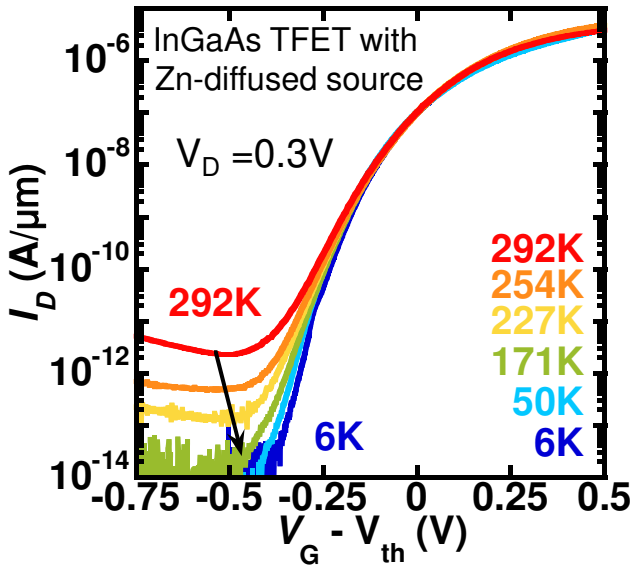

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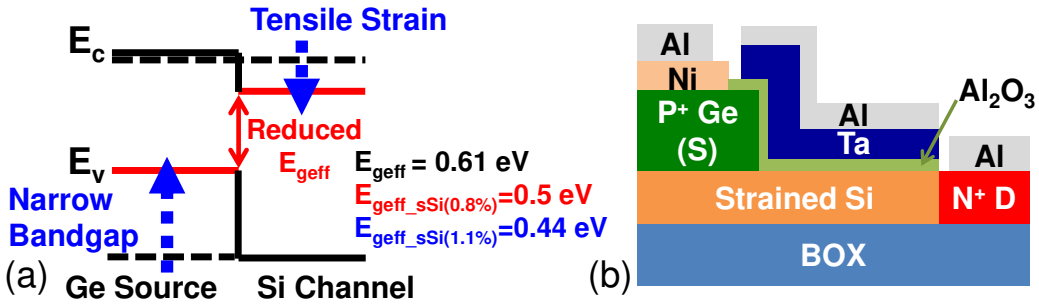

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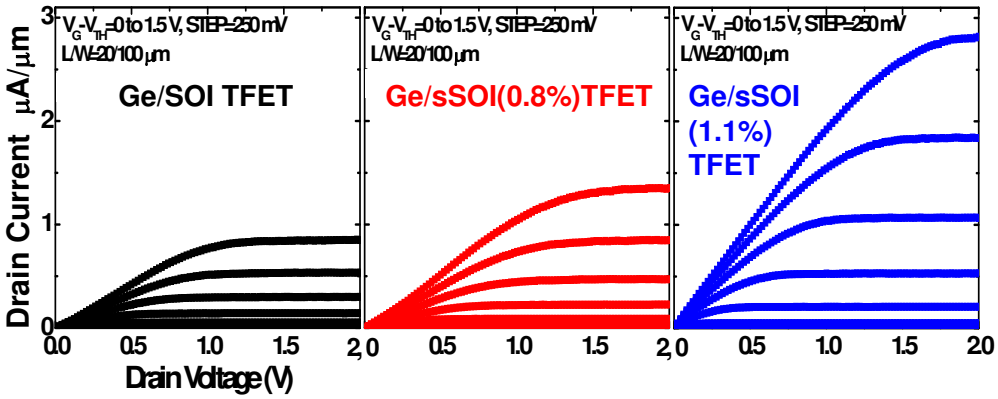

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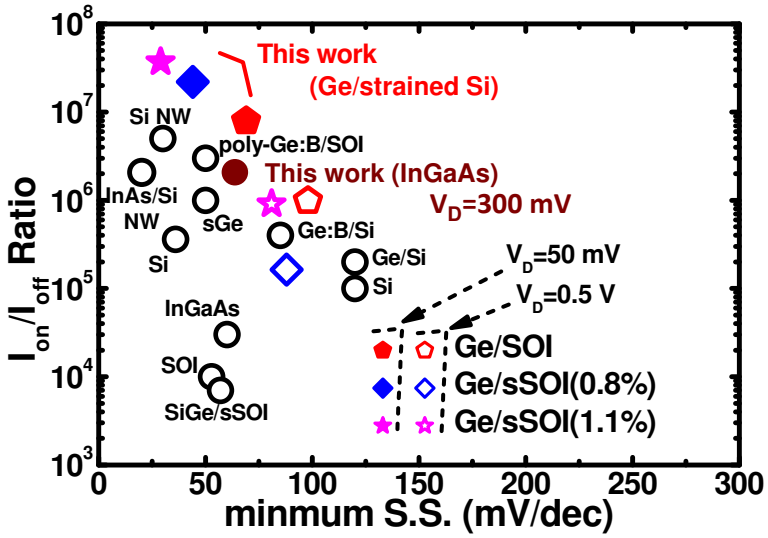

Fig. 29 (S. Takagi)