III-V-on-nothing metal-oxide-semiconductor field-effect transistors enabled by top-down nanowire release process: Experiment and simulation

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III-V-on-nothing (III-VON) metal-oxide-semiconductor field-effect transistors (MOSFETs) are experimentally demonstrated with $In_{0.53}Ga_{0.47}As$ as channel and atomic layer deposited Al_2O_3 as gate dielectric. A hydrochloric acid based release process has been developed to create an air gap beneath the InGaAs channel layer, forming the nanowire channel with width down to 40 nm. III-VON MOSFETs with channel lengths down to 50 nm are fabricated and show promising improvement in drain-induced barrier lowering, due to suppressed short-channel effects. The top-down processing technique provides a viable pathway towards fully gate-all-around III-V MOSFETs. © *2011 American Institute of Physics*. [doi:10.1063/1.3638474]

Recently, encouraging progress has been made on the understanding and improvement of oxide/III-V interfaces. As a result, high performance surface channel inversion-mode InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) with large current drivability have been demonstrated[1–7] and are considered as a strong candidate to replace conventional Si MOSFET at beyond 14 nm technology node. Besides the numerous efforts spent on reducing the interface trap density at the oxide/InGaAs interface, another major challenge of realizing an InGaAs MOSFET in the deep-submicron regime is the effective control of short channel effects (SCE).[8–10] Very recently, Intel has announced that 3-dimensional (3D) tri-gate transistors would be introduced at 22 nm technology node on Si complementary metal-oxide-semiconductor (CMOS) manufacturing. Due to the inherently lower bandgap and larger permittivity of III-V materials, III-V MOSFETs are more susceptible to SCE, making 3D structure a must for III-V logic applications. In fact, InGaAs fin field-effect transistors (FinFETs) (Refs. 11 and 12) as well as multiple gate InGaAs quantum well transistors[13] have been demonstrated, showing improved SCE control by 3D device structure. Further suppression of SCE requires more advanced device architecture that can offer a better gate electrostatic control. Silicon on nothing (SON) MOSFETs have been proposed[14] and experimentally demonstrated,[15] providing a solution for quasi-total suppression of SCE and drain induce barrier lowering (DIBL) with gate length down to 30 nm. The key fabrication processes for SON MOSFETs involve selective removal of the SiGe layer and formation of an air tunnel underneath the Si channel. Similarly, a SON counterpart on the III-V platform, namely III-V on nothing (III-VON), can also be realized if a selective etching process is developed to form an air gap underneath the III-V channel.

In this letter, we report the experimental demonstration of III-VON MOSFETs with $In_{0.53}Ga_{0.47}As$ as the channel and atomic-layer-deposited (ALD) Al_2O_3 as the gate dielectric. The key fabrication has been enabled by well-controlled hydrochloric acid (HCl) based selective etching of InP over InGaAs. It is found that the InGaAs fins have to be patterned along [010] direction in order to achieve a channel release process, owing to the anisotropy of InP wet etching. III-VON MOSFETs with channel length (L_{ch}) down to 50 nm and fin width down to 40 nm were fabricated. A low DIBL of 45 mV/V at 50 nm gate length is observed experimentally, which is consistent with the numerical simulation results from 3D Synopsys Sentaurus Technology Computer-Aided Design (TCAD). This shows that the III-VON structure is effective at suppressing the SCE of III-V MOSFETs down to at least $L_{ch} = 50$ nm.

MOSFET fabrication started with a 2 in. p+ InP wafer. A 30 nm $In_{0.53}Ga_{0.47}As$ layer with p-doping of 2×10^{16} cm^{-3} was grown on InP substrate by molecular beam epitaxy as the channel layer. After surface treatment with NH_4OH solution, a 10 nm Al_2O_3 was grown by ALD as an encapsulation layer. Source/drain regions were then defined and Si ion implantation at energy of 20 keV and dose of 1×10^{14} cm^{-2} was performed. The shortest L_{ch} 50 nm was defined by the separation between source and drain regions. The metal gates were designed to be 50 nm longer than the L_{ch} with 25 nm extension on each side due to the non-self-aligned process. Dopant activation was done using rapid thermal annealing at 600 °C for 15 s in nitrogen ambient.[9,10] Next, the InGaAs fins were patterned along [010] direction as shown in Figure 1(a), using diluted ZEP520A electron-beam resist with a thickness of 200 nm. The fin etching was performed with BCl_3/Ar gas using a Panasonic high density plasma etcher.[11] After removing the resist, the sample was treated sequentially with diluted buffered oxide etch (BOE) and diluted mixture of HCl and hydrogen peroxide (H_2O_2). Then the channel release process was performed using HCl:H_2O (1:2) solution. It is known that HCl based solution has high selectivity between InP and InGaAs. However, the InP etching is found to be highly anisotropic, and undercut etching is only possible along $\langle 100 \rangle$ directions.[16] Test fin structures along [011], [010], and [01$\bar{1}$] were patterned, followed by etching in diluted HCl. For different fin patterning directions, the

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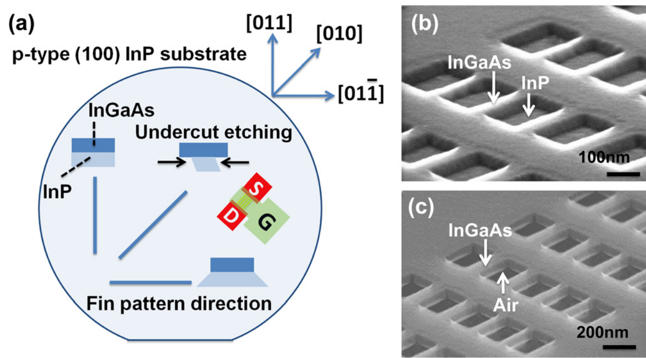

FIG. 1. (Color online) (a) Schematic diagram of fin patterning direction, release etching profile, and device alignment to the substrate. (b) Tilted SEM image of fin test structures after fin dry etching and before wire release. (c) Tilted SEM image of fin testing structures after wire release.

etching profile varies as depicted in Figure 1(a). This is also confirmed in Ref. 17 where different emitter mesa surfaces were revealed for different emitter electrode orientations. Figures 1(b) and 1(c) show the tilted scanning electron microscopy (SEM) images for fin test structures before and after channel release process, respectively, where undercut etching was demonstrated. Patterning the fin along ⟨100⟩ directions is the key to realize the III-V channel release at the deep sub-micron scale. After channel release, a 5 nm Al_2O_3 was regrown using ALD as the gate dielectric. Note that for the purpose of process demonstration, no pre-gate surface passivation such as $(NH_4)_2S$ treatment was carried out here. The gate structure was formed by electron beam evaporation of Ni/Au and liftoff process. Due to the vertical directionality of the evaporation, the air gap naturally remains underneath the channel. Au/Ge/Ni source/drain metal was then evaporated and annealed at 350 °C in nitrogen ambient. Finally, test pads were deposited which concluded the fabrication processes. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system.

Figure 2(a) shows the schematic diagram of a finished III-VON device from a bird's eye view. Figures 2(b) and 2(c) depict the schematic cross section of the device in the y-z plane and the x-z plane, respectively. The fin height

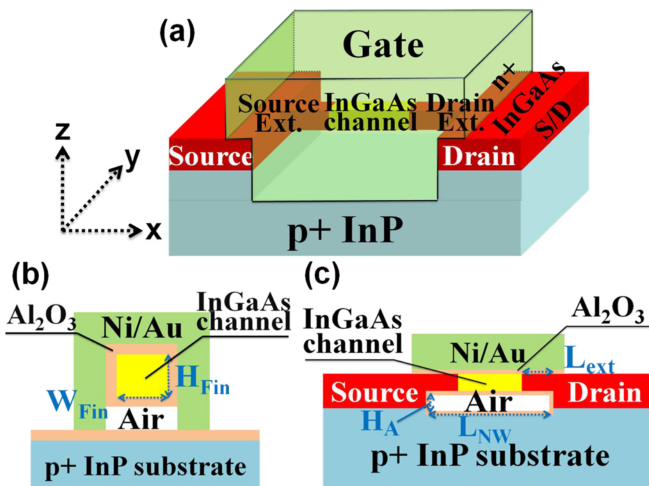

FIG. 2. (Color online) (a) Schematic diagram of a III-VON MOSFET with $In_{0.53}Ga_{0.47}As$ channel and Al_2O_3 gate dielectric from a bird's eye view. (b) Cross sectional view of a III-VON MOSFET in x-y plane. (c) Cross sectional view of a III-VON MOSFET in x-z plane.

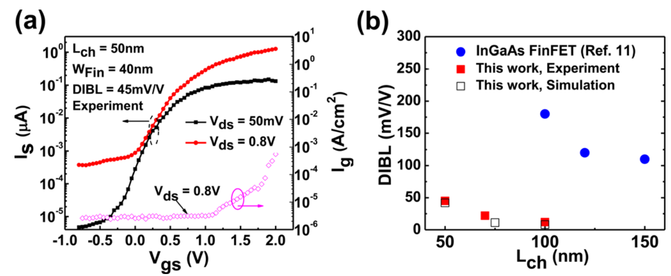

FIG. 3. (Color online) (a) Source current (left) and gate current (right) versus gate voltage for a L_{ch} = 50 nm III-VON MOSFET with W_{Fin} of 40 nm. (b) DIBL versus L_{ch} for III-VON MOSFETs from experiment (square) and simulation (hollow square) compared to that of InGaAs FinFET (circle).

(H_{Fin} = 30 nm) is determined by the initial InGaAs layer thickness. The smallest fin width (W_{Fin}) achieved is 40 nm. The nanowire length (L_{NW}) in this work is fixed at 300 nm, yielding a source/drain extension length (L_{ext}) of around 125 nm for a 50 nm L_{ch} device. The smallest air gap height (H_A) is around 40 nm, controlled by the release etching time. The L_{ch} of the devices vary from 100 nm down to 50 nm. Figure 3(a) shows the transfer characteristic and gate leakage current versus gate voltage of a typical III-VON MOSFET with L_{ch} of 50 nm, W_{Fin} of 40 nm, and four wires in parallel. To better evaluate the intrinsic device performance, source current is used to eliminate the effect from non-ideal source/drain junction leakage current. The device operates in enhancement mode, with a threshold voltage of 0.36 V from linear extrapolation at a drain voltage of 50 mV. A low DIBL of 45 mV/V is obtained at the shortest gate length of 50 nm, thanks to the III-VON structure. As a comparison, a 100 nm channel length InGaAs FinFET has a DIBL of around 180 mV/V.[11] The subthreshold swing (SS) is found to be around 200 mV/dec, indicating relatively large interface trap density (D_{it}). Surface treatment before the formation of ALD Al_2O_3 gate dielectric which could have improved the D_{it} was not performed since that was not our main purpose in this study. Gate leakage current at V_{ds} = 0.8 V is similar to that in Ref. 11 and stays very low at gate voltage less than 1 V. The saturation current at a drain voltage of 1.6 V and a gate voltage of 2 V reaches 10 μA/μm, normalized by the total width of the gated region, i.e., $W_G = 2 \times H_{Fin} + W_{Fin}$. The current can be further improved by applying $(NH_4)_2S$ pre-gate treatment[18] and reducing source/drain series resistance.

3D TCAD simulation was performed using Synopsys Sentaurus.[19] Device structures were created according to the experimental parameters, i.e., W_{Fin} = 40 nm, H_{Fin} = 30 nm, etc. The poisson equation, electron and hole continuity equations were solved using a coupled solver at each mesh node to obtain various output parameters such as potential, electric field, electron and hole densities, etc. No interface traps were incorporated in the simulation. From the simulated transfer characteristics, DIBL was extracted and compared with the experimental data as shown in Figure 3(b). The experimental data agree well with the simulation results. Moreover, the DIBL obtained from InGaAs FinFETs in Ref. 11 is also plotted in the same figure. The III-VON structure shows significant improvement in DIBL reduction, confirming that the more advanced 3D structures are beneficial for the suppression of the SCE.

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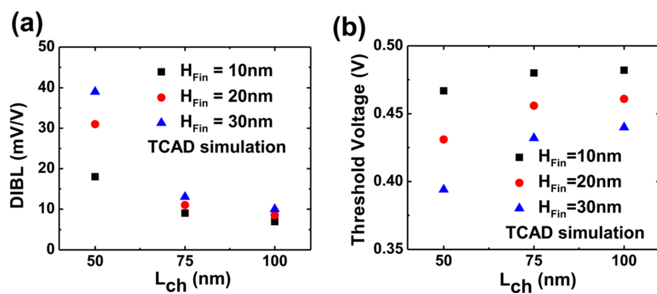

FIG. 4. (Color online) (a) DIBL versus L_{ch} for III-VON MOSFETs with different H_{Fin} from TCAD simulation. (b) Threshold voltage roll-off property of III-VON MOSFETs with different H_{Fin} from TCAD simulation.

Finally, the effect of channel layer thickness (H_{Fin}) and source/drain extension length (L_{ext}) on the device performance were simulated. H_{Fin} was varied from 30 nm down to 10 nm. Figures 4(a) and 4(b) show the DIBL and saturation threshold voltage as a function of channel length with different H_{Fin}. Smaller H_{Fin} reduces DIBL and improves the threshold voltage roll-off property, due to a better gate electrostatic control of the channel. Devices with different L_{ext} of 10 nm, 50 nm, and 125 nm were also simulated. The results show a clear trade-off between on-current and DIBL. By increasing the extension length, DIBL is reduced while the on-current drops, due to the increase in source/drain resistance. A 2× higher on-current is expected when L_{ext} is reduced from 125 nm to 10 nm, while DIBL increases by 30%. These simulation results provide a guideline for future experimental work.

In conclusion, III-VON MOSFETs are experimentally demonstrated. A HCl based release process has been developed to enable air gap formation beneath the InGaAs channel. A typical 50 nm gate length device shows a low DIBL of 45 mV/V, consistent with the results from TCAD simulation. The significant improvement in DIBL compared to the previous InGaAs FinFETs demonstrates better immunity to SCE using the III-VON architecture. This top-down process provides a viable pathway to realize gate-all-around (GAA) III-V MOSFETs which should show even better electrostatic control of the channel.[20]

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