III–V-on-Si Photonic Crystal nanocavity laser technology for optical Random Access Memories (RAMs)

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Abstract—**Heterogeneous integration of III-V semiconductors on silicon has gained considerable momentum fueled by the need to implement fully functional photonic devices and circuits in a CMOS compatible platform. In this communication, we report on a III-V photonic crystal (PhC) nanocavity, heterogeneously integrated on a Silicon-on-Insulator (SOI) platform, to form a PhC nanocavity laser capable of exhibiting two elementary RAM cell functions individually, namely switching and latching operations under a high-speed, bit-level regime. As such, the PhC nanocavity laser is examined as a generic logic functions building block, suitable towards multi-Gb/s energy-efficient, optical Random Access Memory (RAM) cells with minimal footprint. The proposed device active layer is a nanobeam cavity of 650nm×285nm InP-based wire waveguide, allowing for a record-low footprint of only 6.2µm² among integrated optical memories so far presented. Bit-level RAM cell operation requires two elementary functions: the Access Gate (AG) switching function and Set-Reset Flip-Flop (SR-FF) latching function. At first, AG switching operation is evaluated through successful Wavelength Conversion (WC) at 10Gb/s, revealing a power penalty of 1dB at 10^{-9} BER and a switching energy of only 4.8fJ/bit. Then, fully functional SR-FF memory operation is successfully demonstrated, exhibiting error-free operation with negative power penalty at 5Gb/s and switching energies of 6.4fJ/bit. Flip-Flop operation at higher speeds of 10Gb/s with reduced switching energy levels of 3.2fJ/bit is also experimentally investigated. Both logic operations were demonstrated separately with the same PhC nanocavity laser device exhibiting <50ps switching times and evaluated under real-type data traffic patterns, raising expectations for beyond 20Gb/s capabilities towards implementing energy-efficient, ultra-compact and high-speed true optical RAM setups.**

Index Terms— **Optical memories, Photonic Crystal nanocavity laser, Access Gate, Wavelength Conversion, Optical Flip Flop**

I. INTRODUCTION

Silicon photonics have enabled the penetration of optical technology to the computing environment, starting from optical interconnection for rack-to-rack and board-level communications [1] towards photonic-electronic co-integration [2]-[4] and on-chip processing [5],[6]. Furthermore, recent progress on InP-on-Si integration technology has revealed great potential in developing novel photonic devices [7], [8] with advanced functionalities as heterogeneous integration of III-V semiconductors on silicon enables the fabrication of optically active devices on a CMOS-compatible platform, raising expectations for an even more powerful photonic integration technology platform. Such advanced photonic devices that would exhibit unique performance in terms of energy efficiency, high bandwidth and large scale integration capabilities could be employed in the near future to address demanding on-chip processing applications and tackle long-lasting problems in computing [9] towards enabling novel architectures [10] that can radically reform the shape of computer science.

One demanding application could be the alleviation of Von Neumann bottleneck, also known as the Memory Wall problem [9]. The root cause of this problem [9] extends along two primary bottlenecks degrading the overall system performance: the long access time of both static and dynamic electronic Random Access Memories (SRAMs and DRAMs, respectively) and the limited bandwidth of the processor-main memory electrical bus. Towards addressing the limited bandwidth problem of electrical bus, optically interconnected CPU-memory paradigms have been demonstrated, indicating that future processor-main memory systems can leverage optics to increase bandwidth through data parallelism [11]-[13]. On the other hand, the long access times of electronic SRAM circuitry will still persist even though optical bus solutions come at the foreground. Towards removing also this bottleneck, high-speed bit-level memory units are required. Recent advances in Chip-Multiprocessors (CMP) technology and the extensive use of parallelism[14],[15] have resulted in further enhancing the Von Neumann problem, as electronic RAMs have proved incapable to keep up with the required Read/Write memory access speeds [9] and their operational capabilities do not exceed 4.6GHz [16]. Today, the deployment of large two- or even three-level on chip cache memory hierarchies to ease

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the limited off-chip bandwidth and the high main memory's response latency introduces new challenges as on-chip caches take up almost 40% of the total chip energy consumption [17] and more than 40% of chip real-estate [18] without contributing to main job of the CPU chip (i.e. processing).

Facing these problems, all-optical memory technology could be the drastic answer, not only due to its inherent advantage of offering faster response times and thus covering the need for significantly improved memory speeds and access times, but also because it would allow for better interconnection links directly in the optical domain. In this way, the critical latency sensitive memory-processor path could reap the benefits of optical interconnection including Wavelength Division Multiplexing (WDM) increased bandwidth and minimal transmission time. Such an alternative approach was recently proposed [19], suggesting the exploitation of both optical interconnect technology together with all-optical bit-level memory configurations towards an off-chip, high-speed optical cache memory architecture. This work [19] revealed that a performance speed-up of up to 40% can be achieved reducing at the same time the total cache capacity requirements by 84% for a certain benchmarking suite, indicating in this way that the use of all-optical memories can be the alternative way to relax the Von Neumann bottleneck.

In the way towards practical all-optical memories, a rich body of research activity has been reported [20]-[24] and several technologies have been pursued to deliver light-based storage, including polarization bistable VCSELs [20], integrated InP ring-lasers on SOI relying on light direction bistability [21], coupled laser-based [22] and switch-based [23],[24] "master-slave" configurations. Within this frame, photonic crystal (PhC) nanocavities have drawn significant attention due to their capabilities of delivering high integration densities together with increased energy efficiency compared to previous integrated optical memory demonstrations[20]-[24]. Optical memory devices based on PhC nanocavities have already been presented utilizing the InGaAsP/InP platform and relying on the bistability of PhC nanocavity lasers [25] with 60ps switching times at 70μW of switching power. Moreover, optical memory devices based on the bistability of InGaAsP/InP PhC switches [25]-[28] have been demonstrated requiring a switching energy of 13fJ/bit while exhibiting ~10μm^2 footprint [26]. The energy and footprint benefits come, however, at the cost of a slower fall time of 7.4ns rendering these optical memory implementations more suitable for buffering schemes in routing applications rather than for bit-level high-speed caching in computing environments.

Even more, the realization of radically new all-optical memory architectural schemes in large-scale configurations requires a complete toolbox for the optical memory technology that extends simple latching/ Flip-Flop operation towards full-scale functional RAM memories. To highlight this, Fig. 1a) shows a typical two dimensional (2D) layout of 4×4 RAM bank [29] along with the peripheral circuits (i.e. Row/Column decoders) [30][31] that are usually required in such advanced implementations. As it can be seen, the RAM bank consists of 16 separate single RAM cells that not only implement the storing functionality, but they are also independently controlled by Access Signals to allow access to a specific single row for
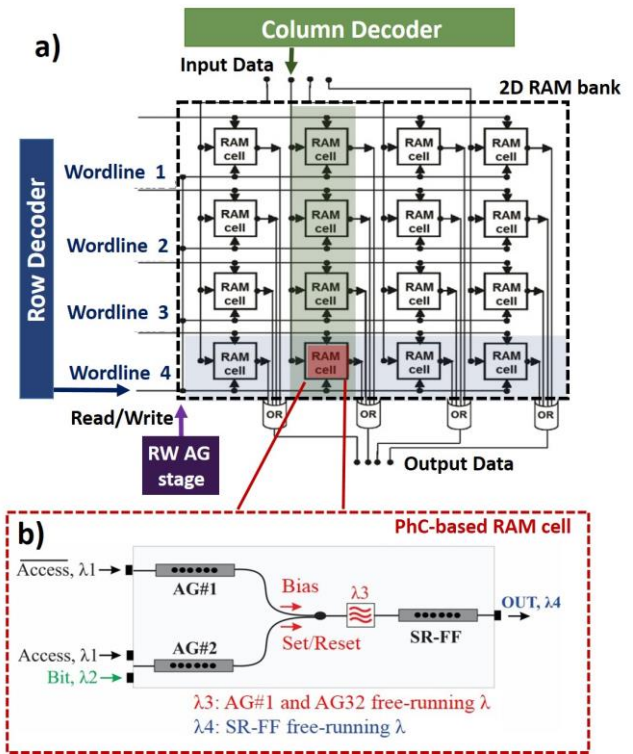

Fig. 1: a) 4×4 Optical RAM bank layout with peripheral circuits and b) PhC-based RAM cell architecture where two PhC-based nanocavity lasers perform as the AGs and a single PhC-based nanocavity laser acts as the FF memory.

storing/retrieving a 4-bit word. This means that in order to build an independent optical RAM cell that can be accessed to perform Read/Write functionalities, a Flip-Flop (FF) latching mechanism serving as the storage unit has to be combined with two additional Access Gate (AG) elements that control the access of the incoming Bit sequences to the memory cell. On a RAM cell basis, as depicted in Fig.1b), Read operation is performed when the Access signal's logical state is one and no incoming Bit sequences are injected into the RAM cell. This allows only Bias pulses to enter the RAM cell to preserve its memory content. On the other hand, Write operation is performed when Access signal is logical zero, allowing Set/Reset pulses to change the memory state.

Although numerous optical FF implementations have been already reported, only a few demonstrations have addressed true all-optical static RAM cells implementations with Read/Write control by external Access signals [29],[32]. All these demonstrations managed to exhibit isolated performance or integration benefits but did not succeed so far to comply with all the demanding requirements (i.e. footprint, energy efficiency and high-speed operation at real data-traffic environments), simultaneously.

On the other hand, an InP-on-Si nanocavity configuration has been presented to perform high-speed Wavelength Conversion (WC) operation [36] while very recently we employed an InP-on-Silicon photonic crystal nanocavity laser to demonstrate Flip-Flop and WC principle of operation at 5Gb/s [37], [38]. This effort has revealed that the InP-on-Si PhC nanocavity laser technology holds great potential for providing a generic component capable to implement a functional RAM cell that combines all desired characteristics in terms of speed, footprint and power consumption. Such a PhC-based RAM cell concept

is illustrated in Fig.1b) where two PhC components serve as the AG elements and one PhC-based nanocavity laser is employed as the SR-FF. As it will be explained in Section III, the PhC-based SR-FF requires a three-level input signal (λ2) with highest and lowest power level representing the Set, Reset pulses, respectively, while the middle power level acts as the Bias pulses retaining the previous memory content. As can be observed in Fig. 1b) the first PhC-based AG (AG #1) is responsible for allowing/blocking the Set/Reset signals whereas the second AG (AG#2) creates the necessary Bias signal to the SR-FF memory unit.

In this paper, we report on a hybrid III-V on Si PhC-based nanocavity laser device capable to perform both fundamental logic functionalities, such as switching and latching, providing a generic building block towards implementing fully functional optical RAM cells with minimal footprint, enhanced energy efficiency and high-speed bit-level operation for real data-traffic computing environments. On that account, we introduce a novel RAM cell achitecture allowing memory control with Access signals, based explicitly on the PhC nanocavity laser device, and we evaluate separately combinational (AG) and sequential (SR-FF) operations of the proposed PhC nanocavity laser, required for the RAM cell configuration. The AG capability of the PhC nanocavity laser SR-FF was confirmed by successful Wavelength Conversion (WC) operation at 10Gb/s with $2^{31}-1$ PRBS signals, revealing an Extinction Ratio (ER) value of 10dB, at switching energies as low as of 4.8fJ/bit with a power penalty of 1dB. The SR-FF operation of the PhC nanocavity laser was verified at 5Gb/s and 10Gb/s with data patterns simulating true data-traffic. Experimental results at 5Gb/s, reveal an ER value of 12.7dB with switching energies as low as 6.4fJ/bit and error-free operation with a negative power penalty of -0.2dB while verification of PhC-based memory operation at 10Gb/s reveal an ER of 6dB halving the switching energy requirements. Moreover, as the device relies on the heterogeneous integration of a InP-based PhC nanocavity with SOI passive waveguides circuitry utilizing evanescent wave coupling between the two optical levels, it enables efficient interfacing of active nanophotonic elements to be densely integrated in a circuit with direct compatibility to CMOS electronics. The footprint of the device was a record value of $6.2\mu m^2$, achieving significant reduction compared to previous PhC nanocavity-based optical memory implementations. Memory state switching-ON and switching-OFF occur at time constants lower than 50ps, indicating bit-level operation capabilities up to 20Gb/s.

The rest of this paper is organized as follows: the fabrication of the hybrid PhC nanocavity laser is presented in section II, the complete PhC nanocavity laser-based optical RAM cell concept is introduced in section III, the experimental setup is described in section IV and the respective results of the WC and SR-FF operation are examined in section V. Then, a conclusion is reached in section VI.

II. FABRICATION OF THE HYBRID PHC-BASED NANOCAVITY LASER

The structures under investigation are InP-based 1D PhC nanobeam cavities which are heterogeneously integrated onto 500nm×220nm (width×thickness) SOI wire waveguides. The
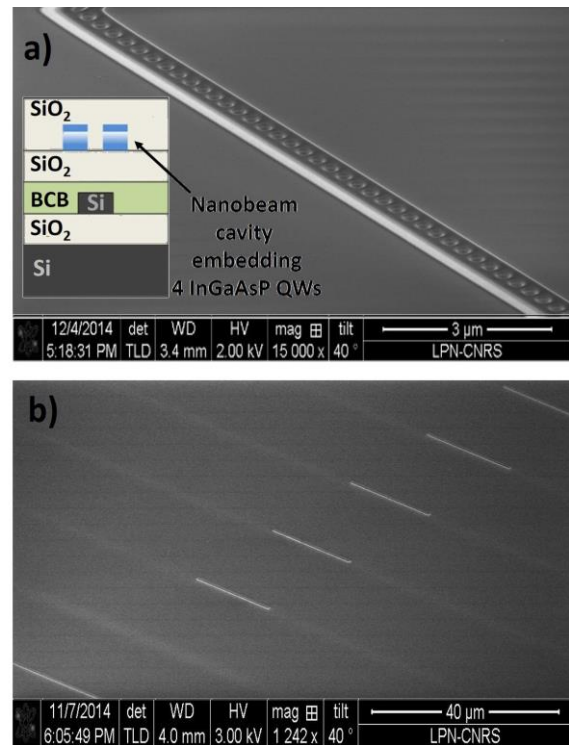

Fig. 2: SEM images of a) the photonic crystal nanocavity laser (inset with schematic view of the layers stack,) and b) fabricated silicon chip

cavities consist of 650nm×285nm (width×thickness) InP-based wires embedding four InGaAsP strained quantum wells, drilled with a row of equally-sized holes (radius=123nm). The distance between the holes is varied according to [39] in order to obtain a Gaussian field profile for the resonant mode which enables Q factors higher than 10^4 (10^6 in simulations) with $V\sim(\lambda/n)^3$. The thickness of the BCB layer is 260nm. Besides energy efficiency and ultra-fast dynamics, these cavities are also particularly interesting as they exhibit small footprint [41][42] due to their natural ability to be coupled efficiently with wire waveguides. The cavity is positioned on top of a SOI waveguide whose width was chosen properly to enable a coupling efficiency greater than 90%. The structures are encapsulated in SiO_2 in order to improve heat sinking as well as the robustness of the systems.

The fabrication of these InP-on-SOI hybrid nanocavity lasers starts with the adhesive bonding using DVS-benzocyclobutene (BCB) of a 1cm² of the InP-based heterostructure grown by molecular beam epitaxy, onto an SOI die processed with waveguides into a CMOS pilot line (Epixfab). In order to set the distance between the SOI waveguides and the III-V materials to a value enabling an efficient evanescent wave coupling, the InP material is covered with a 400nm thick SiO_2 layer before the bonding. The cavities are then patterned right on top of the SOI wires [40] using electron beam lithography followed by inductively coupled plasma etching. The etched sidewalls of the cavity are then chemically passivated using ammonium sulfide in order to reduce non radiative surface recombination of electron-hole pairs and allow CW operation of the nanocavity lasers [41]. Finally, the sample is fully encapsulated in a 1µm-thick silica layer which decreases the overall thermal resistance of the devices and increases their

robustness [42]. The total length of the device is 9.54μm, while its width is 650nm, resulting in a total footprint of 6.2μm² that is the smallest value among all PhC cavity-based optical memories reported so far. The laser was integrated with silicon photonic wire waveguides and Transverse Electric (TE) grating couplers at both input and output ends to enable fiber-to-fiber data transmission. The evaluated PhC nanocavity laser was part of a chip that incorporated 462 of PhC nanocavities emitting close to 1550nm occupying a total area of 4.2mm×250μm. This corresponds to an integration density of 440 devices/mm². In Fig. 2 a), b) SEM images of the PhC nanocavity laser and the fabricated silicon chip with the PhC nanocavity lasers are shown, respectively while the inset in Fig.2a) depicts the respective schematic stuck of the layers of every single PhC nanocavity laser. Each SOI waveguide has three PhC cavities. The distance between the PhC cavities is 100μm while the distance between SOI waveguides is 25μm. The maximum integration density that can be achieved is related to the distance between the lasers needed to avoid any optical crosstalks. In the transverse direction, putting the cavities farther than 2μm is sufficient to prevent evanescent wave coupling. In the longitudinal direction, this distance must simply be greater than the half length of the laser.

III. PHC-BASED NANOCAVITY LASER MEMORY CONCEPT

Both basic operations of the PhC-based nanocavity laser device rely on the interchanging of the laser emission state between a free-running mode (unlocked state) and an injection-controlled mode (injection-locked state), achieved through the injection of a wavelength detuned external optical signal into the device. This concept is represented graphically in Fig. 3. Initially, the PhC nanocavity laser emits at its free-running state signal, shown in red color in Fig. 3, as it is powered by an optical pump at 1180 nm. At the presence of a wavelength detuned input injection signal, called control signal, represented in blue color in Fig. 3, the laser starts emitting at the injection wavelength and not at its free-running mode wavelength when the control power increases above a specific threshold. This is called "locking" emission to the injection wavelength and it lasts until the control signal optical power is decreased below a cut-off level, where the laser emission returns to its free-running state. This process of injection locking is exploited in two different operational modes to provide: a) Access Gate (AG) by exploiting Wavelength Conversion (WC) and b) Flip-Flop (FF) operation by exploiting optical bistability, as described below.

A. InP-on-SOI PhC-based SR-FF operation

The operation of the device as a memory element relies on exploiting the bistability behavior that is exhibited in the PhC laser emission and is expressed by means of wavelength
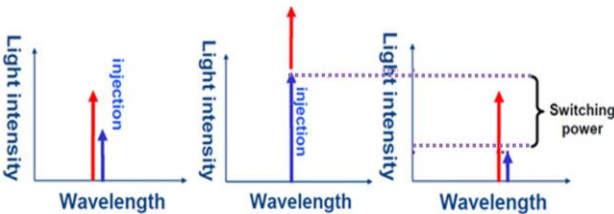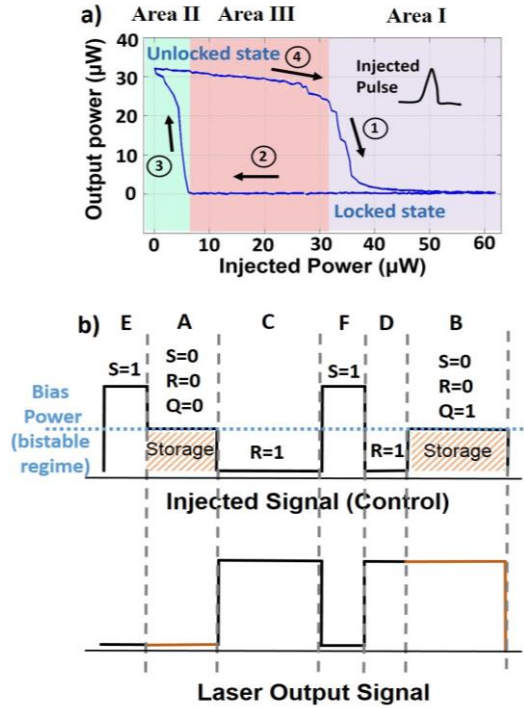

Fig. 4: a) Hysteresis loop and b) schematic representation of the SR-FF operation of the bistable PhC-based nanocavity laser device.

emission detuning controlled by the optical power of the injection signal. The bistability phenomenon occurs between the free-running mode (unlocked state) and the injection - controlled mode (injection-locked state), under specific injected optical signal power conditions. When a wavelength detuned input injection signal is inserted to the laser, it starts emitting at the injection wavelength when the control power increases above a specific threshold. However, as the control signal optical power decreases to a certain value at this state, the device enters a hysteresis loop retaining this emission state even when the control signal optical power is decreased to a certain cut-off level. Fig. 4 shows an indicative hysteresis loop formed by the PhC laser device for a given wavelength detuning. As it becomes evident, when the optical power of the injected signal
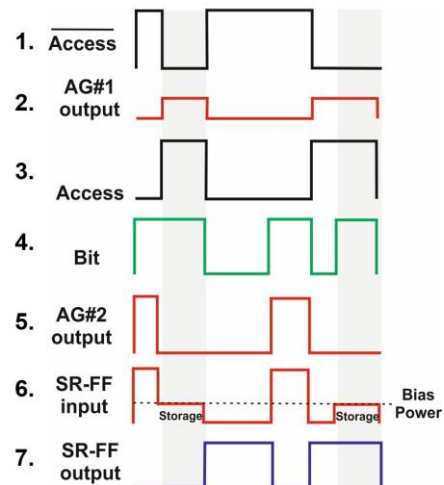

Fig. 3: Process of injection locking of the bistable PhC nanocavity laser.

Fig. 5: Schematic representation of the two AGs and SR-FF operation towards PhC-based RAM cell operation of the bistable nanocavity laser device.

falls below this cut-off level, the laser emission returns to its free-running state. Consequently, the laser emission output has two states – locked and unlocked –, which depend on the ascending or descending direction of the injection signal power and memory operation can be achieved when operating within the bistable range of the device. Consequently, the device operates as a Set-Reset Flip-Flop (SR-FF) taking advantage of the three discrete areas of injection signal optical power levels shown in Fig. 4a): Area I where injection power levels allow for Set FF operation, as the laser output is changed from free-running (unlocked) to injection-controlled (locked) state, Area II where injection power levels enable Reset FF operation as the laser output returns to the free-running (unlocked) state and Area III where injection power levels cover the bistable range and enable storing operation, as the laser emission retains its previous state. Fig.4b) shows a schematic diagram of the injected signal covering all possible states of the SR-FF. When a Set pulse is inserted into the device (timeslot E and F), the FF enters its locked state so that no optical power exits the FF at the wavelength of its free-running emission state, corresponding to a logical '0' at its output. When a Reset signal is being inserted (timeslot C and D), the device returns to its unlocked state emitting a high-power level and as such a logical '1' is obtained at its output. Whenever the incoming signal has a power level equal to the Bias threshold (timeslot A and B), the FF retains its previous state, operating in its storage regime.

B. InP-on-SOI PhC-based AG operation

As described in Section I of this manuscript, a complete optical RAM cell requires AG functionality before the SR-FF storing operation to control the communication between the memory unit and the outer world, in order to guarantee true random memory access. In this respect, access to the FF memory element is controlled via the injection of external optical Access signals. According to Fig.1b) conceptual schematic, two AG are needed in order to interpret the Bit (data to be stored) signal and $Access/\overline{Access}$ (permission to be stored) signal RAM-cell inputs to the Set/Reset and the Bias signals respectively, required by the PhC-based SR-FF to operate.

In our case, the desired AG operations are performed through the employment of the wavelength conversion capabilities of the PhC nanocavity lasers. To make this more clear, Fig.5 shows a schematic diagram of the injected signal into the two Access Gates and the respective combined output that feeds the

three-state SR FF to obtain complete optical RAM cell operation. The 1st and the 2nd row of Fig.5 correspond to the Inverted Access signal and the output of the first AG (AG#1), corresponding to a directly wavelength converted output signal. The inverted Access Bit pulse will force the laser to emit at the injection wavelength and not at its free-running mode wavelength, provided that its power is beyond a specific threshold. By monitoring the free-running wavelength, a logical "0" pulse will form. However, when the inverted Access Bit becomes "0", the laser emission returns to its free-running mode wavelength, forming in this way the "1" level pulse of the Bias signal.

The role of AG#2 is to produce the Set/Reset signal of the FF that encodes a NAND operation between the Bit and the Access signal. The Access Bit of logical "1" value will block communication between the memory cell and the outer world. When the Access Bit becomes "0", the Set/Reset signal is formed through the injection locking process induced by the logical value of the Bit signal. In this case, the PhC nanocavity laser is injected two optical control signals, the Bit and the Access signals. The 3rd, 4th and 5th rows of Fig.5 depict the Access signal, the Bit signal and the output of the second AG (AG#2). At the presence of either the injected Bit signal pulse, the Access signal pulse or both signals pulses, the nanocavity laser starts emitting at the injection wavelength and not at its free-running mode wavelength. In this case, the 6th row represents the combined output of both AGs that result in a three-level signal entering the FF. Finally, the 7th row depicts the final FF/RAM cell output.

As it is evident, both cases of AG operation proposed in the PhC-based optical RAM cell are based on the wavelength conversion operation capabilities of the nanocavity laser that rely on the laser injection locking properties of the device. As the injected external optical signal switches the laser output to the injection wavelength, the injection signal is inversely imprinted to the free-running wavelength, achieving in this way the required wavelength conversion. On that account, wavelength conversion operation of the PhC nanocavity laser is evaluated for monitoring single AG operation.

IV. EXPERIMENTAL SETUP

The proposed PhC nanocavity laser was experimentally evaluated as a Wavelength Conversion Access Gating element and also as a SR-FF to ensure its applicability in complete
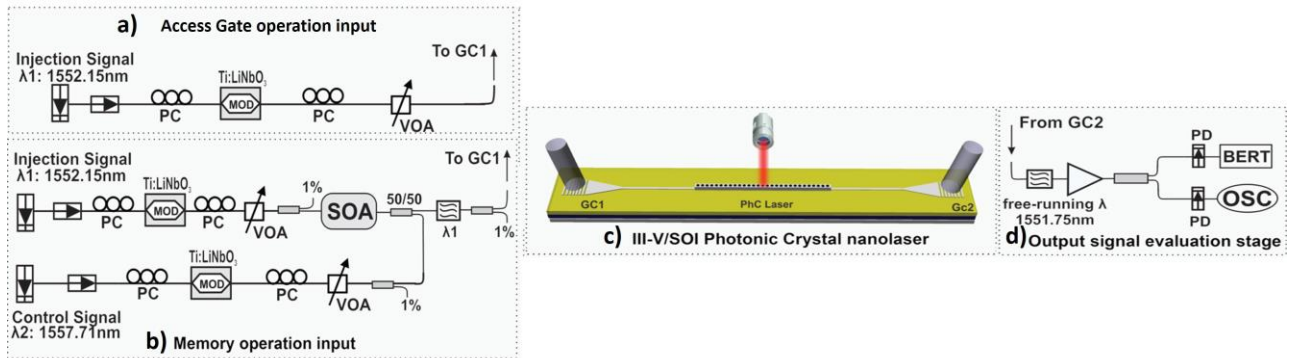

Fig. 6: Experimental setup and signal generation for the: a) Wavelength Conversion-based AG operation b) Bit-level optical Set-Reset Flip Flop memory evaluation c) III-V/SOI PhC nanocavity with I/O grating couplers and d) Signal evaluation stage.

optical RAM-based systems. The experimental evaluation was performed utilizing signals with true repetition rates of up to 10Gb/s and employing PRBS-like data patterns, so as to demonstrate the device capabilities under real-type data-traffic environments. The following subsections describe the experimental setup employed for the verification of the PhC-based WC Access Gating and FF operation.

A. Wavelength Conversion (WC) operation at 10Gb/s

To evaluate the wavelength conversion performance of the PhC laser, the experimental setup shown in Fig.6a) was employed. The device was powered with an optical pump signal at 1180nm, which was injected vertically to the nanocavity laser using a 10× microscope objective, so as to adjust aperture and enhance the absorption of the pump signal. The pump power was set at 103.5µW, corresponding to 4.5 times the laser threshold. This value refers to the estimated absorbed pump power in the quantum wells. A laser at $\lambda1$=1552.15 nm was modulated with a 2^{31}-1 PRBS data pattern at 10Gb/s Non-Return-to-Zero (NRZ) line-rate in a Ti:LiNbO$_3$ Mach-Zehnder modulator for the generation of the injection optical signal. The data signal was injected into the SOI motherboard through the input Grating Coupler (GC1) while a polarization controller was employed to compensate for the polarization dependence of the grating coupler, together with a VOA (Variable Optical Attenuator) to control the injected signal power levels. After the WC operation in the PhC nanocavity laser (Fig.6c), the product signal of the PhC laser was received at the output Grating Coupler (GC2). Lensed fibers with a spot size diameter of 5µm and anti-reflection coatings were used for injecting and collecting light at both grating couplers in order to avoid back-reflections at cleaved fibers' facets. The coupling loss between the lensed fibers and each of the grating couplers was 7dB. As can be seen in Fig.6 d) the output signal was then filtered in a bandpass filter with a 3-dB bandwidth of 0.02nm, which was centered at the laser's free-running mode wavelength, prior to being amplified through an Erbium Doped Fiber Amplifier (EDFA) and recorded at a sampling oscilloscope. Finally, an Error Detector was used for performing Bit Error Rate (BER) measurements.

B. Set Reset Flip-Flop (SR-FF) operation at 5Gb/s and 10Gb/s

To evaluate the performance of the PhC nanocavity laser as a SR-FF, different injection signal line rates were selected, namely 5 and 10 Gb/s. Again, the device was powered with 103.5µW of an optical pump signal at 1180 nm. For the generation of optical input signal that simulates the encoded Set and Reset signals of the SR-FF, an SOA was employed as a gating element to form the three-level signal containing the Set and Reset pulses as well as the Bias state. For this PhC control signal preparation, two individual lasers emitting light at $\lambda1$=1552.15 nm (Injection signal) and $\lambda2$=1557.71 nm (Control signal of the SOA), respectively, were modulated by a NRZ custom-made pattern in a Ti:LiNbO$_3$ Mach-Zehnder modulator, as can be observed in Fig.6 b). The line rate of the NRZ custom pattern was 5Gb/s and consequently 10Gb/s. This custom pattern was programmed appropriately, so as to evaluate its performance in fast memory state switching employing a

PRBS-resembling stream and also induce long periods of '1' or '0' to demonstrate the device's capability for long memory state holding. Again, the use of VOAs and PCs ensured proper signal input powers and compensation for the SOA's polarization gain dependence. The two signals were then injected into the SOA, with the Control signal at $\lambda2$ being the stronger one and inducing a Cross Gain Modulation (XGM) process in the SOA and reducing its gain. As a result, the amplitude of any Injection signal pulse that coincides in the SOA with a Control signal pulse was reduced. The pulses with reduced amplitude serve as the Bias signal that maintains the memory state of the device. The ratio between the amplitude of the unaffected Injection signal pulses and the suppressed Bias pulses was set to follow the hysteresis loop of the PhC nanocavity laser device. This amplitude ratio was properly adjusted through the optical power of both input signals of the SOA. An optical bandpass filter with a 3-dB bandwidth of 1nm was used at the output of the SOA to select only the injection Signal at $\lambda1$. The PhC injection signal – now consisting of three levels, corresponding to Set, Reset and Bias- was then launched into the SOI motherboard through the input grating coupler (GC1) and into the bistable photonic crystal nanocavity laser. Again, a PC was employed to compensate for the polarization dependence of the grating coupler, while a VOA sufficiently attenuated the signal. The output signal of the bistable photonic crystal was then received at the output grating coupler (GC2). The rest of the SR-FF memory evaluation was the same with the WC case as presented in Fig.6 c) and d).

V. Experimental Results

A. WC operation at 10Gb/s

The experimental results of the evaluation of the PhC nanocavity laser device as a wavelength conversion access gating element are depicted in Fig.7. The pulse trace of the $\lambda1$ input signal of the PhC nanocavity laser (injection signal) at 10Gb/s is shown in Fig.7 a) while the pulse trace of the wavelength-converted signal at the $\lambda2$ free-running laser wavelength is illustrated in Fig.7 b), confirming the complementarity between the two signals and thus the successful operation of the PhC laser as an access gating element. The successful wavelength conversion operation of the proposed device can be also confirmed by the eye diagrams depicted in Fig.7 c) and d) for the input and output signals, respectively. An can be observed, a clear open eye diagram is obtained at the output with an Extinction Ratio (ER) of 12dB and an Amplitude Modulation (AM) of 1.5dB. The switching energy was calculated 4.8fJ/bit at 10Gb/s for average optical input power of 24µW. By taking into account the optical pump the power consumption for the AG is found to be 15.1fJ/bit at 10Gb/s. Fig.7 e) shows the BER curves versus the received power for the WC operation at 10Gb/s. Error-free operation was achieved for the $\lambda2$ wavelength-converted signal with a power penalty of 1dB.

B. SR-FF operation at 5Gb/s - 10Gb/s

Successful experimental demonstration of the PhC-based laser operating as a SR-FF was achieved for several data patterns. Fig.8 shows an experimentally obtained data trace at the a)

input and b) output of the SR-FF confirming its successful operation at 5Gb/s at 1552.15nm. Fig. 8a) shows the input signal as obtained at the output of the SOA with three logical levels, the logical one, Bias and the logical zero imprinted as it is imprinted in the free-running laser wavelength at 1551.75nm while Fig. 8b) shows the final SR-FF memory content. When a bit of logical '1' Set signal is injected into the PhC laser, the SR-FF enters its locked state, resulting in a logical '0' state the output of the SR-FF. When a bit of logical "0" Reset pulse is inserted into the laser, it unblocks the free-running transmission state and the laser is switched back to its initial state of logical '1' value. In case of a Bias pulse, the SR-FF memory content remains unaltered retaining its last value. This situation is evident in the Bias pulses that are highlighted with blue color in Fig. 8a) and b), depicting four different cases of memory operation provided by the PhC nanocavity laser. The 1st highlighted area depicts two Bias pulses following a Set pulse resulting in a logical zero state for three consecutive bit slots at the SR-FF output, as shown in Fig. 8b). The 2nd highlighted area presents three Bias pulses after a single Reset pulse that result in logical one state for four bits at the output of the SR-FF as shown in Fig. 8b). The 3rd and the 4th highlighted areas show the retention time of the SR-FF memory after one Set and seven Reset pulses. Successful memory operation is observed in both cases in Fig. 8b) where memory output stays constant to a

logical zero state for a duration of 8 bits, approximately 1.6ns, and to a logical one state for 15 bits corresponding to a memory time duration of 3ns, respectively. Fig.8 c) and d) illustrate the rise and fall times of the FF output pulses with 10%-to-90% values being approximately 50ps, indicating potential speed capabilities of up to 20Gb/s. Fig.8 e) and f) show the respective eye diagrams for the Set/Reset signal and the SR-FF output providing a more detailed look into the performance of the demonstrated device. Clear open eye diagram is obtained for the SR-FF operation at 5Gb/s with an ER of 12.7dB and an AM equal to 1dB. The input eye diagram exhibits three logical levels corresponding to the three logical states, the logical one, the Bias and the logical zero level as shown in the right inset and corresponds to an ER of 11.7dB and an AM of 0.8dB. Fig.8
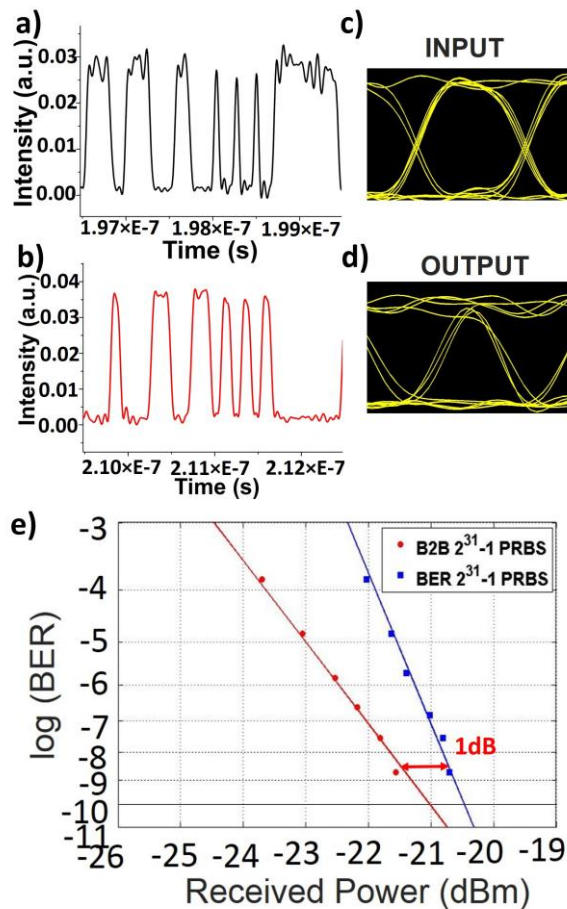

Fig. 7: a) Input pulse trace inserted into the PhC nanocavity laser for WC operation, b) Output pulse trace obtained at the exit of the nanocavity laser, c) input d) output eye diagrams and e) BER curves for the wavelength conversion at 10Gb/s.

Fig. 8: a) Input pulse trace with three logical levels (logical one, bias, logical zero) inserted into the PhC-based SR-FF, b) Output pulse trace obtained at the exit of the FF, c) Rise and d) Fall time of the FF output pulses e) input f) output eye diagrams and g) BER curves for PhC-based SR-FF at 5Gb/s.
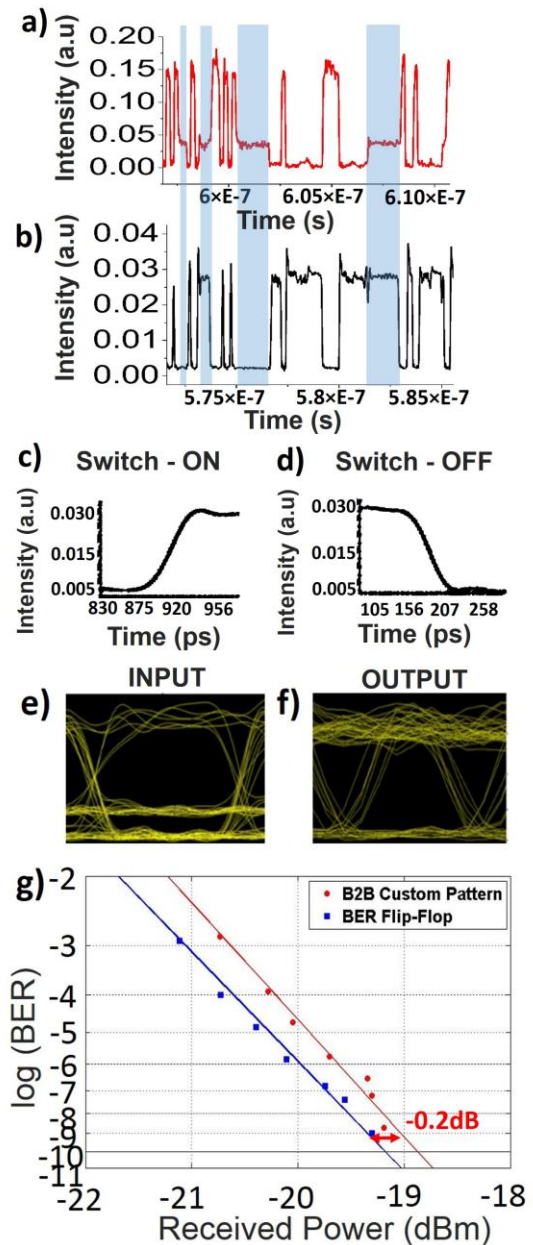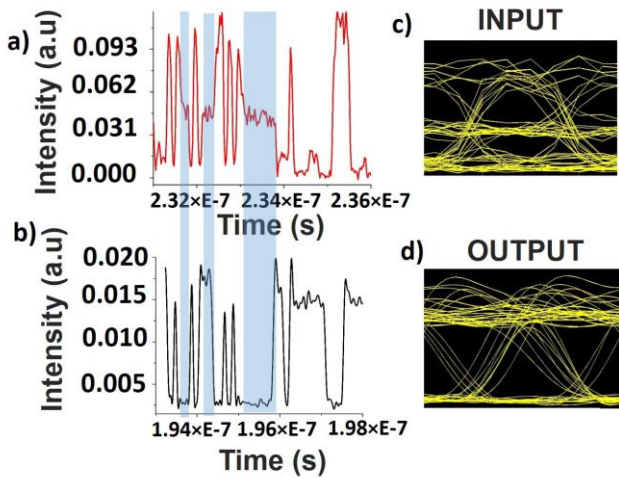
Fig. 9: a) Input pulse trace with three logical levels (logical one, bias, logical zero) inserted into the PhC-based SR-FF, b) Output pulse trace at the exit of the SR-FF, c) input d) output eye diagrams for PhC-based SR-FF at 10Gb/s.

g) shows the BER curves obtained for the PhC-based SR-FF operation at 5GHz. Back-to-Back (B2B) measurement was obtained by using the same custom-made 127-bit pattern, employed to demonstrate SR-FF operation, transmitted through the system without entering the PhC-based laser, with no Bias level. Error free SR-FF operation at 10^{-9} BER value was achieved for the device at 5Gb/s, revealing a negative power penalty of -0.2dB. The regenerative properties of the demonstrated laser device are mainly due to the improvement of noise in the"0" level, induced by the SOA used to construct the Set/Reset signal. The average optical Bias power was 8μW, the input optical power was measured to be 20μW and the average output power of the laser was 19.9μW taking into account the grating coupler losses in both cases. In the absence of any input signal, the laser emission was 34.6μW. PhC-based SR-FF memory operation was achieved with a switching energy of 6.4fJ/bit at 5GHz at the pump power of 103.5μW, for a given memory output ER of 12.7dB.

Then, the memory operation of the PhC nanocavity laser device was experimentally evaluated at 10Gb/s. Fig.9 shows an experimentally obtained data trace at the a) input and b) output of the SR-FF proving its successful operation at 10Gb/s. Fig.9 a) shows the input signal as obtained at the output of the SOA with three logical levels, the logical one, Bias and the logical zero imprinted at 1552.15nm while Fig. 9b) illustrates the final SR-FF memory content as it is imprinted in the free-running laser wavelength at 1551.75nm. The memory state holding of the device can be witnessed at the areas highlighted with blue color in Fig. 9a) and 9b). The first highlighted area depicts one Bias pulse following a Set pulse resulting in a logical zero memory state for two consecutive bit slots at the FF output, as shown in Fig.9 b). The second highlighted area presents two Bias pulses after a single Reset pulse resulting in logical one memory state retained for three bits at the FF output while the third highlighted area shows eight Bias pulses after one Set indicating that memory output stays constant to a logical zero state for a duration of 8 bits, corresponding to approximately 800ps. Fig. 9c) and d) show the eye diagrams for the input signal and the SR-FF output, respectively. The input signal exhibits an ER value as low as 7dB and an AM of 1.5dB,

whereas the SR-FF output signal exhibits an ER of 6dB and an AM of 0.8dB. The reduced performance of the SR-FF in terms of ER stems from the degraded SOA performance at 10Gb/s. In addition, employing the SOA to produce the required three-level input signal at 10Gb/s leads to the appearance of severe pattern effects [43] in the three-level SR-FF input signal that are imprinted –among other- as jitter variation at the output signal of the SR-FF. As a result the input signal injected to the PhC nanocavity laser at 10Gb/s is of poorer quality compared to the input signals at 5Gb/s, hindering in this way the error-free performance of the SR-FF. To this end, the successful SR-FF memory operation at 10Gb/s was evaluated only with eye-diagrams and as it retains the same operational conditions with 5Gb/s operation, it now yields a reduced switching energy of 3.2fJ/bit. By taking into account the optical pump the power consumption for the SR-FF is found to be 27fJ/bit and 13.5fJ/bit for 5Gb/s and 10Gb/s respectively. Moreover, as the device exhibits fast rise and fall times of approximately 50ps, the employment of faster SOAs or other alternative switching elements for the generation of the three-level SR-FF input signal can potentially lead to successful SR-FF operation in speeds of up to 20Gb/s. Recent advances [44] on electrically-driven PhC nanocavity lasers have demonstrated up to 11% wall-plug efficiency improving the power conversion efficiency of the demonstrated optically pumped PhC laser where only a fraction of the pump is absorbed resulting in pumping. The electrically pumped PhC laser device [44] requires a power consumption of 500μm, that corresponds to 25fJ/bit considering an operational speed of 20Gb/s and is also expected to improved heat sinking and stability of the device, occupying an area of less than 100μm^2.

VI. CONCLUSION

We have presented an InP-on-Silicon PhC-based nanocavity laser that can serve as the fundamental building block for energy efficient, ultra-compact and high-speed RAM setups by exhibiting two individual elementary RAM functions: a) Access Gate and b) SR-FF operation. The AG operation was confirmed by successful WC at 10Gb/s requiring only 4.8fJ/bit switching energy. Moreover, successful SR-FF memory operation with the same device was achieved by exploiting the bistability behavior of the nanocavity laser both at 5Gb/s and 10Gb/s with record switching energies of 6.4fJ /bit and 3.2fJ/bit, respectively. By including the optical pump the power consumption for the SR-FF is found to be 27fJ/bit and 13.5fJ/bit for 5Gb/s and 10Gb/s respectively while the power consumption for the AG module is 15.1fJ/bit. The presented PhC laser device exhibits the smallest size among all integrated optical memory implementations with a total footprint of 6.2μm^2, raising expectations for densely integrated optical memories. The device also offers ultra-fast dynamics with switching times of <50ps for both ON and OFF state, indicating bit-level memory capabilities in the order of 20 Gb/s.

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