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Imbalance Current Analysis and Its Suppression Methodology for Parallel SiC MOSFETs With Aid of a Differential Mode Choke

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***Abstract*—Parallel connection of SiC MOSFETs is a cost-effective solution for high-capacity power converters. However, transient imbalance current, during turn-on and -off processes, challenges the safety and stability of parallel SiC MOSFETs. In this paper, considering the impact factors of device parameters, circuit parasitics, and junction temperatures, in-depth mathematical models are created to reveal the electro-thermal mechanisms of the imbalance current. Moreover, with the incorporation of a differential mode choke (DMC), an effective approach is proposed to suppress the imbalance current among parallel SiC MOSFETs. Physic concepts, operation principles, and design guidelines of the DMC suppression method are fully presented. Besides, to reduce the equivalent leakage inductance and equivalent parallel capacitance of the DMC, winding patterns of the DMC are comparatively studied and optimized to suppress turn-off over-voltage and switching ringing. Concerning the influence of winding patterns, load currents, gate resistances, and junction temperatures, experimental results are comprehensively demonstrated to confirm the validity of theoretical models and the function of the proposed DMC suppression method. It is turned out the low-cost DMC is easy to design and utilize without complex feedback circuits or control schemes, which is a cost-effective component to guarantee consistent and synchronous on-off trajectories of parallel SiC MOSFETs.**

***Index Terms*—Parallel SiC MOSFETs, mechanism of imbalance current, consistency and synchronization of on-off trajectories, differential mode choke.**

I. Introduction

HIGH-frequency and high-capacity power converters are increasingly demanded for transportation electrification and smart grid applications to reduce cost, improve power-density, and save manpower [1]–[3]. Thanks to the high switching speed and low switching loss, SiC MOSFET device becomes more and more popular for high-frequency power converters [4]–[6]. However, due to the low yield rate in the wafer and high thermal-mechanical stress in the device, the active area of SiC chip is limited, and the current rating of commercial SiC chip is within 100A [4], generally. Parallel connection of SiC MOSFETs is an invertible approach to elevate the current rating of the power device and pursue the high capacity of the power converter. However, the unacceptable imbalance current among parallel SiC MOSFETs poses unsolved challenges [1], [2].

Static and transient imbalance current among parallel SiC MOSFETs may lead to over-current, over-temperature, even thermal runaway, which challenges the safety of parallel devices and limits the usable current rating [7]. The static imbalance current might be automatically suppressed by the positive temperature-dependent on-resistance of device. However, compared with Si counterpart, the on-resistance of SiC MOSFET is not sensitive to junction temperature [8]. The inherent current-sharing capability of SiC MOSFET by using on-resistance is restricted. Besides, the transient imbalance current cannot be self-suppressed by the parallel devices [9], [10]. In contrast, the negative temperature-dependent threshold voltage undesirably increases the transient imbalance current. Due to the challenge of imbalance current, current de-rating is inevitable to design and use the parallel SiC MOSFETs. Current capacities of parallel devices are not fully utilized, which is undesired and uneconomical [11], [12]. Therefore, the transient imbalance current should be carefully addressed for high-capacity applications of parallel SiC MOSFETs.

Some researches focus on the reasons of imbalance current among parallel SiC MOSFETs. From the viewpoint of manufacturing and material, SiC MOSFETs are not as mature as their Si counterparts. Differences in electrical parameters of parallel SiC MOSFETs may lead to imbalance current [13], [14]. For instance, inconsistent threshold voltages of parallel SiC MOSFETs result in asynchronous turn-on and -off trajectories, as well as the imbalance current. Besides, an asymmetrical circuit layout results in mismatched parasitics in power loops, common source loops, and gate loops among parallel SiC MOSFETs [15], [16]. The mismatched parasitic inductances result in asymmetrical impedances and increase the imbalance current among parallel branches [17], [18].

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Furthermore, unequal junction temperatures of parallel SiC MOSFETs also lead to imbalance current by the electro-thermal coupling of temperature-sensitive electrical parameters [19]–[21]. However, how the imbalance current generated and expanded is still poorly modeled. In-depth principles and mathematical models of the imbalance current should be carefully concerned to suppress it better.

Recently, some existing approaches have been reported to overcome the imbalance current [22]–[32]. Series resistor inserted into the parallel branches can limit the static imbalance current, but it does not affect on the transient imbalance current. Some researches focus on the optimal layout of direct bonding copper (DBC) to guarantee consistent parasitics and balance currents of parallel SiC MOSFETs [22], [23]. Generally, it is costly and time-consuming to design novel and effective DBC layouts for parallel SiC MOSFETs. Additionally, an absolutely symmetrical DBC layout does not exist, so it is a very challenging task to suppress the imbalance current by using optimized DBC. With the aid of differential current sensor and analog time-delay controller, the active gate driver is a practical approach to handle the imbalance current and ensure the synchronous trajectories of parallel MOSFETs [24]–[26]. By using active gate driver, the differential current sensor with multi-channel and high-bandwidth property is difficult to fabricate. Besides, the analog feedback control is complicated to design. Therefore, to overcome the imbalance current, some simple approaches based on passive elements should be further investigated. Inductance-based passive balancing is a creative solution, which has been proposed to reshape the loop impedance and limit the imbalance current [27]–[31]. The inserted passive inductances and gate resistances change the impedance of gate-source loops, the stability of parallel SiC MOSFETs in transient processes ought to be further addressed [32]–[34]. However, thanks to the benefits of low cost, fast dynamics, and easy design, passive-based approaches to suppress the imbalance current are promising solutions and need more concerns.

Revisiting the imbalance current issue of parallel SiC MOSFETs, the imbalance current is a kind of differential mode current, essentially. Inspired by the successfully used common mode chokes to attenuate common mode current in high-frequency power supplies, an interesting idea is naturally generated as: the imbalance current can be suppressed by a simple differential mode choke (DMC).

In this paper, in-depth mathematical models are proposed to reveal the electro-thermal principles of imbalance current among parallel SiC MOSFETs. After that, a DMC-based suppression methodology is proposed, designed, and verified to guarantee the consistent and synchronous on-off trajectories of parallel SiC MOSFETs. The rest of this paper is organized as follows. The phenomenon of imbalance current issue is briefly described and analyzed in Section II. In Section III, to understand the imbalance current, electro-thermal mechanisms of the imbalance current are comprehensively modeled and analyzed. In Section IV, the DMC-based method is proposed to suppress the imbalance current. Physic concepts, operation principles, and design guidelines of the DMC are also presented. In Section V, considering multiple impact factors, extensive experiments are provided to confirm the validity of the proposed approach. Extension and comparison of proposed DMC suppression method are illustrated in Section VI. Finally, Section VII summarizes this paper.

II. Problem Description: Imbalance Current Among Parallel SiC MOSFETs

The configuration of parallel SiC MOSFET devices under test (DUTs) is shown in Fig. 1. Some key variables are listed in TABLE I. i_{d1} and i_{d2} are drain currents, where subscripts 1 and 2 respectively represent DUT 1 and DUT 2. Typically measured imbalance current issue of parallel SiC MOSFETs is demonstrated in Fig. 2.

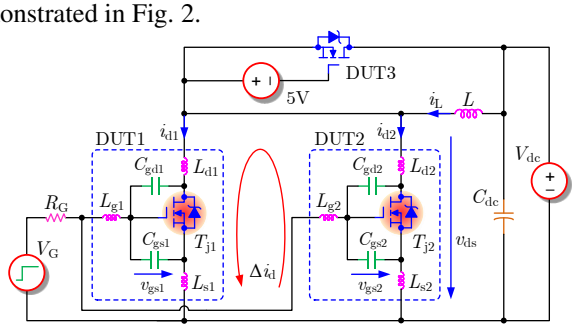

Fig. 1. Schematic circuit of parallel SiC MOSFETs.

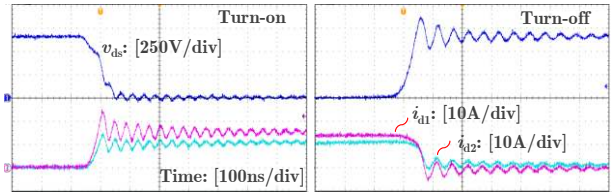

Fig. 2. Imbalance current issue of parallel SiC MOSFETs.

TABLE I
PARAMETERS OF TEST RIG

V_{dc}	DC-link voltage	v_{gs}	Gate-source voltage
C_{dc}	DC-link capacitance	C_{gd}	Gate-drain capacitance
v_{ds}	Drain-source voltage	C_{gs}	Gate-source capacitance
L	Load inductance	L_g	Gate loop inductance
i_L	Load current	L_d	Power drain inductance
V_G	Output voltage of gate driver	L_s	Common source inductance
R_G	Gate resistance	T_j	Junction temperature

Compared SiC MOSFET C2M0080120D from Wolfspeed to Si MOSFET IXFK32N100Q3 from IXYS, the temperature-dependent R_{dson} and threshold voltage V_{th} are depicted in Fig. 3. The R_{dson} of SiC device is less sensitive to temperature than Si device. The self-current-sharing capability of SiC MOSFET is limited. In contrast, the negative temperature-dependent V_{th} degrades the current-sharing performance. Therefore, the imbalance current of parallel SiC MOSFETs is more severe than Si ones. Mechanism models and physic methods are urgently needed to understand and suppress the imbalance current.

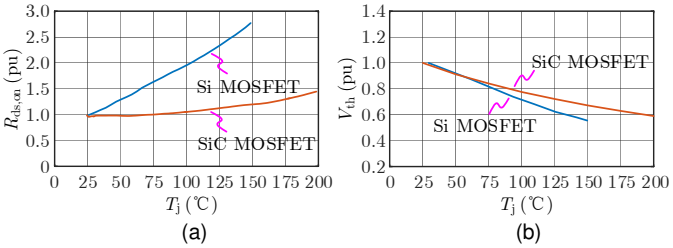

Fig. 3. Comparison of SiC and Si MOSFETs. Temperature-dependent (a) on-resistance R_{dson} and (b) threshold voltage V_{th}.

III. Mathematical Mechanisms of Imbalance Current From Electro-Thermal Perspective

The imbalance current among parallel SiC MOSFETs is mainly influenced by three factors: inconsistent device parameters, asymmetrical circuit layouts, and unequal junction temperatures. These inevitable factors jointly result in the imbalance current $\Delta i_d = i_{d1} - i_{d2}$, which can be expressed as

$$\Delta i_d = F_i(\Delta V_{th}, \Delta\beta, \Delta L_d, \Delta L_s, \Delta T_j), \quad (1)$$

where $F_i(\cdot)$ is a nonlinear function; ΔV_{th} and $\Delta\beta$ are dispersing threshold voltage and transconductance coefficient of parallel devices; ΔL_d and ΔL_s are mismatched stray inductances at drain and source terminals; ΔT_j is junction temperature difference of parallel devices.

Although the impact of individual factor may be small, the entire imbalance current Δi_d might be unacceptable. Lacking of mechanism models to characterize the imbalance current, it poses an unsolved challenge to rebalance the load currents of parallel SiC MOSFETs.

The imbalance current is nonlinearly influenced by many factors as indicated in (1). It is not possible to consider all the impacts at the same time. Based on the small-signal analysis methodology, some essential principles of imbalance current are mathematically modeled considering the electro-thermal factors one-by-one as follows.

A. Impact of Dispersing Device Parameters

Drain current of either SiC MOSFET in Fig. 1 can be expressed as

$$i_d = \begin{cases} 0 & \text{if } v_{gs} < V_{th} \\ g_m(v_{gs} - V_{th}) = \beta(v_{gs} - V_{th})^2 & \text{if } v_{gs} \geq V_{th} \end{cases}, \quad (2)$$

where g_m and V_{th} are the transconductance and threshold voltage. Transconductance coefficient is β determined by the structure size of chip [35], which can be written as

$$\beta = \frac{\mu_n C_{OX} Z_{CH}}{2L_{CH}}, \quad (3)$$

where μ_n is the majority-carrier mobility. C_{OX} is the gate oxide capacitance per unit area, $C_{OX} = \varepsilon_{OX}/t_{OX}$. ε_{OX} is the dielectric constant of the silicon dioxide. t_{OX} is the thickness of the gate oxide. Z_{CH} and L_{CH} are channel width and length.

According to Fig. 1, the transfer function model from gate drive voltage V_G to gate-source voltage v_{gs} can be written as

$$V_{gs}(s) = \frac{1}{(L_g + L_s)C_{gs}s^2 + R_G s + 1} V_G, \quad (4)$$

where $s = j2\pi f$ is the Laplace operator; f is the specific frequency; C_{gs} is the gate-source capacitance of SiC MOSFET; L_g and L_s are parasitic inductances at gate and source terminals; R_G is gate resistance of gate driver, as summarized in TABLE I. $V_{gs}(s)$ is the gate-source voltage in frequency domain. The gate-source voltage in time domain can be derived from (4) by using inverse Laplace transform, $v_{gs} = \mathscr{L}^{-1}[V_{gs}(s)]$.

If the parameter variation of V_{th} is ΔV_{th}, the transient imbalance current caused by ΔV_{th} can be expressed as

$$\Delta i_d(\Delta V_{th}) = \frac{\partial i_d}{\partial V_{th}} \Delta V_{th} = -2\beta(v_{gs} - V_{th})\Delta V_{th}. \quad (5)$$

According to (4), during turn-on and -off processes, because the impedances of stray inductances and capacitance are affected by specific frequency, the gate-source voltage v_{gs} in time domain can be analyzed in frequency domain to understand the frequency-related principles of imbalance current.

Similarly, transient imbalance current caused by dispersing parameter β can be derived as

$$\Delta i_d(\Delta\beta) = \frac{\partial i_d}{\partial\beta} \Delta\beta = (v_{gs} - V_{th})^2 \Delta\beta, \quad (6)$$

where $\Delta\beta$ is the parameter variation of β.

Taking C2M0080120D as an example, in (2)–(6), $V_G = 20$ V, $V_{th} = 2.6$ V, $\beta = 1$ A/V^2, $R_G = 20\Omega$, $C_{gs} = 1980$ pF at 600 V [36], parasitics $L_g = 9.2$ nH, $L_s = 7.5$ nH [37]. According to (4) and (5), the numerical results of Δi_d caused by ΔV_{th} and influenced by v_{gs} is illustrated in Fig. 4 (a). It can be found the magnitude of transient imbalance current Δi_d dramatically increases with v_{gs}, ΔV_{th}, and β.

The transient imbalance current in frequency domain is depicted in Fig. 4(b). The imbalance current in three-dimension space can be mapped to two-dimension space as shown in Fig. 4(c) and (d).

Although the maximum switching frequency of SiC MOSFET may be up to several MHz, the commonly used switching frequency of SiC MOSFET is from several dozens of kHz to several hundreds of kHz. As shown in Fig. 4(b) to (d), frequency-dependent transient imbalance current is attenuated above 1 MHz, considering the frequency range from switching frequency to ten times of switching frequency. Due to the un-negligible imbalance current, the imbalance current in the considered frequency range should be paid enough attention.

Besides, in Fig. 4, it can be concluded that small β is useful to reduce the transient imbalance current. The imbalance current Δi_d can be eliminated if and only if $\Delta V_{th} = 0$. However, due to the difficulty of device fabrication, the parameter variation of SiC MOSFET is inevitable.

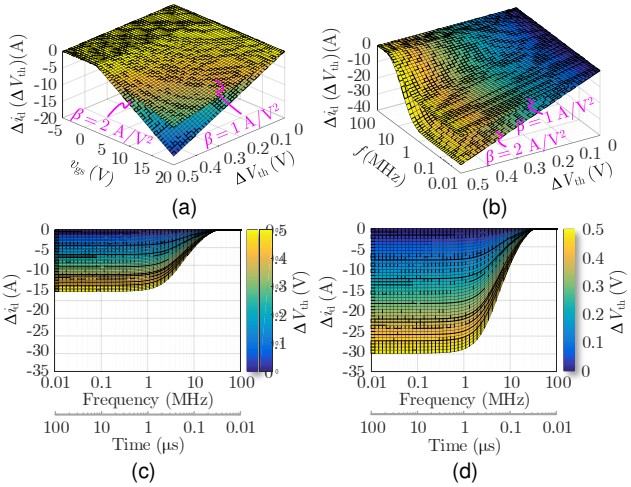

Fig. 4. Imbalance current affected by dispersing parameter V_{th} at $I_L = 30$ A. (a) Δi_d versus v_{gs} and ΔV_{th}, (b) Δi_d versus f and ΔV_{th}, (c) mapped Δi_d versus f at $\beta = 1$ A/V^2, and (d) mapped Δi_d versus f at $\beta = 2$ A/V^2.

Similarly, according to (4) and (6), the impact of β is numerically illustrated in Fig. 5. The transient imbalance current Δi_d increases with v_{gs}, $\Delta\beta$, and f. Besides, it is figured out that increasing the threshold voltage V_{th} is helpful to suppress the imbalance current.

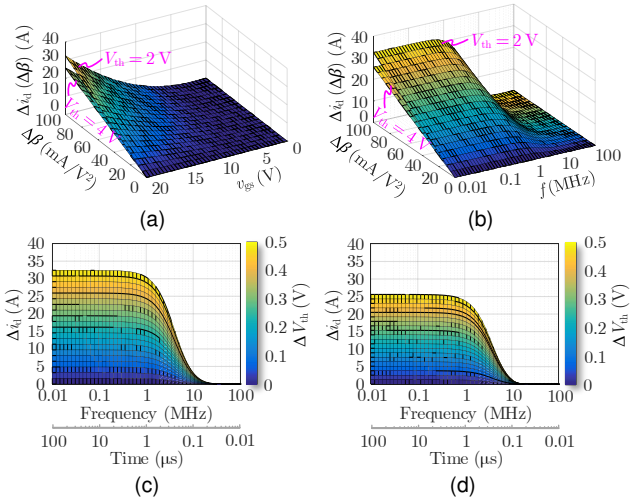

Fig. 5. Imbalance current affected by dispersing parameter β at $I_L = 30$ A. (a) Δi_d versus $\Delta\beta$ and v_{gs}, (b) Δi_d versus $\Delta\beta$ and f, (c) mapped Δi_d versus f at $V_{th} = 2$ V, and (d) mapped Δi_d versus f at $V_{th} = 4$ V.

B. Impact of Mismatched Stray Inductances

Caused by asymmetrical layouts of parallel devices in power package or power circuit, mismatched stray inductances also lead to transient imbalance current. The mismatched parasitics mainly come from power drain inductance L_d and common source inductance L_s in power loops.

Accounting for the mismatched L_d, parallel branches in Fig. 1 satisfy Kirchhoff's voltage law, which can be expressed as

$$L_{d1}\frac{di_{d1}}{dt} + L_{s1}\frac{di_{d1}}{dt} + i_{d1}R_{dson1} = L_{d2}\frac{di_{d2}}{dt} + L_{s2}\frac{di_{d2}}{dt} + i_{d2}R_{dson2} = v_{ds}\,, \quad (7)$$

where R_{dson1} and R_{dson2} are on-resistances of parallel SiC MOSFETs. Supposing $R_{dson1} = R_{dson2} = R_{dson}$, $L_{s1} = L_{s2} = L_s$, and $L_{d1} = L_{d2} + \Delta L_d$, where ΔL_d is the difference of drain stray inductances between parallel branches, (7) can be rewritten as

$$\Delta L_d\frac{di_{d1}}{dt} + (L_{d2} + L_s)\frac{d\Delta i_d}{dt} + R_{dson}\Delta i_d = 0\,. \quad (8)$$

The slope of drain current i_{d1} is determined by the performance of SiC MOSFET, which can be approximately expressed as

$$\frac{di_{d1}}{dt} \approx \frac{1}{2}\frac{I_L}{t_r}\,, \quad (9)$$

where I_L is the load current in load inductor, t_r is the transient time of device's drain current rising from 0 to $I_L/2$.

Therefore, Δi_d caused by mismatched L_d can be expressed as

$$\Delta i_d(\Delta L_d) = -\frac{I_L}{2t_r[(L_{d2} + L_s)s + R_{dson})]}\Delta L_d\,. \quad (10)$$

It can be seen Δi_d is proportional to I_L/t_r, which means slow switching speed is useful to reduce the transient imbalance current caused by ΔL_d. Additionally, the maximum value of transient imbalance current occurs at $s = 0$, which can be expressed as

$$\Delta I_d(\Delta L_d) = \Delta i_d\big|_{s=0} = -\frac{I_L}{2R_{dson}t_r}\Delta L_d\,. \quad (11)$$

Taking $L_{d2} = 5.9$ nH, $R_{dson} = 80$ mΩ, $L_s = 7.5$ nH, and $g_m = 2.4$ S for example, the imbalance current Δi_d versus ΔL_d and t_r is depicted in Fig. 6. Transient imbalance current should be paid more attention for high-frequency application of SiC MOSFET with very small t_r.

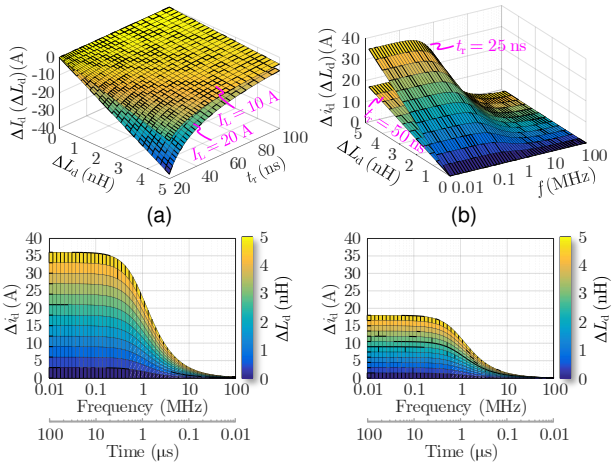

Fig. 6. Imbalance current affected by mismatched L_d at $I_L = 30$ A. (a) ΔI_d versus ΔL_d and t_r at $s = 0$, (b) Δi_d versus ΔL_d and f, (c) mapped Δi_d versus f at $t_r = 25$ ns, and (d) mapped Δi_d versus f at $t_r = 50$ ns.

Similarly, considering the influence of mismatched L_s, the drain currents in (2) can be written as

$$\begin{cases} i_{d1} = g_{m1}(v_{gs} - v_{s1} - V_{th1}) \\ i_{d2} = g_{m2}(v_{gs} - v_{s2} - V_{th2}) \end{cases}, \quad (12)$$

where $v_{s1} = L_{s1}di_{d1}/dt$ and $v_{s2} = L_{s2}di_{d2}/dt$ are the induced voltages by common source inductances of the SiC MOSFET devices. If the threshold voltage and transconductance are matched ($V_{th1} = V_{th2} = V_{th}$, $g_{m1} = g_{m2} = g_m$), (12) can be simplified to

$$\Delta L_s\frac{di_{d1}}{dt} + L_{s2}\frac{d\Delta i_d}{dt} = -\frac{1}{g_m}\Delta i_d\,, \quad (13)$$

where $\Delta L_s = L_{s1} - L_{s2}$. Transient imbalance current can be derived as

$$\Delta i_d(\Delta L_s) = -\frac{g_m I_L}{2t_r(g_m L_{s2}s + 1)}\Delta L_s\,. \quad (14)$$

Similar to (11), the maximum value of transient imbalance current appears at $s = 0$, which can be expressed as

$$\Delta I_d(\Delta L_s) = \Delta i_d\big|_{s=0} = -\frac{g_m I_L}{2t_r}\Delta L_s\,. \quad (15)$$

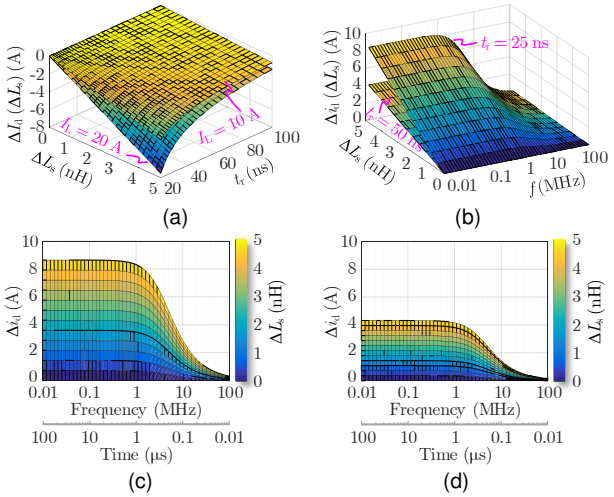

Fig. 7. Imbalance current affected by mismatched L_s at $I_L = 30$ A. (a) ΔI_d versus ΔL_s and t_r at $s = 0$, (b) Δi_d versus ΔL_s and f, (c) mapped Δi_d versus f at $t_r = 25$ ns, and (d) mapped Δi_d versus f at $t_r = 50$ ns.

In the condition of $L_{s2} = 7.5$ nH and $g_m = 2.4$ S, the impact of mismatched L_s is illustrated in Fig. 7. Compared (14) to (10),

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because $1/g_m > R_{dson}$, the imbalance current caused by ΔL_s is smaller than that by ΔL_d.

C. Impact of Unequal Junction Temperatures

Electrical characteristics of SiC MOSFETs are highly temperature-dependent. The asymmetrical layout of parallel SiC MOSFETs on a heat-sink or DBC results in unequal thermal resistances and junction temperatures. Based on (2), how temperature affects the drain current through the temperature-dependent g_m and V_{th} can be derived, which can be expressed as

$$\frac{\partial i_d}{\partial T_j} = (v_{gs} - V_{th})\frac{\partial g_m}{\partial T_j} - g_m \frac{\partial V_{th}}{\partial T_j}, \tag{16}$$

where T_j is the junction temperature of the SiC MOSFET. The transient imbalance current, caused by the junction temperature difference ΔT_j of parallel SiC MOSFETs, can be derived as

$$\Delta i_d(\Delta T_j) = \frac{\partial i_d}{\partial T_j}\Delta T_j. \tag{17}$$

The typical temperature-dependent g_m and V_{th} of the SiC MOSFET device C2M0080120D can be expressed as [38]

$$\begin{cases} V_{th} = 2.71 - 6.37\times10^{-3} T_j \\ g_m = 2.39 + 1.62\times10^{-2} T_j \end{cases}. \tag{18}$$

According to (16)–(18), Fig. 8 demonstrates the transient imbalance current caused by unequal junction temperatures, in case of $V_{th} = 2.7$ V, $g_m = 2.4$ S, $T_j = 25$ °C, and $I_L = 30$ A. It can be found that the imbalance current Δi_d increases with ΔT_j and v_{gs}. Big V_{th} is helpful to suppress the transient imbalance current. Besides, it is evident that the transient imbalance current has a positive temperature-dependent coefficient, which may lead to thermal runaway among parallel SiC MOSFETs and cause damages.

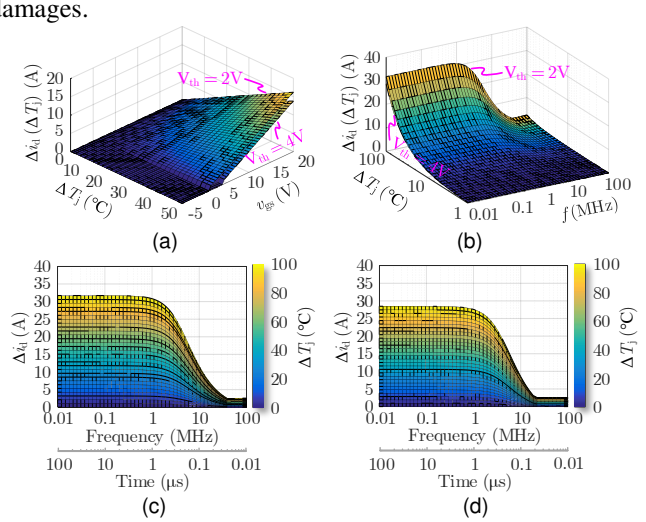

Fig. 8. Imbalance current affected by unequal T_j at $I_L = 30$ A. (a) Δi_d versus ΔT_j and v_{gs}, (b) Δi_d versus ΔT_j and f, (c) mapped Δi_d versus f at $V_{th} = 2$ V, and (d) mapped Δi_d versus f at $V_{th} = 4$ V.

According to the before mentioned mechanisms of imbalance current, multiple inevitable electro-thermal factors jointly result in the imbalance current among parallel SiC MOSFETs, it is difficult to eliminate all these factors. Therefore, some auxiliary circuits should be addressed to suppress the imbalance current.

IV. Proposed DMC Method for Imbalance Current Suppression

A. Physic Concept of the Proposed DMC

Schematic diagram of the DMC is illustrated in Fig. 9. As shown in Fig. 9(a), the balance load current is common mode current, and the magnetic flux density B_c in the core is zero. i_{d1} and i_{d2} are affected by leakage inductance caused by leakage magnetic flux density B_a in the air. As depicted in Fig. 9(b), the imbalance current is differential mode current, and it activates the B_c. The corresponding magnetizing inductance is big enough to limit the imbalance current.

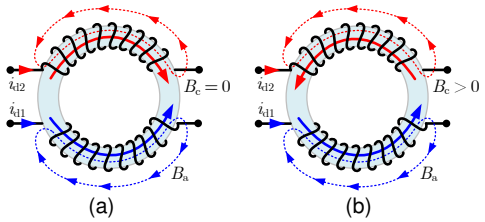

Fig. 9. Magnetic flux densities of DMC induced by (a) balance current $i_{d1} = i_{d2}$ and (b) imbalance current $i_{d1} > i_{d2}$.

From the viewpoint of impedance, the imbalance current, caused by the before mentioned impact factors, can be modeled as

$$\Delta i_d = v_{ds}/Z_1 - v_{ds}/Z_2 = v_{ds}(Z_2 - Z_1)/Z_1 Z_2, \tag{19}$$

where Z_1 and Z_2 are equivalent impedances in parallel branches.

Operation principles of the DMC to suppress imbalance current can be characterized as 4 dynamic intervals, as illustrated in TABLE II and Fig. 10.

(1) *Interval 1:* At the beginning, assuming $Z_1 = Z_2$, so $i_{d1} = i_{d2}$, currents of parallel SiC MOSFETs are balanced.

(2) *Interval 2:* If $Z_1 \neq Z_2$, for instance, $Z_1 < Z_2$, the corresponding imbalance current in (19) circulates between the parallel branches, i.e., $i_{d1} > i_{d2}$ in Fig. 10.

(3) *Interval 3:* According to the dot convention of DMC, the induced voltages in parallel branches are opposite (i.e., v_m and $-v_m$ in Fig. 10, where $v_m = L_m \mathrm{d}\Delta i_d/\mathrm{d}t$).

(4) *Interval 4:* Induced voltages regulate the imbalance current (i.e., $i_{d2}\uparrow$, $i_{d1}\downarrow$, $\Delta i_d \to 0$) until the currents are balanced again.

TABLE II
INTERVALS DURING IMBALANCE CURRENT SUPPRESSION

Interval 1	Currents are balance, $i_{d1} = i_{d2}$
Interval 2	Currents are imbalance, i.e. $i_{d1} > i_{d2}$
Interval 3	Due to induced voltage v_m, i_{d1} decreases and i_{d2} increases
Interval 4	Currents are balance again

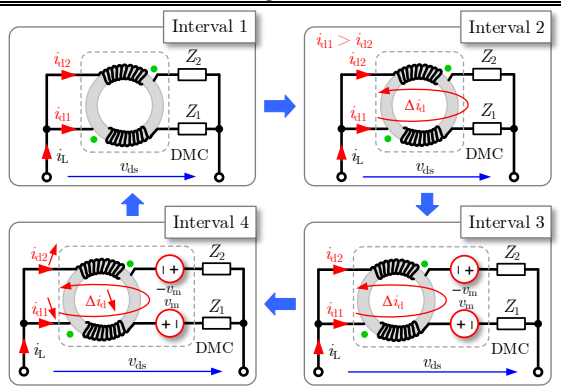

Fig. 10. Schematic diagram for imbalance current suppression by DMC.

It should be noted, by using the DMC to suppress imbalance current, one winding observes energy $P_{in} = v_m \Delta i_d$ and converts electric energy to magnetic energy. However, the other winding generates energy $P_{in} = -v_m \Delta i_d$ and converts magnetic energy to electric energy. Therefore, DMC utilizes magnetic flux as a media to transfer current from one branch to the other, and it can eliminate the imbalance current without energy loss in ideal condition.

B. Theory Foundation of the Proposed DMC

(1) *Mathematical Models of the Proposed DMC Method*

Fig. 11(a) demonstrates a test rig for current sharing of parallel SiC MOSFETs by incorporating the DMC. According to the configuration of the DMC by using sectional winding in Fig. 11(b), the magnetic flux density B_c in the core caused by the transient imbalance current can be expressed as

$$B_c = 2n\mu_r\mu_0 \frac{i_{d1} - i_{d2}}{\pi(D_{max} + D_{min})} = \frac{2n\mu_r\mu_0}{\pi(D_{max} + D_{min})} \Delta i_d , \tag{20}$$

where n is the turns of winding, μ_0 and μ_r are the vacuum permeability and relative permeability, respectively. D_{max} and D_{min} are external and inner diameters of the core. The leakage magnetic flux density B_a in the air can be expressed as

$$B_a = n\mu_r\mu_0 i_d / l . \tag{21}$$

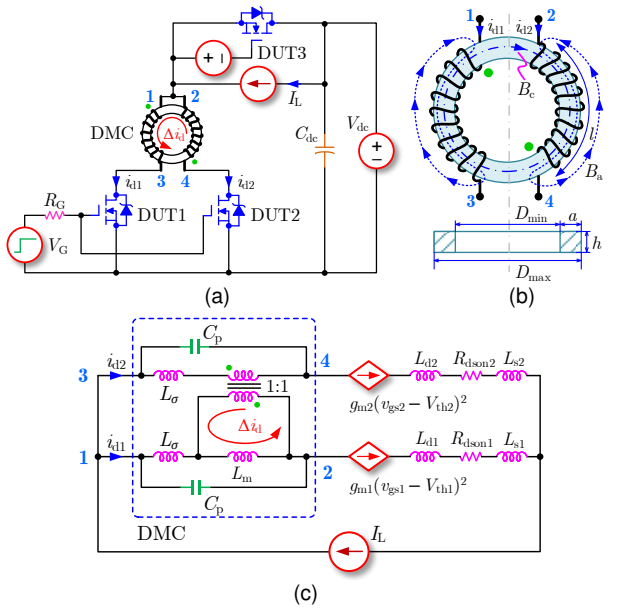

Fig. 11. Test rig for parallel SiC MOSFETs. (a) Schematic of test rig, (b) structure of DMC, and (c) equivalent circuit of test rig.

Fig. 11(c) indicates the schematic diagram of DMC. Equivalent parallel capacitance (EPC) C_p is caused by the stray capacitor of DMC winding. It might result in ringing during turn-on and -off, but it does not influence the current-sharing performance. The EPC can be minimized by using optimized winding patterns.

In Fig. 11(c), the magnetic inductance L_m and leakage inductance L_σ of the DMC can be expressed as

$$\begin{cases} L_m = \dfrac{nB_cS}{\Delta i_d} = \mu_r\mu_0 \dfrac{2n^2S}{\pi(D_{max} + D_{min})} , \\ L_\sigma = nB_aS / i_d = n^2\mu_0 S / l \end{cases} \tag{22}$$

where $S = ah = 0.5(D_{max} - D_{min})h$ is the cross-sectional area of the core; l is the length of winding, as shown in Fig. 11(b). It should be noted L_σ is determined by the leakage magnetic flux density and can be eliminated by using advanced winding structure.

(2) *Operation Principles of the Proposed DMC Method*

Ignoring the EPC, based on the proposed DMC suppression solution, according to the schematic diagram in Fig. 11(c), controlled currents in parallel branches satisfy

$$\begin{aligned} &(L_\sigma + L_{d1} + L_{s1})\frac{di_{d1}}{dt} + L_m \frac{d\Delta i_d}{dt} + R_{dson1} i_{d1} \\ &= (L_\sigma + L_{d2} + L_{s2})\frac{di_{d2}}{dt} - L_m \frac{d\Delta i_d}{dt} + R_{dson2} i_{d2} \end{aligned} . \tag{23}$$

If $R_{dson1} = R_{dson2} + \Delta R_{ds}$, (23) can be simplified to

$$\begin{aligned} &(2L_m + L_\sigma + L_{d2} + L_{s2})\frac{d\Delta i_d}{dt} + (\Delta L_d + \Delta L_s)\frac{di_{d1}}{dt} \\ &+ R_{dson2}\Delta i_d + \Delta R_{ds} i_{d1} = 0 \end{aligned} . \tag{24}$$

Therefore, according to (24), Δi_d can be expressed as

$$\Delta i_d = -\frac{\Delta R_{ds} + (\Delta L_d + \Delta L_s)/t_r}{(2L_m + L_\sigma + L_{d2} + L_{s2})s + R_{dson2}} \frac{I_L}{2} . \tag{25}$$

It can be seen Δi_d increases with I_L. To avoid saturation of DMC, the DMC core material and winding turns should be optimally designed. In dynamic state, $s \neq 0$, because $L_m >> L_\sigma + L_{d2} + L_{s2}$, the high-frequency transient imbalance current Δi_d is mainly limited by L_m. In steady-state, $s = 0$, (25) can be simplified to

$$\Delta i_{dmax} = \Delta i_d\big|_{s=0} = -\frac{\Delta R_{ds} + (\Delta L_d + \Delta L_s)/t_r}{R_{dson2}} \frac{I_L}{2} . \tag{26}$$

The maximum imbalance current Δi_{dmax} is theoretically determined by the equivalent impedance $\Delta R_{dson} + (\Delta L_d + \Delta L_s)/t_r$.

According to (25), the ratio of imbalance current, which is defined as γ, can be expressed as

$$\gamma = \frac{\Delta i_d}{I_L/2} = -\frac{\Delta R_{ds} + (\Delta L_d + \Delta L_s)/t_r}{(2L_m + L_\sigma + L_{d2} + L_{s2})s + R_{dson2}} . \tag{27}$$

In the condition of $\Delta L_d = \Delta L_d = 2$ nH, $L_\sigma = 1$ nH, and $\Delta L_d = 10$ nH, the γ greatly decreases with the increased L_m, as indicated in Fig. 12(a). However, big L_m also means bulk volume, heavy weight, and more cost. Therefore, there is a trade-off to determine L_m.

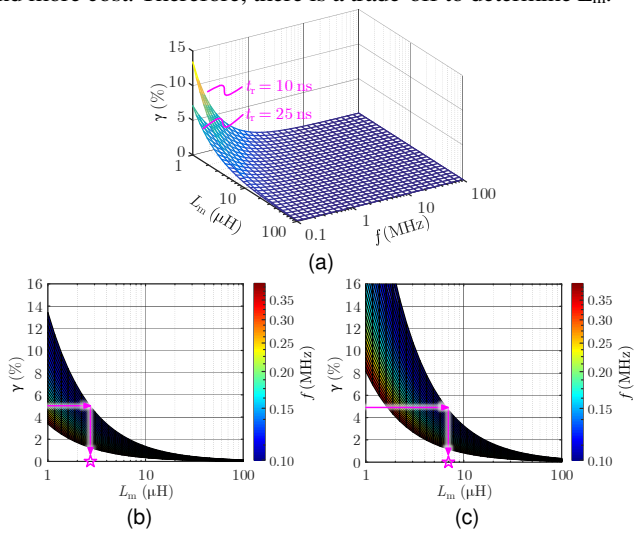

Fig. 12. Transient imbalance current ratio limited by L_m. (a) γ versus L_m and f, (b) mapped γ and L_m at $t_r = 25$ ns, and (c) mapped γ and L_m at $t_r = 10$ ns.

Fig. 12(a) can be mapped as Fig. 12(b) and Fig. 12(c), the relationship between γ and L_m can be expressed by a nonlinear function $L_m = F_\gamma(\gamma, f, t_r)$. As long as the expected γ is determined, the designed L_m can be found in Fig. 12(b) and Fig. 12(c). For

example, in the condition of $t_r = 25$ ns, if the ratio of imbalance current is set as $\gamma = 5\%$, the minimum L_m should be 2 μH to meet the desired γ according to Fig. 12(b). As indicated in Fig. 12(c), to guarantee the same γ in the scenario of faster di/dt, the minimum L_m should be 7 μH in the condition of $t_r = 10$ ns.

As mentioned before, it can be found magnetic flux density in the core is the main contributor to limit imbalance current, while leakage magnetic flux density should be minimized to limit parasitic inductance and attenuate switching ringing.

C. Design Guidelines of the Proposed DMC

To optimally design the DMC for imbalance current suppression, some criteria should be fulfilled: high-frequency material, proper winding turns, enough operation magnetic flux density, and optimal winding structure. Some practical design guidelines of DMC are presented step-by-step as follows.

(1) *Step 1: Selecting Materials of Core and Wire*

Targeting at high-frequency application, AlSiFe based metallic powder core is preferred for the DMC to reduce the loss caused by eddy-current and hysteresis effect. Besides, Litz wire is recommended for the windings to reduce the loss caused by skin effect and proximity effect.

(2) *Step 2: Calculating Winding Turns* (n)

Winding turns n is determined by the expected L_m which decided by the map between γ and L_m in Fig. 12. According to (22), the numerical calculation of minimum turns n can be derived as

$$n = \sqrt{\frac{\pi(D_{max} + D_{min})L_m}{\mu_r \mu_0 (D_{max} - D_{min})h}} . \tag{28}$$

In practice, turns can be chosen as the minimum integer larger than the calculated n in (28).

(3) *Step 3: Determining Operation Magnetic Flux Density* (B_{op})

B_{op} is determined by the maximum imbalance current to be handled, which can be expressed as

$$B_{op} = \frac{2n\mu_r\mu_0}{\pi(D_{max} + D_{min})} \Delta i_{dmax} . \tag{29}$$

B_{op} is limited by the saturation magnetic flux density of core. To avoid the saturation of DMC, B_{op} should not larger than the saturation magnetic flux density B_{sat} of the core material, $B_{op} \leq B_{sat}$, and it can be derived that

$$\varepsilon = (B_{sat} - B_{op})/B_{sat} , \quad \varepsilon \in [0, 1] , \tag{30}$$

where ε is a coefficient to quantify the margin of reserved magnetic flux to resist the saturation of DMC in extreme load conditions.

(4) *Step 4: Optimizing Winding Pattern*

To avoid turn-off over-voltage caused by DMC, leakage inductance L_σ of the DMC should be minimized. Besides, the EPC may activate switching ringing, and it should be minimized. These issues can be achieved by using an optimal winding pattern.

Sectional and bifilar windings are the commonly used windings, as shown in Fig. 13. Compared with the sectional winding, currents in bifilar winding flow in opposite directions. Therefore, the magnetic field created by one winding is equal and opposite to that created by the other. Thus, leakage magnetic flux density and leakage inductance of the DMC can be reduced by using bifilar winding. Besides, bifilar winding performs lower EPC because the distance between successive turns is greater than sectional winding.

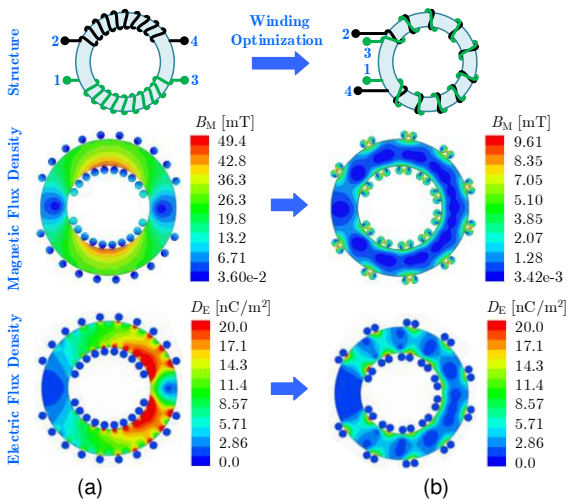

Fig. 13. Comparison of electromagnetic fields in DMC by using (a) sectional winding and (b) bifilar winding.

The electromagnetic fields of the DMC with specific winding patterns at $I_L = 30$ A are virtualized by using finite element analysis (FEA) tool Maxwell, as depicted in Fig. 13. Compared with sectional winding, the magnetic flux density (B_M) of DMC by using bifilar winding is remarkably reduced as desired. Besides, the electric flux density (D_E) of DMC by using bifilar winding is much smaller than that by using sectional winding. As a result, thanks to the minimized leakage inductance and EPC, bifilar winding is recommended for the DMC to reduce turn-off over-voltage and switching ringing.

(5) *Design Case of the DMC*

It should be noted, like all magnetic components, trial and error method may be used to design the DMC. To better understand the DMC, a design example is provided:

Step 1: Choosing AlSiFe core CS229125 ($\mu_r = 125$, $B_{sat} = 1.05$ T, $D_{max} = 23$ mm, $D_{min} = 14$ mm, $h = 7.62$ mm) and Litz wire (100 strands and cross-area 0.78 mm^2) as DMC materials.

Step 2: As illustrated in IV.B, based on the trade-off between current-sharing performance and volume, γ is set as 5%, and L_m is selected as 9 μH according to Fig. 12. Winding turns are derived as $n = 10$ according to (28).

Step 3: To handle $\Delta i_{dmax} = 20$ A, according to (29), B_{op} is calculated as 0.54 T, which is much smaller than B_{sat}. Margin coefficient ε approximates to 50%. Thus, sufficient margin is reserved to avoid saturation of DMC in extreme load conditions.

Step 4: Bifilar winding is implemented to reduce L_σ and EPC as small as possible.

V. Experimental Validations

To confirm the performance of the proposed DMC-based suppression method, an inductor-clamped double-pulse test (DPT) platform is set up, as shown in Fig. 14(a). Parallel SiC MOSFETs C2M0080120D are employed as DUTs. Facilities utilized in the test rig are listed in TABLE III. A TI TMS320F28335 DSP control board is used to generate the gate pulses. DMC prototypes with different windings patterns are made as shown in Fig. 14(b). Overall test conditions are selected as $V_{dc} = 600$ V, $I_L = 20$ A, $R_G = 20\,\Omega$, $V_G = 20/-5$ V, and $L = 560$ μH.

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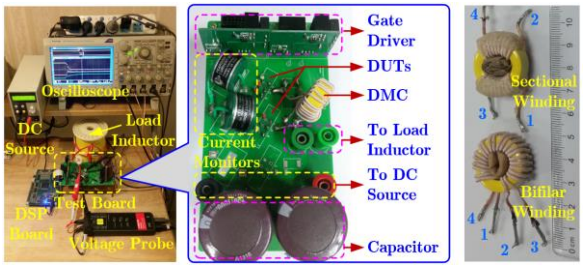

Fig. 14. Experimental set-up. (a) Schematic diagram of test rig and (b) prototypes of DMC by using different winding patterns.

TABLE III
FACILITIES USED IN TEST RIG

Facilities	Type	Bandwidth	Function
Digital oscilloscope	Tektronix DPO3054	500 MHz	Capture curves
Current monitor	Pearson 2877	200 MHz	Measure $i_{\rm d}$
Passive voltage probe	Tektronix P6139A	500 MHz	Measure $v_{\rm gs}$
Differential voltage probe	Cybertek DP6150B	200 MHz	Measure $v_{\rm ds}$

As mentioned in Section IV, due to the leakage inductance and EPC, performances of the DMC highly depend on the winding pattern. Commonly used sectional and bifilar windings are fabricated and evaluated, as illustrated in Fig. 15. By using sectional winding of DMC, due to the non-optimized leakage-inductance and EPC, the resonant frequency of drain current and drain-source voltage approximates 10 MHz, which is much smaller than that by using bifilar winding (nearly 20 MHz). Thanks to the minimized parasitics, bifilar winding can effectively reduce the ringing during turn-on and -off. Besides, compared with sectional winding, the peak value of imbalance current ratio γ is reduced from 40% to 7% by using bifilar winding. It is proved the bifilar winding can achieve better current-sharing performance and reduce switching ringing, compared with the sectional winding.

Different test conditions are further compared, including without solution, with series resistors, and with DMC. Experimental results are depicted in Fig. 16.

In condition of no current-sharing solution, Fig. 16(a) illustrates the measured on-off trajectories of parallel SiC MOSFETs. As mentioned in Section III, the maximum imbalance current occurs at the end of turn-on or -off processes. With the help of series resistors 1 Ω inserted in the parallel branches, Fig. 16(b) demonstrates that the static imbalance current can be suppressed. However, because the utilized series resistors cannot affect the on-off trajectories of SiC MOSFETs, the transient imbalance current remains. By implementing the DMC with bifilar winding, both the transient and static imbalance currents are greatly suppressed, as indicated in Fig. 16(c).

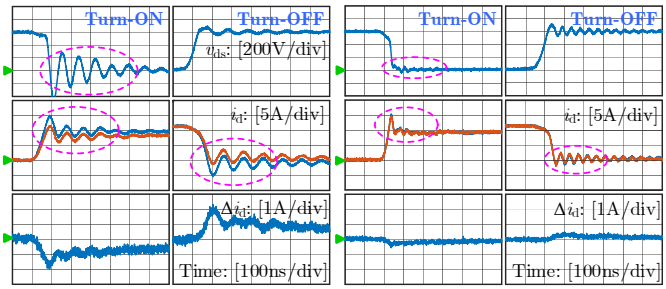

Fig. 15. Experimental results for different winding patterns. (a) Sectional winding and (b) bifilar winding.

Key characteristics of the experimental waveforms in Fig. 16 are quantified in TABLE IV. Thanks to the DMC, behaviors of parallel SiC MOSFETs approximately keep the same, including current curves, turn-on loss $E_{\rm on}$, turn-off loss $E_{\rm off}$, peak current $i_{\rm dmax}$, turn-off loss $E_{\rm off}$, current rise time $t_{\rm ir}$, current fall time $t_{\rm if}$, voltage rise time $t_{\rm vr}$, voltage fall time $t_{\rm vf}$, and maximum voltage $v_{\rm dsmax}$. Trajectories of parallel SiC MOSFETs are forced to be synchronized and consistent. Benefit from the minimized leakage inductance by using bifilar winding, DMC nearly increases the peak value of voltages $v_{\rm ds}$ during turn-off. By using the DMC, the ratio of imbalance current is reduced from 28% to 6%. Compared with the scenario without suppression, peak value of load current is reduced from 18.8 A to 17.6 A by using the DMC. That is to say, the peak value of drain current is decreased by (18.8 – 17.6)/17.6 = 7%, which is helpful to promote the safety of parallel SiC MOSFETs. By using DMC, the dv/dt of SiC MOSFET decreases and its switching loss slightly increases, compared with the scenario by using series resistors.

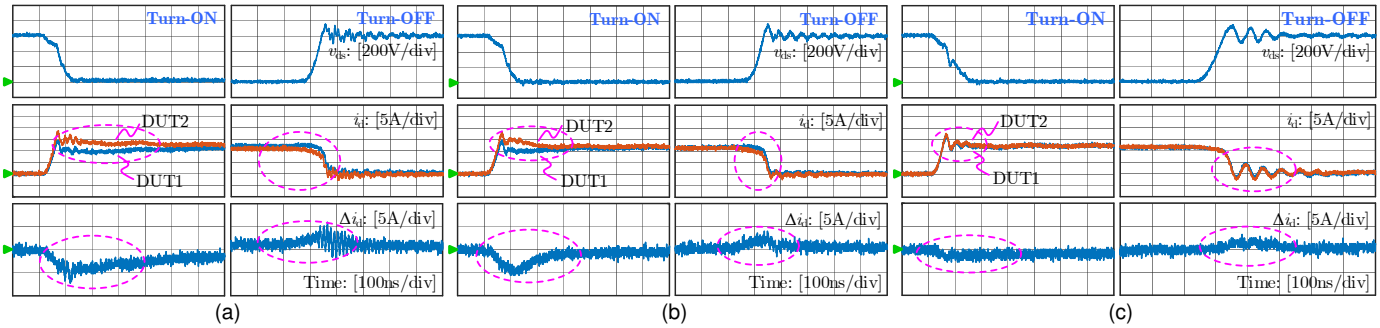

Fig. 16. Experimental results (a) without solution, (b) with series resistors suppression method, and (c) with the proposed DMC method.

TABLE IV. COMPARISON OF EXPERIMENTS IN DIFFERENT CASES

Condition	Device	Turn-on				Turn-off				
		$E_{\rm on}$ (μJ)	$i_{\rm dmax}$ (A)	$t_{\rm ir}$ (ns)	$t_{\rm vf}$ (ns)	$E_{\rm off}$ (μJ)	$i_{\rm dmax}$ (A)	$t_{\rm if}$ (ns)	$t_{\rm vr}$ (ns)	$v_{\rm dsmax}$ (V)
Without solution	DUT1	368	14.4	36.4	86.8	502	13.6	45.6	58.4	760
	DUT2	474	18.8	41.6		378	12.4	59.6		
With series resistor	DUT1	444	14.8	36.4	90.4	470	13.2	36.4	55.2	760
	DUT2	544	18.4	39.6		367	12.8	77.2		
With DMC	DUT1	506	17.6	37.2	95.8	495	12.8	67.4	66.8	750
	DUT2	509	17.6	38		498	12.8	67.6		

Fig. 17 further demonstrates the comparative experiments in conditions of different load currents. As seen, with series resistors, the transient imbalance current cannot be suppressed. The imbalance current increases with the load current, especially in the turn-on process. In contrast, with the DMC, the

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turn-on and -off trajectories of the parallel SiC MOSFETs are consistent.

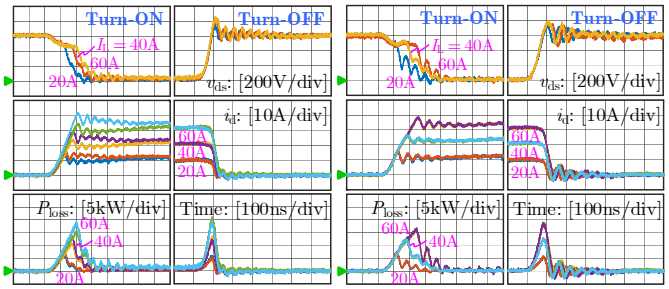

Fig. 17. Experimental results at different load currents. (a) With series resistors and (b) with the proposed DMC.

The trajectories of v_{ds} and i_d during turn-on and -off processes are demonstrated in Fig. 18. It can be found that, compared with the inserted series resistors, the imbalance current between parallel SiC MOSFETs can be effectively suppressed by the DMC.

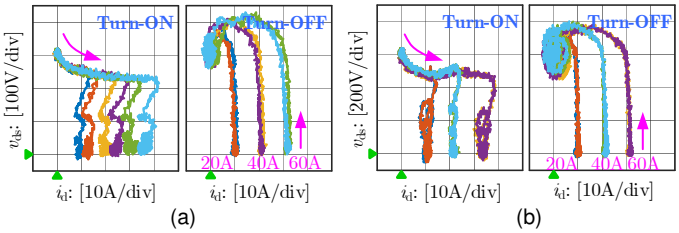

Fig. 18. Measured on-off trajectories of SiC MOSFETs at different load currents. (a) With series resistors and (b) with the proposed DMC.

To confirm the capability of proposed DMC, comparative experiments by using different gate resistances between 2.5 Ω and 51 Ω are achieved, as depicted in Fig. 19. Small gate resistance can elevate the switching speed and di/dt of SiC MOSFET. In Fig. 19(a), without suppression solution, decreasing gate resistance will increase imbalance current, as analyzed in Section III. Both static and dynamic imbalance currents can be well suppressed by the proposed DMC, as displayed in Fig. 19(b).

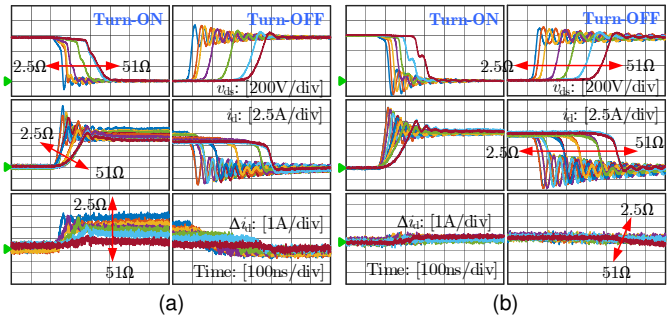

Fig. 19. Experimental results at different gate resistances. (a) Without solution and (b) with the proposed DMC.

Considering the influence of junction temperature difference ΔT_j of parallel SiC MOSFETs between 0°C and 25°C, experiment results are presented as shown in Fig. 20 in the condition of $R_g = 5$ Ω. In the test bench, one device is soaked in ambient temperature environment and the other one is heated by hotplate. Without suppression solution, the temperature difference mainly affects the turn-off processes. The peak value of transient imbalance current increases with the temperature difference. Because the on-resistance R_{dson} is not sensitive to temperature, the static imbalance current is nearly affected by the temperature. It can be seen the current-sharing performance of DMC-based suppression is very robust to the temperature difference.

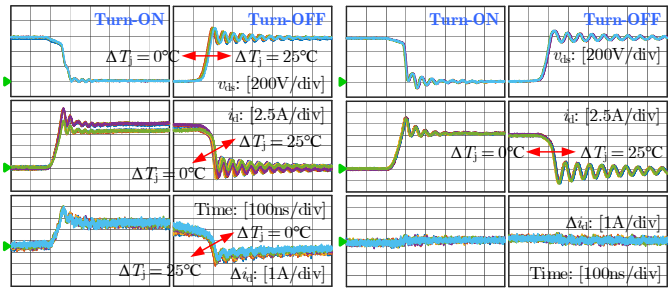

Fig. 20. Experimental results at different junction temperature differences. (a) Without solution and (b) with the proposed DMC.

According to the experiments in Fig. 16 to Fig. 20, a full comparison of studied solutions for imbalance current suppression is conducted as listed in TABLE V. The inserted series resistors cannot suppress the transient imbalance current, while the incorporated DMC can effectively suppress the transient and static imbalance current. The possible turn-off over-voltage and switching ringing, caused by the leakage-inductance and EPC of the DMC, can be overcome by using the optimized bifilar winding. The series resistors will result in remarkable power loss and reduce the efficiency of converters. Due to the excellent current-sharing capability of the DMC, the current rating of parallel SiC MOSFET, limited by imbalance current, can be expanded. The volume, size, and cost of the DMC are slightly larger than the resistor. However, considering the perfect current-sharing capability, the proposed DMC is a more cost-effective solution in general.

TABLE V
COMPARISON OF SERIES RESISTOR AND DMC

Indices	Series Resistor	Proposed DMC
Static imbalance current suppression	■	■
Dynamic imbalance current suppression	□	■
Current rating improvement	■	■
Transient over-voltage	□	□
Energy loss of auxiliary circuit and MOSFETs	■	■
Size,volume, and cost	■	■

Note: ■ ■ ■ □ ■ ■ ■ (Worse ← → Better)

VI. EXTENSION AND COMPARISON

A. Extension of Proposed Suppression Approach

Scalability of methods for imbalance current suppression is very important. To extend the proposed method and adapt the scenario with more than two parallel devices, two geometries of DUTs and chokes are indicated in Fig. 21. Theoretically, the maximum number of parallel SiC devices can be infinite.

Concerning geometry 1 in Fig. 21(a), taking N-parallel SiC devices into account, primary windings of chokes are inserted into parallel branches. Secondary windings of chokes are series one-by-one. Primary windings flow through load current, while the secondary windings just carry imbalance current.

Concerning geometry 2 in Fig. 21(b), each SiC MOSFET branch contains two windings in series, and the device couples with two neighbor devices. Both primary and secondary windings of each DMC flow through load current.

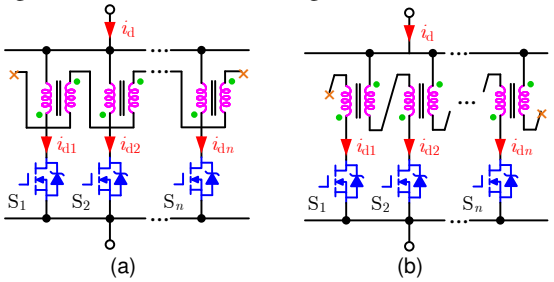

Fig. 21. Extension of proposed DMC-based suppression method to multiple parallel SiC MOSFETs. (a) Geometry 1 and (b) geometry 2.

It should be noted, the DMC also can be inserted into the source terminals of parallel devices, which is another alternatively effective way to implement the DMC.

B. Comparison With Existing Suppression Approaches

To further confirm the performance of the proposed DMC, based on existing methods for imbalance current suppression of parallel SiC MOSFETs, a comprehensive comparison is provided in Fig. 22 from viewpoints of electrical, safety, and economic indices. It can be seen that the proposed DMC approach is a low cost, fast dynamic, easy integration method for imbalance current suppression.

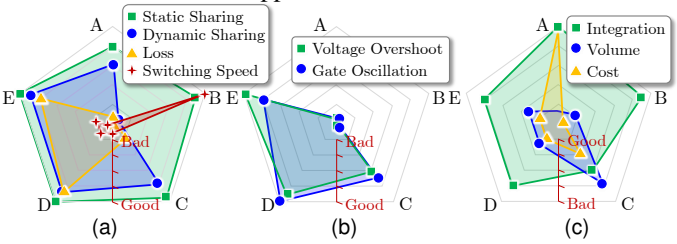

Fig. 22. Comparison of imbalance current suppression methods with respect to (a) electric indices, (b) safety indices, and (c) economic indices. A: DBC layout, B: series resistor, C: active gate driver, D: passive balancing, E: DMC.

VII. Conclusion

To suppress the imbalance current of parallel SiC MOSFETs, a DMC concept is proposed in this paper. In-depth mathematical mechanisms of the imbalance current are modeled. It is observed the imbalance current covers the normal operating frequency of SiC MOSFET, and it should be carefully addressed for the high-frequency application. The imbalance current is jointly influenced by inconsistent chips, asymmetrical layouts, and unequal junction temperatures, and it is hard to be overcome by changing the SiC MOSFET itself. Auxiliary DMC is utilized to suppress the imbalance current. Its effectiveness is confirmed by proposed operation principles, theoretical analyses, and design guidelines. Besides, it is recommended that bifilar winding is the best choice for the DMC in the proposed method to minimize the leakage inductance and EPC. Finally, the forced current-sharing capability of the proposed DMC based suppression method is ensured by extensive experiments, which also demonstrates the effectiveness of the proposed DMC method. Moreover, considering electrical, safe, and economic indices, comparative analyses for studied current-sharing approaches are presented, which demonstrates the merits of the proposed DMC, including low cost, fast dynamic, easy integration, etc. Concerning some abnormal conditions like cross-talk, short-circuit, avalanche, etc., the interactions mechanisms between DMC and SiC MOSFET should be further addressed in the near future.

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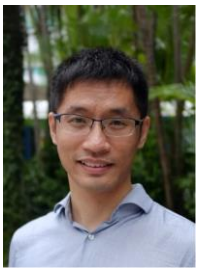

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