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Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs

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Abstract

The role of buffer traps (identified as C_N acceptors through current DLTS) in the off-state leakage and dynamic Ron of 650V rated GaN-on-Si power devices is investigated. The dynamic Ron is strongly voltage-dependent, due to the interplay between the dynamic properties of the C_N traps and the presence of space-charge limited current components. This results in a complete suppression of dyn Ron degradation under HTRB conditions between 420V and 850V.

Introduction

AlGaN/GaN based HEMTs are actively being researched as next generation power devices in the 100-650V range. A key concern inhibiting the widespread adoption in the market is their reliability, especially during long-term off-state stress at high temperature (HTRB), under which the 2DEG is depleted and the GaN stack behaves as a dielectric, with the threading dislocations serving as leakage paths. Voltage acceleration between 100V and 130V under HTRB condition has been observed for 100V GaN-on-Si devices [1]. The importance of the buffer epi stack for off-state stress of 600V GaN-on-Si devices is discussed in [2], but without reporting any voltage acceleration data or model.

In this paper, the role of space charge limited (SCL) buffer current in the dyn Ron and degradation under HTRB stress is discussed. No voltage-accelerated degradation under HTRB stress between 420V and 850V is observed, which is explained by the GaN buffer stack becoming resistive above a certain critical voltage (trap filling level V_{TFL}), allowing the trapped charge to leak away.

Results and Discussion

AlGaN/GaN-on-Si power devices are processed on 6 inch wafers. The devices are 100mΩ power transistors with a ~20A current rating, see Fig.1a for a device cross-section [3]. Growing GaN-on-Si results in ~10^9 cm^{-2} threading dislocations which serve as leakage paths through the buffer stack (Fig.1b). Fig. 2 shows the vertical leakage current through the GaN stack as a function of temperature. The J-V characteristic is typical for space-charge limited current (SLC), or the conduction in a dielectric through spillover from a metal [4]. V_{TFL} is the voltage at which the traps in the buffer are ionized, so the quasi- Fermi levels are de-pinned and move up to the band-edge, hence the steep increase in current with voltage ($J \sim V^n$ behavior). The very steep increase also has an impact ionization component [5]. The traps are identified using current DLTS, see Fig. 3, as C-atoms on a N-site at E_v+0.85eV [3]. Above V_{TLF}, the vertical field becomes large enough to stimulate field-enhanced Poole-Frenkel current conduction [5] which allows the charge in the C_N acceptors to leak away, see Fig. 2 and the proposed model in Fig. 5.

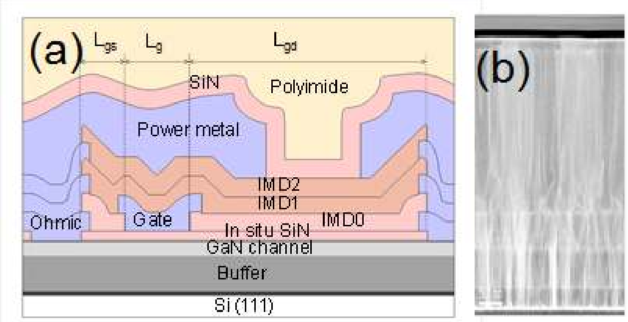

Fig. 1 : (a) Schematic cross-section of the AlGaN/GaN HEMT power transistor. (b) SEM cross-section of a typical GaN stack grown on Si. Note the high density of dislocations.

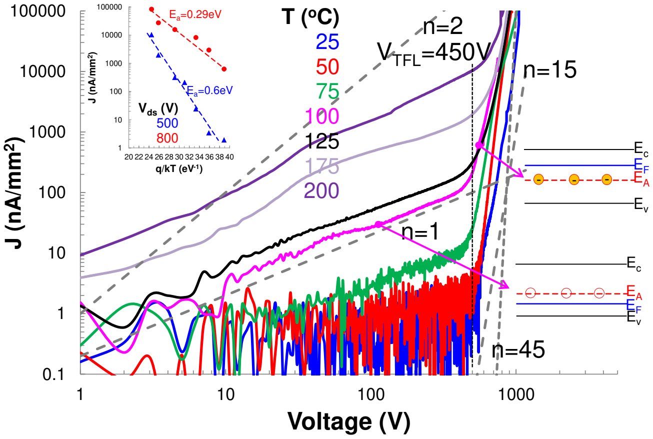

Fig.2 : ln(J)-ln(V) characteristic of the vertical leakage current as a function of temperature. The trap filling voltage V_{TFL} is the voltage at which all acceptor traps are ionized (see [4]), Note the Ohmic conduction (n=1) till $V=V_{TFL}$. Above V_{TFL}, the current through the buffer increases rapidly. Electrons are injected from the Si substrate by thermionic emission with E_a=0.6eV.

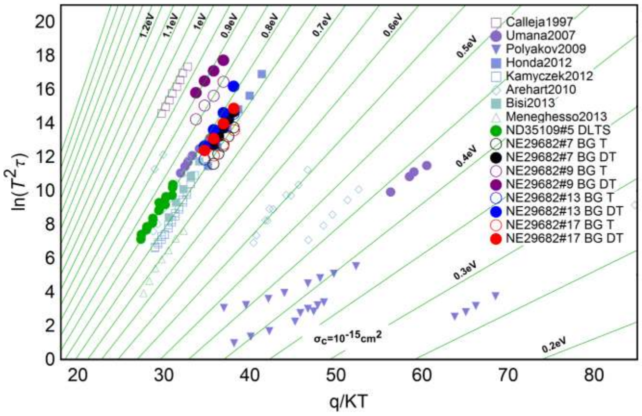

Fig. 3 : Trap-mapping, using current-DLTS. Comparison with literature suggest that the is a C-atom on a N-site (C_N), acceptor type, E_a=E_v+0.85eV. This is the trap responsible for the increase in Ron during HTRB (but also subsequent recovery). Full lines refer to E_a above the valence band, for a capture cross section $\sigma=10^{-15}$ cm^2

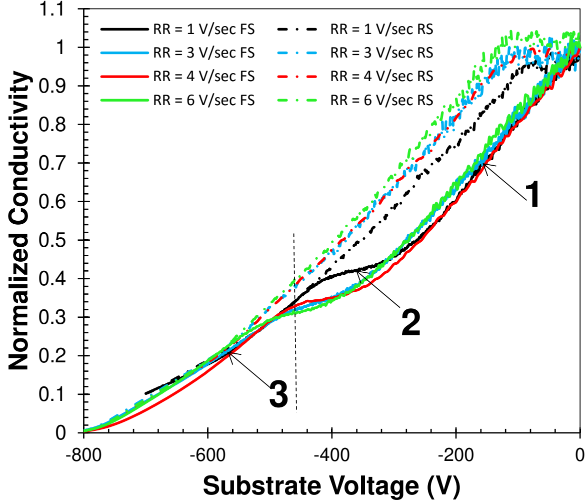

Fig. 4: Substrate ramp experiment, for different ramprates of the backgate voltage sweep. During "1", the buffer shows a capacitive behavior, during "2" charge redistribution occurs as the C-doped layer and UID layer starts to leak, during "3" the whole buffer is resistive [3].

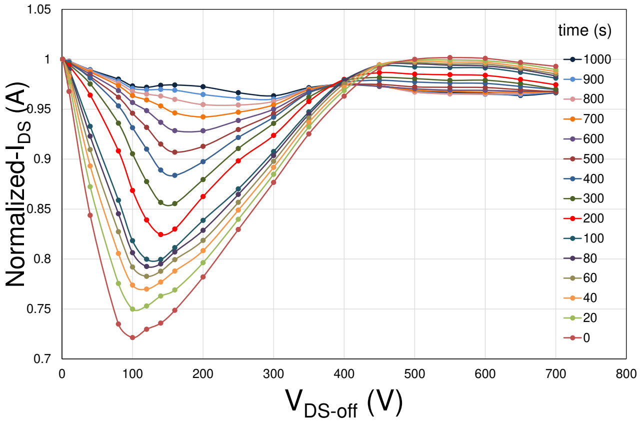

Fig 5 : Recovery of the on-state current as a function of relaxation time, after a 1000s trap filling pulsed at T=60ºC, up to V_{ds}=700V. Note that from 450V, insignificant dynamic Ron is observed. This voltage corresponds to V_{TFL} from Fig. 2.

As a result, the GaN buffer becomes resistive instead of capacitive, which is supported by substrate ramp experiments, see Fig. 4. By performing a negative voltage ramp on the Si substrate, the 2DEG conductivity decreases through capacitive coupling with some charge redistribution within the GaN:C layer (region "**1**" in the substrate ramp). As from ~-300V, the undoped layer under the 2DEG conducts, resulting in hole trapping and a constant field at the 2DEG. Hence the conductivity remains unaltered (region "**2**"). Finally, the complete buffer structure starts to leak and behaves as a resistor (region "**3**").

Fig. 5 shows the evolution of I_{DS} after a trap filling pulse of 1000s, as a function of recovery time and trap filling voltage. The minimum in I_{DS} at around 100-200V is associated with balancing positive and negative buffer charge storage[6], but above V_{ds}=450V, almost no static I_{DS} degradation is observed. To study the de-trapping kinetics, current DLTS at V_{ds}=200V and V_{ds}=500V is performed. Fig.6 shows the de-trapping Ron transients at T=100°C along with the proposed model, as well as the dynamic Ron (pulsed IV, t_{on}=20μs, t_{off}=2ms) from which the same effect is observed (dyn Ron is worst at 200V, and almost absent for V_{ds}>500V). The proposed model is that up to V_{ds}=V_{TFL}, charge redistribution (storage) occurs, but that for larger V_{ds} the current leaks away. This is supported by Figs.2, 4 and 6..

The de-trapping transient from the C_N traps seen in Fig. 6 has two time constants with the same activation energy of 0.9eV (not shown), which we have assigned to two different leakage paths: lateral and vertical. This is supported by TCAD simulations, shown in Fig. 7, plotting the potential distribution in the off-state at 200V (near worst case condition as from Fig.5), and after switching to the on-state as a function of switch-on time. In the ON state there is initially a strong vertical field until 1000s after which charge has redistributed vertically and giving the first time constant. Then the charge leaks away laterally to the source/drain giving the second time constant. This is reflected in two different time constants, as can be noticed from the simulated derivative of the drain current, see also Fig. 7.

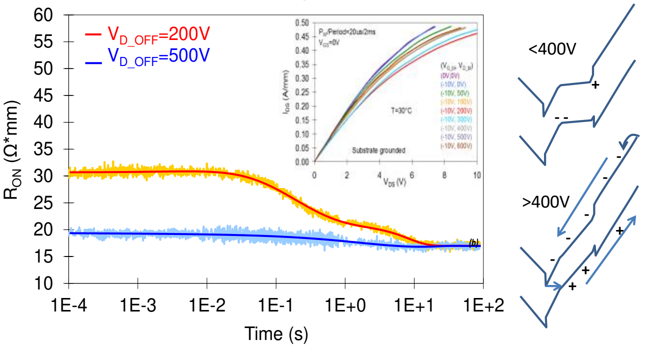

Fig. 6 : current DLTS spectra at T=100ºC, after a 100s trap filling pulse at 200V and 500V. The recovery has two time constants, attributed to one trap (C_N acceptor, E_a=E_v+0.85eV, see Fig. 3) which is emptied by a vertical and lateral leakage component, see Fig. 6. Insert : Pulsed I-V showing that dyn Ron is worst around 200V, and becomes better for higher voltage. At V=V_{TFL}, all traps are emptied and no net charge is stored any longer in the C_N traps.

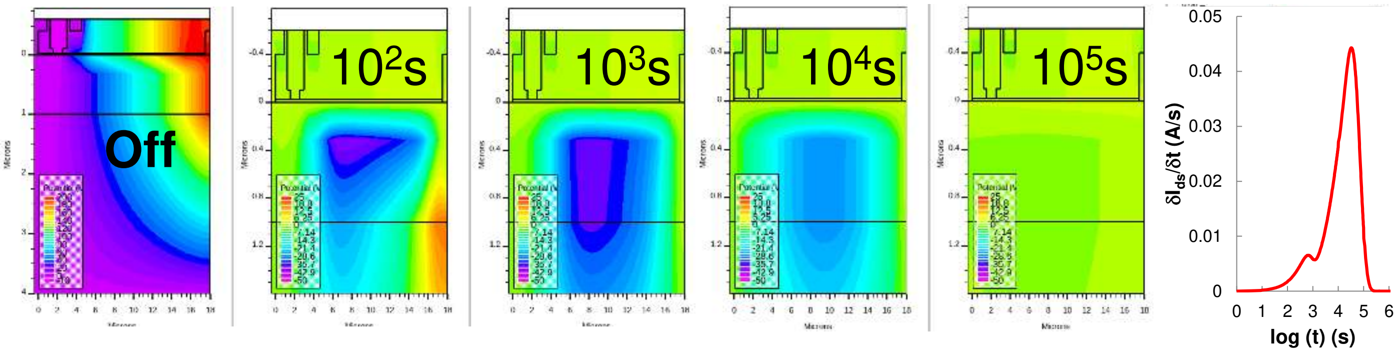

Fig. 7 : Simulated potential distribution in the device, after switching from off-state to on-state, for different recovery times. Off-state condition is V_{ds}=200V, scaling of the potential is from -10V to +200V. On-state plots after 10^2s, 10^3s, 10^4s and 10^5s after switch-on ; scaling of the potential is from -50V to +25V for better readability of the plots. The last graph shows the simulated derivative of the drain current during the on-state recovery. Two distinct time constants are observed, which correlate with a vertical and lateral leakage path for the charge stored in the C_N traps, at ~10^3s and 10^4s respectively.

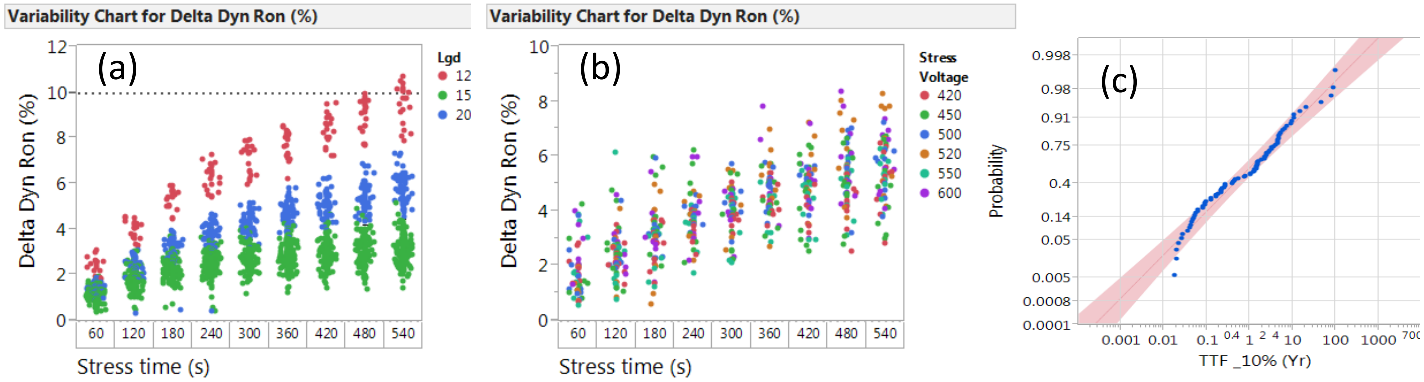

Fig. 8 : Measurements on 100mΩ power transistors at T=150°C. (a) dyn Ron increase measured as a function of HTRB stress time at V_{ds}=520V, for different Lgd. (b) dyn Ron increase as a function of HTRB stress time for L_{gd}=20µm, for stress voltages ranging from 420V to 600V. Dyn Ron is measured at the drain stress condition. (c) Time-to-fail for Dyn Ron at T=150°C, V_{ds}=520V failure criterion is 10% degradation in dyn Ron. Data are obtained by extrapolating the results of each device of Fig. 8(a) (L_{gd}=15µm only) using a ln(t) behavior.

Reliability

A. *High temperature reverse bias stress*

The model that above V_{TFL}, no net charge is stored in the C-doped GaN layer and the devices become insensitive to the trap dynamics, has important consequences for any reliability test that relies on voltage acceleration. We will focus on both the degradation of the "dynamic" Ron (measured 4ms after releasing the stress voltage) and "static" Ron (measured 30s after releasing the stress voltage). Fig.8a shows the degradation of dyn Ron at T=150°C, V_{ds}=520V, as a function of stress time for different L_{gd}. The slight increase in dyn Ron (following a ln(t) behavior, see also [1]) indicates that slightly more charge is trapped following the stress. Shorter L_{gd} gives better performance (total amount of trapped charge in the access region is smaller). However, for too short L_{gd}, the degradation becomes larger due to too high lateral field, indicating the subtle balance between device design and buffer epi design. Fig. 8b shows the data at T=150°C, for one L_{gd}, with different stress voltages. Between 420V and 600V no voltage acceleration is observed, in line with the model that above V_{TLF} no net charge is stored in the buffer stack. Fig. 8c shows the extrapolated time-to-fail at 10% degradation in dyn Ron using an ln(t) extrapolation. The devices show full recovery after 10^2 s at RT (not shown). These data suggest that for half of the population, the devices can be stressed at T=150°C for 1 year at V_{ds}=520V, with a shift in dyn Ron of less than 10%.

In a next step the power devices are stressed at T=150°C, from 500V up to 950V , see Fig. 9, showing the Ron as a function of stress time. Up to 800V, the Ron is stable (within 10%), but as from V_{ds}=900V, the Ron starts to increase and other mechanisms start to occur. However, removing the stress and letting the device relax for 16h results in almost full recovery (within less than 10% of the original value). Remarkably, even during the stress the Ron seems to recover, which can be best seen from the V_{ds}=950V stress data, but can also be noted from the V_{ds}=600V stress data.

B. *High voltage wearout*

Since the buffer stack behaves as a (leaky) dielectric, one can apply high voltage TDDB during which the stack is stressed in off-state at high voltage until failure. This so-called high voltage off-state stress (HVOS) consists in applying a high voltage to the drain of the large area power device, the substrate and the source are at ground, and the gate is in pinch-off. The drain leakage current is monitored during the stress, and the devices are stressed till failure. High voltage off-state stress on high voltage power transistors is reported in [7,8]. In [7], large area devices were stressed till failure at

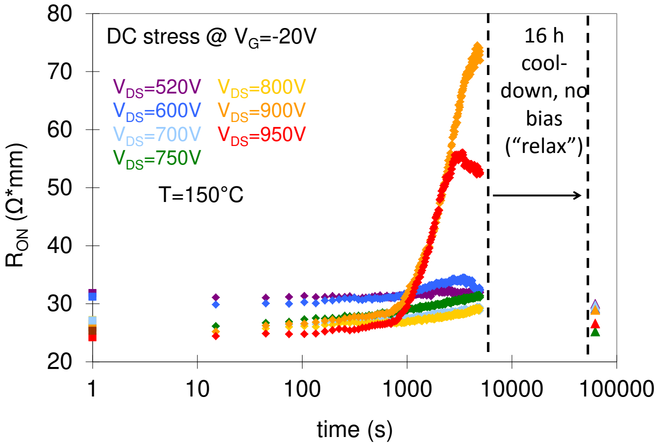

Fig. 9 : Ron as a function of stress time for different V_{ds_stress} conditions, from 520V up to 950 V. T=150°C. Stress is stopped after 6000s, after which the devices are cooled down ("relax"). Devices fully recover after 16h of relax, in line with the data of Fig. 6. Note the dynamics in the static Ron at V_{ds}=900 and 950V, showing a partial recovery even during the off-state stress.

RT, at V_{ds}=700V and V_{ds}=750V. In [8], large area power transistors were stressed at T=80°C, at V_{ds}=1100V and 1150V. An inverse power law was used for field acceleration.

Here large area power transistors (W>100mm) are stressed at V_{ds}=900V, 925V and 950V. The ambient temperature was increased until 200°C to induce failure of the buffer stack within a reasonable measurement time. The time-to-failure distributions at V_{ds}=900V, 925V and 950V are plotted on a Weibull plot in Fig.11. The data seem to follow a Weibull distribution (as expected), albeit that the distribution is bimodal. This is attributed to wafer variation and within wafer non-uniformities in the buffer stack itself. Three common field acceleration models are used to extrapolate the data to 600V : E, 1/E and Poole-Frenkel. The E-model is the most conservative model, but based on the data of Fig.2 and [5], the Poole-Frenkel model is selected. This yields a time-to-fail of 10 days at 600V, at T=200°C at the 100ppm level.

Conclusions

The vertical current through the GaN buffer stack of 650V rated GaN-on-Si power devices is found to be a SCL current. From a certain voltage (V_{TFL}), the buffer structure behaves resistively, and no net charge is stored any longer in the buffer traps (identified as C_N acceptors through current DLTS). This has important consequences for the off-state leakage, dynamic Ron and any voltage accelerated reliability test. The dynamic Ron is strongly voltage-dependent, due to the interplay between the dynamic properties of the C_N traps and the presence of space-charge limited current components with a complete suppression of dyn Ron degradation above V_{TLF}. Under HTRB stressing, no voltage accelerating is observed between 420V and 850V. Stressing the buffer structure till failure (TDDB) yields a Weibull distributed time-to-fail, with a Poole-Frenkel field acceleration model.

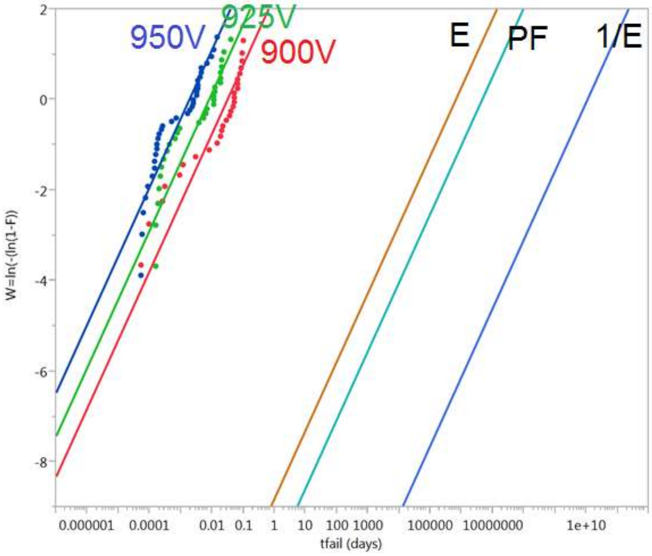

Fig. 10 : High voltage off-state stress at T=200°C, on 100mΩ power transistors, at V_{ds}=900, 925 and 950V. Data are plotted on a Weibull plot, three different extrapolation models are used : E, 1/E and Poole-Frenkel. Field extrapolation for the three models is done at T=200°C, V_{ds}=600V.

Acknowledgments

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