# Impact of Channel Doping on DG-MOSFET Parameters in Nano Regime-TCAD Simulation

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## ABSTRACT
Double gate MOSFET is one of the most promising and leading contender for nano regime devices. In this paper we investigate the impact of channel engineering on double gate MOSFET by using different channel doping. Sentaurus TCAD simulator is used to analyze the channel engineering of double gate MOSFET. It is observed in the results that we can change the threshold voltage by changing the channel doping. The impact of channel engineering also observed on performance parameters of the DG-MOSFET such as on current, off current, drain induced barrier lowering, sub-threshold slope and carrier mobility. Thus, an optimized value of the channel doping will be projected for future reference in context of leakage power. Thus channel engineering will play an important role in optimizing the device parameters.

## General Terms
Integrated Circuit, VLSI, MOS Device Modeling.

## Keywords
DG-MOSFET, MOSFET scaling, SS-sub threshold slope, DIBL-drain induced barrier lowering.

## 1. INTRODUCTION
In 1965 Gordon Moore predicted that the number of transistors per chip would quadruple every three years [1]. When channel length of the device shrinks, the close proximity between source and drain reduces the ability of the gate electrode to control the potential distribution and flow of current in the channel. This increases the electrostatic effect of the source/drain electrodes on the channel. As a result short channel effects (SCEs) take dominance. To reduce SCEs we need to increase gate to channel coupling with respect to source/drain to channel coupling. So conventional bulk MOSFET cannot be scaled down below 20 nm [2]. Many structures have been proposed to reduce short channel effects in SOI devices. These limitations can be overcome by using double-gate (DG) MOSFETs. With one extra gate, the gate to channel coupling is doubled resulting in good reduction of SCE's.

When the gate length becomes comparable of depletion region then short channel effects are seen but in DG-MOSFET we are able to reduce these effects. Because of having two gates in DG-MOSFET both gates control the channel from both sides and have better electrostatic control over the channel. So we can perform more scaling of gate length. Due to better control on short channel effects DG-MOSFET is better alternative of conventional bulk MOSFET and it has higher current density, higher sub threshold swing at low supply voltages [3]. Thus we are able to maintain the device performance in term of higher current density and low leakage by using DG-MOSFET.

It recent times double gate MOSFET device structures have drawn more attention of the researchers due to their inherent capability of suppressing the short channel effects. Due to two-channel formation in symmetrical DG-MOSFET, it shows steep subthreshold swing, high drive current and transconductance.

## 2. DG-MOSFET STRUCTURE
In DG-MOSFET structure we use two gates namely front gate and back gate. Due to double gate structure, gate to channel coupling gets doubled and hence SCE's can be suppressed easily.

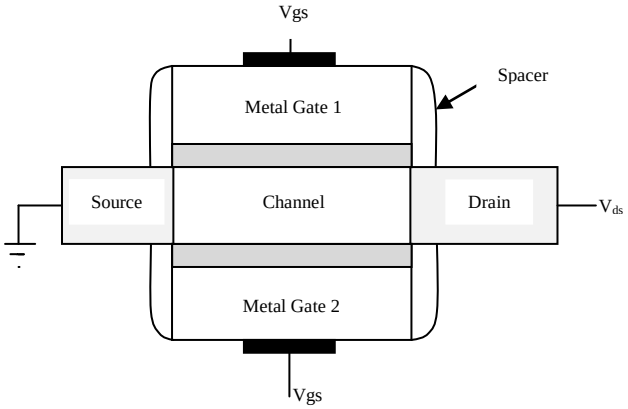


**Fig 1: A general Double Gate MOSFET structure.**

Figure 1 shows a general structure of a double gate MOSFETs. Here we are using metal gate technology instead of polysilicon gate to overcome the poly depletion effect.

### 2.1 Types of DG-MOSFET
Depending upon the way the gate voltages are applied, DG-MOSFETs may be categorized as following:

#### *2.1.1 Symmetric DG-MOSFET*
A DG-MOSFET is said to be symmetric when both gates have the same work function and a single input voltage is applied to both gates.

#### *2.1.2 Asymmetric DG-MOSFET*
An asymmetric DG-MOSFET either has synchronized but different input voltages to both of the identical gates, or has the same input voltage to two gates but gates having different work functions.

The name of "symmetric" and "asymmetric" essentially depicts presence or absence of symmetry of the electric field inside the channel of the DG-MOSFET [4].

# 3. TRANSPORT DESCRIPTIONS

Depending on the device under investigation and the level of modeling accuracy required, one can select following simulation models [5]:

## 3.1 Drift-diffusion model

It is isothermal simulation, described by classical semiconductor equations. This model is suitable for devices designed with low power density specification and having long active regions. In present work Drift-diffusion model had been taken for simulating the device.

### *3.1.1 Drift diffusion Approximation*

The drift-diffusion model is widely used for simulation of carrier transport in semiconductors and is defined by the basic semiconductor equations. Current density for electrons is given by:

$$J_n = qn\mu_n E + qD_n \nabla n$$

$$J_n = -qn\mu_n \nabla \psi_n + qD_n \nabla n \quad \text{..... (1)}$$

Current density for hole is given by:

$$J_p = qp\mu_p E - qD_p \nabla p$$

$$J_p = qp\mu_p \nabla \psi_p - qD_p \nabla p \quad \text{..... (2)}$$

Where $\mu_n$ and $\mu_p$ are the electron and hole mobilities, and $\psi_n$ and $\psi_p$ are the electron and hole quasi-Fermi potentials, respectively.

The three governing equations for carrier transport in semiconductor devices are the Poisson equation and the electron and hole continuity equations. The Poisson equation is:

$$-\nabla^2 \psi = \frac{q}{\varepsilon}(N_D - n + p - N_A) + \rho_{trap} \quad \text{..... (3)}$$

Where $\varepsilon$ is the electrical permittivity, $q$ is the elementary electronic charge, $n$ and $p$ are the densities of electron and hole, $N_D$ is the concentration of donor ion, $N_A$ is the concentration of acceptor ion, and $\rho_{trap}$ is the charge density contributed by traps and fixed charges.

Continuity equation for electron is given by:

$$\nabla . J_n = qR + q\frac{\partial n}{\partial t} \quad \text{..... (4)}$$

$$-\nabla . J_p = qR + q\frac{\partial p}{\partial t} \quad \text{..... (5)}$$

Where, **R** is the net electron–hole recombination rate.

## 3.2 Thermodynamic model

This model accounts for self-heating. It is suitable for devices designed with low thermal exchange, particularly, high-power density and having long active regions.

## 3.3 Hydrodynamic model

This model accounts for energy transport of the carriers. It is suitable for devices with small active regions.

## 3.4 Monte Carlo model

This model allows for full band Monte Carlo device simulation in the selected window of the device.

# 4. SIMULATION RESULTS AND DISCUSSION

In this work we had designed an n-channel metal gate symmetric DG-MOSFET on Sentaurus TCAD simulator [6]. $SiO_2$ is used as gate oxide material and spacers of $Si_3N_4$ is also used to reduce fringing field effect. In this simulation Density Gradient quantization model had been used [7-8].

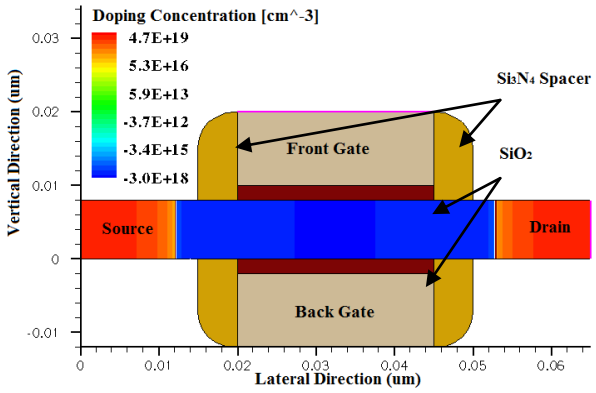


**Fig 2: Simulated Metal gate Symmetric DG-MOSFET**

The simulated device structure (figure 2) is a symmetric DG-MOSFET with following parameters:

**Table 1. Device parameters taken for design**

| S.No. | Parameter | Value [unit] |
|---|---|---|
| 1. | Gate Length | 25[nm] |
| 2. | Gate oxide thickness | 2 [nm] |
| 3. | Silicon film thickness | 8 [nm] |
| 4. | Spacer thickness | 5 [nm] each side |
| 5. | Junction Depth | 12 [nm] |
| 6. | Substrate Doping | 3 x $10^{18}$ [$cm^{-3}$] |
| 7. | Source/Drain Doping | 5 x $10^{19}$ [$cm^{-3}$] |

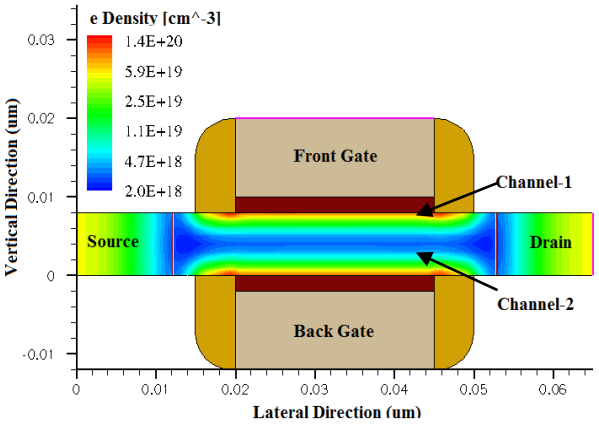


**Fig 3: Electron density in Silicon film**

Figure 3 shows the variation of electron density in silicon film. We can see that electron density is higher at the top and bottom of the film which forms the two conduction channel in DG-MOSFET. Due to formation of two channels it has good drive current $I_{on}$.

## 4.1 Threshold Voltage

Threshold voltage of the device is an important parameter which decides the device performance. The value of gate to source voltage ($V_{gs}$) for which sufficient amount of mobile electrons accumulates in the channel region so that a conducting channel is formed is called the threshold voltage. Table 2 shows the variation of threshold with different doping levels.

**Table 2. Variation of Vth with channel doping conc.**

| S.No. | Channel Doping conc. ($cm^{-3}$) | Vth-lin (mV) | Vth-sat (mV) |
|---|---|---|---|
| 1. | $2x10^{18}$ | 124.91568 | 255.36403 |
| 2. | $3x10^{18}$ | 169.84393 | 355.00426 |
| 3. | $4x10^{18}$ | 217.52769 | 459.12225 |
| 4. | $5x10^{18}$ | 286.09087 | 559.06669 |

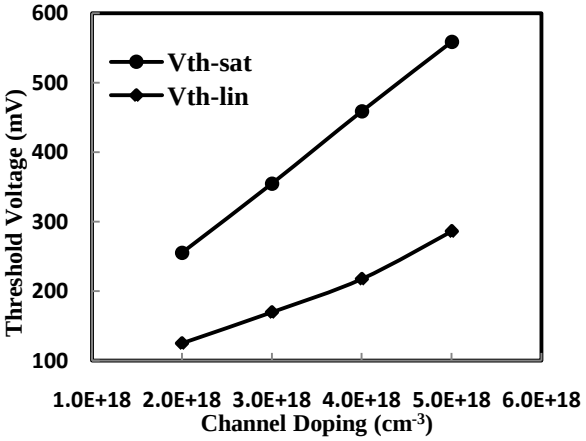


**Fig 4: Threshold voltage versus Channel doping conc.**

From figure 4 it is clear that as we increase the channel doping linear as well as saturation threshold voltage of the device increases. So we can have desired value of the threshold voltage by varying the channel doping. But high channel doping cannot be done as it leads to band to band tunnelling and gate induced drain leakage. For simulated device the suitable value of channel doping is 3.0E+18 $cm^{-3}$ and value of threshold voltage at this doping level are 169.8 mv (linear threshold voltage) and 355 mv (saturation threshold voltage) which is optimum value of threshold voltage for the gate length of 25 nm.

## 4.2 Drive Current ($I_{on}$)

ON-State current, decides the driving capability of the device. It is defined as drain to source current when $V_{gs}=V_{dd}$ and $V_{ds}=V_{dd}$. Table given below shows the drive current variation for different doping levels.

**Table 3. Variation of $I_{on}$ with channel doping conc.**

| S.No. | Channel Doping conc.($cm^{-3}$) | $I_{on}$ current (A/um) |
|---|---|---|
| 1. | $2x10^{18}$ | $4.874x10^{-04}$ |
| 2. | $3x10^{18}$ | $3.872x10^{-04}$ |
| 3. | $4x10^{18}$ | $2.981x10^{-04}$ |
| 4. | $5x10^{18}$ | $2.178x10^{-04}$ |

With increase in channel doping, value of threshold voltage increases as a result of which ON-state current get decreases. Figure 5 shows approximately linear variation with channel doping.

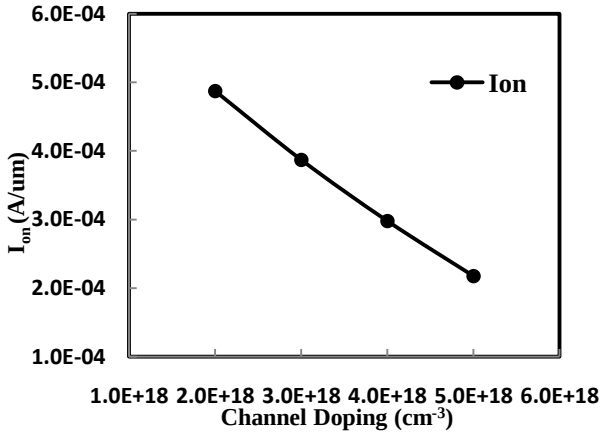


**Fig 5: $I_{on}$ current versus Channel doping conc.**

## 4.3 Drain Leakage Current $I_{off}$

It is defined as drain to source current when $V_{gs}=0$ and $V_{ds}=V_{dd}$. MOSFET's drain leakage current or off-state current ($I_{off}$) is the drain current when no gate voltage is applied. This off-state current is influenced by several other parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide, channel/surface doping profile and supply voltage ($V_{dd}$).

As device dimensions are shrinking, leakage currents are becoming as one of the major parameter which needs more attention. In long-channel devices off-state current mainly due to leakage from the drain-well and well-substrate reverse-bias p-n junctions [9].

**Table 4. Variation of $I_{off}$ with channel doping conc.**

| S.No. | Channel Doping conc. ($cm^{-3}$) | $I_{off}$ current (A/um) |
|---|---|---|
| 1. | $2x10^{18}$ | $8.583x10^{-08}$ |
| 2. | $3x10^{18}$ | $1.449x10^{-08}$ |
| 3. | $4x10^{18}$ | $2.372x10^{-09}$ |
| 4. | $5x10^{18}$ | $3.742x10^{-10}$ |

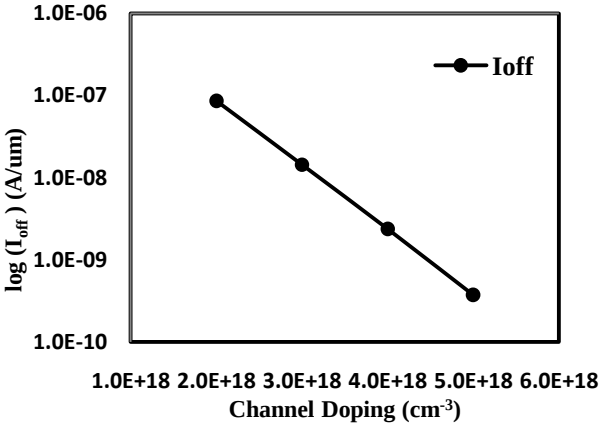


**Fig 6: $I_{off}$ current versus Channel doping conc.**

With increase in channel doping Off-state current get reduces. Figure 6 shows the curve between log($I_{off}$) versus channel doping, from this we can see that for higher values of channel doping Off-state current get reduces very sharply.

## 4.4 $I_{on}/I_{off}$ Ratio

The ratio of total drive current (ON state current) to the leakage current (OFF state current) is an important figure of merit. We define the $I_{on}/I_{off}$ ratio as

$$On/Off \text{ Ratio} = \log_{10}\left[\frac{I_{on}}{I_{off}}\right] \quad \text{..... (6)}$$

Where $I_{off}$ is the current at the gate voltage at $V_{ds}$=0 V and the Ion is the maximum current at gate voltage $V_{ds}=V_{dd}$. The $I_{on}/I_{off}$ current ratio represents the power consumption of a device.

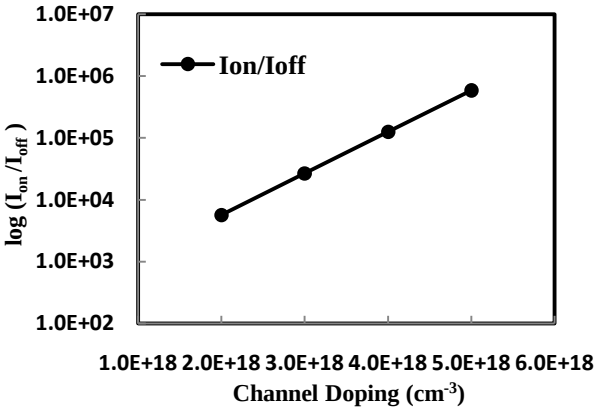


**Fig 7: log ($I_{on}/I_{off}$) versus Channel doping conc.**

As we increase the channel doping drive current reduces almost linearly, but off state current decreases exponentially. This leads to increase in $I_{on}/I_{off}$ ratio very sharply.

## 4.5 Drain Induced Barrier Lowering

DIBL effect occurs in short-channel devices when the depletion regions of the drain and the source interact with each other near the channel surface which results in lowering of the source potential barrier height. Now on application of drain voltage, barrier height reduces in the influence of drain electric field. This leads to injection of more carriers in the channel region but this increase in the carrier is due to drain voltage and not by gate voltage.

*The drain induced barrier lowering is defined as the ratio of change in threshold voltage* $\Delta V_{th}$ *to change in drain voltage* $\Delta V_{ds}$ [10].

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} \quad \text{..... (7)}$$

$$DIBL = \frac{V_{th}(V_{ds1}) - V_{th}(V_{ds2})}{V_{ds2} - V_{ds1}} \quad \text{..... (8)}$$

DIBL is more prominent at high drain voltages and shorter channel lengths. We can reduce drain induced barrier lowering effect by using higher surface and channel doping [11, 12].

**Table 5. Variation of DIBL with channel doping conc.**

| S.No. | Channel Doping conc. ($cm^{-3}$) | DIBL (mV/V) |
|---|---|---|
| 1. | $2x10^{18}$ | 20.533 |
| 2. | $3x10^{18}$ | 19.042 |
| 3. | $4x10^{18}$ | 15.799 |
| 4. | $5x10^{18}$ | 12.036 |

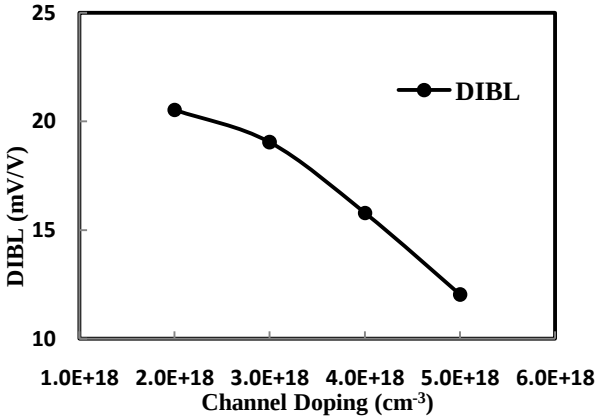


**Fig 8: DIBL versus Channel doping conc.**

From figure 8 we can see that as we increase channel doping, number of carrier in channel region increases and DIBL value reduces.

## 4.6 Subthreshold region and Subthreshold Swing

When $V_{gs}$ is smaller than but close to $V_{th,}$ a small conduction current flows between source and drain in the MOSFET and it is said that transistor is in subthreshold or weak inversion region. In weak inversion, minority carrier concentration is small, but not zero.

Subthreshold swing is an important parameter which determines the scalability limits of DG-MOSFET. It indicates how effectively the flow of drain current of a device can be stopped when $V_{gs}$ is decreased below $V_{th}$.

The inverse of the slope of $\log_{10}I_{ds}$ versus $V_{gs}$ characteristic is called the sub-threshold swing ($S_t$) [11]. It shows how much change in gate voltage is required to change the drain current by one decade.

$$St = \left(\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right)^{-1} \quad \text{..... (9)}$$

**Table 6. Variation of SS with channel doping conc.**

| S.No. | Channel Doping conc. ($cm^{-3}$) | SS (mV/decade) |
|---|---|---|
| 1. | $2x10^{18}$ | 70.775 |
| 2. | $3x10^{18}$ | 74.158 |
| 3. | $4x10^{18}$ | 79.851 |
| 4. | $5x10^{18}$ | 91.154 |

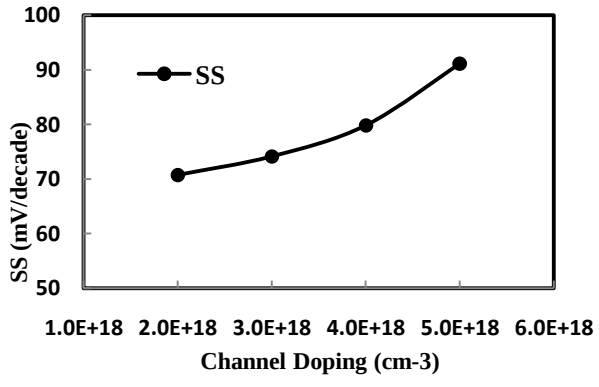


**Fig 9: Subthreshold swing versus Channel doping conc.**

As we increase the channel doping, subthreshold swing increases linearly as shown in figure 9. For a device lower value of subthreshold swing is desirable so undoped or lightly doped channel devices are preferred over doped channel devices.

## 4.7 Mobility degradation

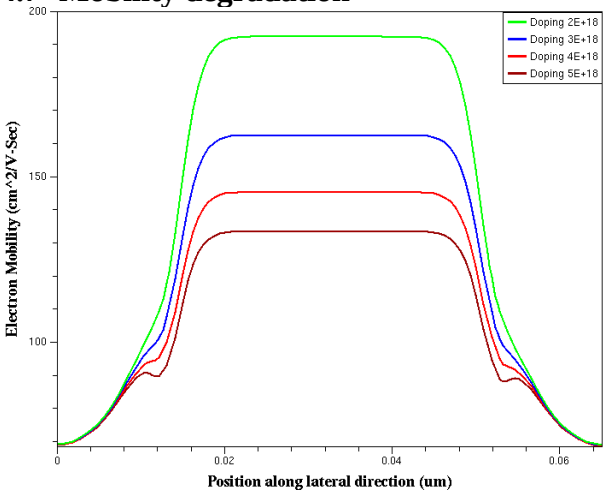


**Fig 10: Electron mobility in lateral direction of device.**

Figure 10 shows the variation of electron mobility along the lateral direction of the device for different channel doping. We can observe that as we move along the lateral direction of the device from source to drain, electron mobility increases and it is highest in the channel region and after that it starts decreasing.

**Table 7. Variation of electron mobility with channel doping conc.**

| S.No. | Channel Doping conc. ($cm^{-3}$) | Electron mobility ($cm^2$/V-Sec) |
|---|---|---|
| 1. | $2x10^{18}$ | 192.676 |
| 2. | $3x10^{18}$ | 162.374 |
| 3. | $4x10^{18}$ | 145.168 |
| 4. | $5x10^{18}$ | 133.319 |

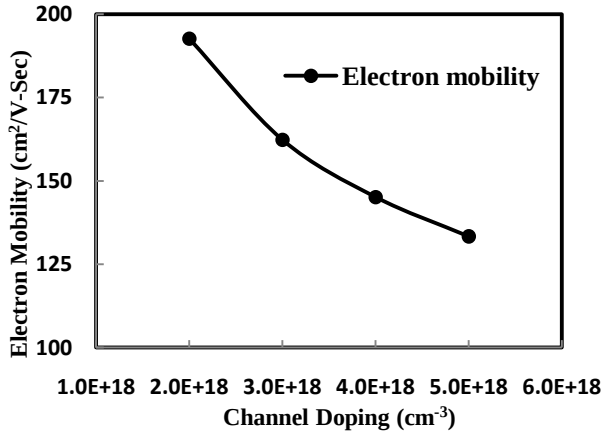


**Fig 11: Electron mobility versus Channel doping conc.**

As shown in figure 11, with increase in channel doping, mobility of electrons in channel region decreases. For enhanced carrier mobility we use lightly doped channel DG-MOSFET.

## 5. CONCLUSION

From the above discussions we can conclude that as we scale down the devices, threshold voltage of the device decreases, to adjust the threshold voltage and other short channel effects within the permissible limits we can do channel engineering. But we cannot increase the channel doping beyond a certain limit because some parameters like subthreshold swing and drain induced barrier lowering, both are opposite in nature. If we increase channel doping one parameter get improved while other get worse. So we have to optimize their value at particular doping level. We also cannot use high doping because mobility degradation of carrier takes place in the channel region.

## 6. ACKNOWLEDGEMENT

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