Impact of Gate Dielectric in Carrier Mobility in Low Temperature Chalcogenide Thin Film Transistors for Flexible Electronics

Electrochemical and Solid-State Letters, **13** (9) H313-H316 (2010)
1099-0062/2010/13(9)/H313/4/$28.00 © The Electrochemical Society

Impact of Gate Dielectric in Carrier Mobility in Low Temperature Chalcogenide Thin Film Transistors for Flexible Electronics

A. L. Salas-Villasenor,[a] I. Mejia,[a] J. Hovarth,[a] H. N. Alshareef,[b] D. K. Cha,[b] R. Ramirez-Bon,[c] B. E. Gnade,[a] and M. A. Quevedo-Lopez[a,z]

[a]*Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, Texas 75080, USA*
[b]*Department of Materials Science and Engineering, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia*
[c]*Centro de Investigación y Estudios Avanzados del IPN, Unidad Querétaro, Querétaro, Qro. 76001, Mexico*

Cadmium sulfide thin film transistors were demonstrated as the n-type device for use in flexible electronics. CdS thin films were deposited by chemical bath deposition (70°C) on either 100 nm HfO_2 or SiO_2 as the gate dielectrics. Common gate transistors with channel lengths of 40–100 μm were fabricated with source and drain aluminum top contacts defined using a shadow mask process. No thermal annealing was performed throughout the device process. X-ray diffraction results clearly show the hexagonal crystalline phase of CdS. The electrical performance of HfO_2/CdS-based thin film transistors shows a field effect mobility and threshold voltage of 25 $cm^2\ V^{-1}\ s^{-1}$ and 2 V, respectively. Improvement in carrier mobility is associated with better nucleation and growth of CdS films deposited on HfO_2.
 [DOI: 10.1149/1.3456551]

Manuscript submitted May 5, 2010; revised manuscript received June 1, 2010. Published June 29, 2010.

Amorphous silicon (a-Si:H) thin film transistors (TFTs) have become one of the most common devices employed in the large area/flexible electronics industries because they are relatively inexpensive to produce over large areas as compared to single-crystal silicon.[1] While the a-Si:H TFT technology has emerged as the industry leader in applications such as active matrix liquid crystal display backplanes, its relatively low mobility (~1 $cm^2\ V^{-1}\ s^{-1}$) and threshold voltage instability[2,3] limit its use in applications that require significant device performance. Therefore, the development of alternative TFT semiconductor materials is very relevant and is currently mostly driven by improved carrier mobility, device stability, and reduced processing costs.[4]

The synthesis of binary metal chalcogenides of group II–VI semiconductors has been a rapidly growing area of research due to their important nonlinear optical properties,[5-8] luminescent properties,[9-12] quantum size effect,[13-15] and other important physical and chemical properties.[16,17] Among the most studied chalcogenides is cadmium sulfide (CdS). CdS, with a bandgap of 2.4 eV (in bulk),[18] was studied as the semiconductor active layer during the early development of TFTs.[19] Recently, chemically deposited CdS active layers have shown acceptable performance in TFTs with field effect mobility values in the range of 0.5–1.5 $cm^2\ V^{-1}\ s^{-1}$, comparable to those obtained with a TFT based in a-Si:H.[20-24] However, all of these articles included a postdeposition annealing process at temperatures higher than 200°C. The maximum processing temperature for flexible electronics must be lower than 200°C.

CdS thin films can be prepared by a variety of physical and chemical methods. Among those, chemical bath deposition (CBD) processes are attractive because they are simple and inexpensive techniques that can yield homogeneous, adherent, transparent, and highly stoichiometric CdS thin films.[25,26] Typically, in CBD, the CdS films are deposited from the reaction between a cadmium salt and thiourea in an alkaline solution.[27-29]

Here we report the properties of CdS synthesized by an ammonia-free CBD process employing sodium citrate as the complexing agent.[30,31] An atomic layer deposited HfO_2 gate dielectric improves the effective mobility of the resulting TFT devices to values as high as 25 $cm^2\ V^{-1}\ s^{-1}$. Furthermore, the maximum processing temperature is maintained below 100°C, which is compatible with flexible substrates used in flexible electronic applications.[32]

Normally, in devices with SiO_2 as the gate dielectric, the mobility increases linearly with increasing charge per unit area on the semiconductor side of the insulator (Q_S) and the gate field (E) until it eventually saturates. Because Q_S is a function of the concentration of accumulated carriers in the channel region (N) and the accumulation region is confined very close to the interface of the insulator with the organic semiconductor,[33] an increase in gate voltage (V_G) results in an increase in E and N. Dimitrakopoulos and Malenfant demonstrated that high mobilities in pentacene TFTs can be achieved at low operating voltages when relatively high dielectric constant gate insulator materials are used. The increased mobility was explained by using a multiple trapping and release model. This model explains that mobility in organic TFTs depends on N (accumulated carriers in the channel) rather than E (electric field). In other words, for the same V_G, N depends on both the dielectric constant and the thickness of the gate insulator, while E depends only on the dielectric thickness. If SiO_2 is replaced with an insulator having similar thickness but a higher dielectric constant (such as HfO_2, used here), then charge accumulation is facilitated and carrier concentrations similar to the SiO_2 case can be attained at a much lower V_G (and E) with improved mobilities.

We used a cadmium chloride/sodium citrate/thiourea system to grow the CdS active layers using the CBD method that we have reported before.[30,31] The CdS was deposited on different gate dielectric materials: p-Si/SiO_2/CdS and p-Si/HfO_2/CdS with Al gate, source, and drain contacts. The SiO_2 dielectric (100 nm) was grown at 1100°C using a single-wafer system. The HfO_2 (100 nm) films were deposited using atomic layer deposition (ALD) at 100°C. After the gate dielectric formation, the substrates were immersed in the chemical bath solution prepared by the sequential addition of 0.05 M $CdCl_2$ (cadmium chloride), 0.5 M $Na_3C_6H_5O_7$ (sodium citrate), 0.5 M KOH (potassium hydroxide), and 0.5 M $CS(NH_2)_2$ (thiourea) in distilled water. The beaker with the solution was then immersed in a thermal bath with the temperature set to 70°C. The substrates were placed vertically in the beaker. Stirring was not used during the deposition. The CdS thickness series to study film nucleation and growth was obtained by sequentially removing the CdS substrates from the CBD solution. Deposition times ranged from 0.5 to 25 min. After deposition, the CdS films were cleaned in an ultrasonic bath with methanol, rinsed with distilled water, and dried with N_2 gas. Next, 100 nm of Al was used as the source and drain metal contacts. The source and drain were defined using a shadow mask process.

The resulting CdS films were studied using many materials characterization techniques. The crystalline structure was analyzed in a

[z] E-mail: mquevedo@utdallas.edu

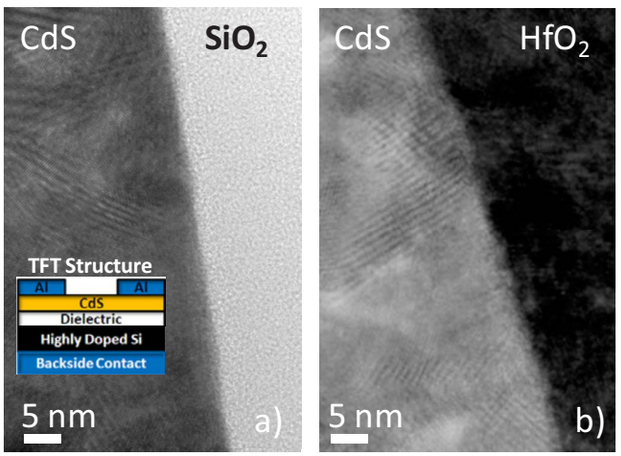

Figure 1. (Color online) TEM for CdS films grown at 70°C for 25 min on (a) SiO_2 and (b) HfO_2. A schematic cross section of the TFT fabricated is also illustrated.

Rigaku Ultima III X-ray diffractometer. Transmission electron microscopy (TEM) was performed in a JEOL 2100 system. X-ray photoelectron spectroscopy (XPS) analyses were performed in an Omicron 5600 system, and the electrical characteristics of the TFTs were determined using current–voltage (*I-V*) measurements at room temperature in a 4200 Keithley semiconductor parameter analyzer.

The resulting CdS layers were homogeneous and continuous with an average grain size of ~30 nm, as calculated by X-ray diffraction (XRD). This morphology suggests that the deposition process is through an ion-by-ion mechanism, as previously reported.[34,35]

Figure 1 shows the TEM images for the CdS thin films grown on SiO_2 and HfO_2 at 70°C for 25 min (~60 nm thick). A higher surface roughness is observed for CdS deposited on HfO_2 when compared with those deposited on SiO_2. However, and independent of the dielectric, crystalline features are observed in the CdS films indicating that the films are polycrystalline.

Figure 2 shows the XRD results for the CdS films grown on SiO_2 (Fig. 2a) and HfO_2 (Fig. 2b) deposited for 6, 12, and 25 min. The thickness of the CdS films grown for 12 min was ~35 nm, whereas the thickness of those deposited for 25 min was ~60 nm. The thickness for the CdS films deposited for times shorter than 6 min could not be measured and no crystalline features were detected by XRD. The XRD pattern for the films deposited for 12 and 25 min shows clear diffraction peaks corresponding to the (100), (002), and (101) crystalline planes of the hexagonal crystalline phase of CdS.[36] Clearly, the resulting CdS films deposited after 12 min are polycrystalline with a hexagonal structure and with a preferred crystalline orientation along the (002) direction. The final microstructure of the CdS deposited on HfO_2 and SiO_2 is different. This difference in the microstructure starts at the early stages of CdS nucleation and growth and it remains constant throughout the entire CdS film thickness, as clearly seen in Fig. 2a and b.

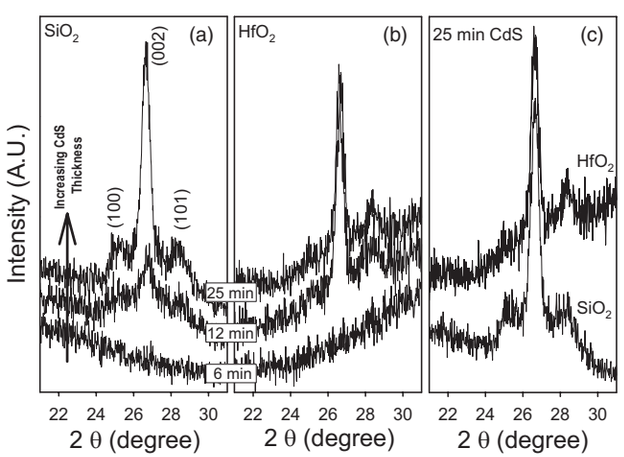

Figure 2. XRD patterns for the samples deposited at different times on (a) SiO_2 and (b) HfO_2 dielectric layer and (c) CdS grown for 25 min on HfO_2 or SiO_2.

Although both films show a preferential growth in the (002) direction, CdS deposited on HfO_2 does not show a clear diffraction for the (100) orientation. The difference in the XRD patterns suggests that the CdS grown in HfO_2 are mostly composed of (002) and (101) phases, whereas the CdS deposited on SiO_2 shows an additional orientation in the (100) direction. The difference in nucleation for CdS on SiO_2 and HfO_2 is likely due to the presence of an excess of hydroxyl groups (OH^-) resulting from the ALD process (as we will discuss in detail below). Thermal SiO_2 is likely to have a lower concentration of OH^- on the surface, and therefore, less nucleation sites for CdS growth.

Figure 2c compares the XRD results for CdS grown for 25 min (~60 nm) on either HfO_2 or SiO_2. Clearly, the CdS grown on SiO_2 is more polycrystalline than that grown in HfO_2. This results in more grain boundaries at the interface between the dielectric and the semiconductor. This is likely to result in degraded carrier mobility for the CdS films deposited on SiO_2.

To further investigate the impact of the dielectric in the nucleation of the CdS films, XPS was performed for the CdS films deposited for 0.5, 1, and 2 min on either SiO_2 or HfO_2. Figure 3a and b shows the Cd 3d region for the CdS films deposited on HfO_2 and SiO_2, respectively. For reference, the scan for the HfO_2 and SiO_2 films before any CdS deposition is also shown. In HfO_2 (Fig. 3a), the Cd 3d feature is observed in depositions of as short as 0.5 min, and after 2 min of reaction, distinct peaks of Cd bonded to S are clearly observed.[37] However, for the CdS films deposited on SiO_2, no Cd features are observed for times shorter than 2 min (Fig. 3b). The presence of the Cd XPS features from the very early stages in CdS deposited on HfO_2 indicates that nucleation in this dielectric is faster than when CdS is grown on SiO_2.

Figure 3c and d shows the S 1s region for the CdS films deposited on HfO_2 and SiO_2, respectively. The peak observed at ~162 eV for the CdS films deposited for 2 min on HfO_2 corresponds to S bonded to Cd and the broad peak at ~169 eV corresponds to $CdSO_4$ (Fig. 3c).[37,36] No sulfur is detected for deposition times shorter than 2 min; therefore, in HfO_2, 2 min of reaction is enough to grow CdS. Similarly, from CdS deposited on SiO_2, no sulfur is observed for times shorter than 2 min (Fig. 3d). The small band at ~162 eV observed in films grown for 2 min indicates that CdS is just beginning to grow. These substantial differences in the nucleation of CdS on HfO_2 and SiO_2 impact the final microstructure of the resulting CdS films (Fig. 2). The $CdSO_4$ feature might be due to surface oxidation due to air exposure before the XPS analyses.

The O 1s region for CdS deposited on HfO_2 is shown in Fig. 3e. The peaks observed in the films grown for less than 2 min are consistent with a mixture of $CdSO_4$ (531.70 eV), $Cd(OH)_2$ (530.90 eV), and CdO (531.60 eV).[36,37] For reference, a CdS film deposited for 25 min is also shown. No clear difference between the CdS films deposited for 2 and 25 min on HfO_2 is observed, which indicates that the excess oxygen is likely due to surface oxidation resulting from air exposure of the films before the XPS analyses. It is difficult to determine if the CdS films grown for times shorter than 2 min on SiO_2 (Fig. 3f) have $CdSO_4$, $Cd(OH)_2$, or CdO because the XPS bands from these materials overlap with the Si–O–Si band at ~533 eV. The broadening and intensity reduction of the band as

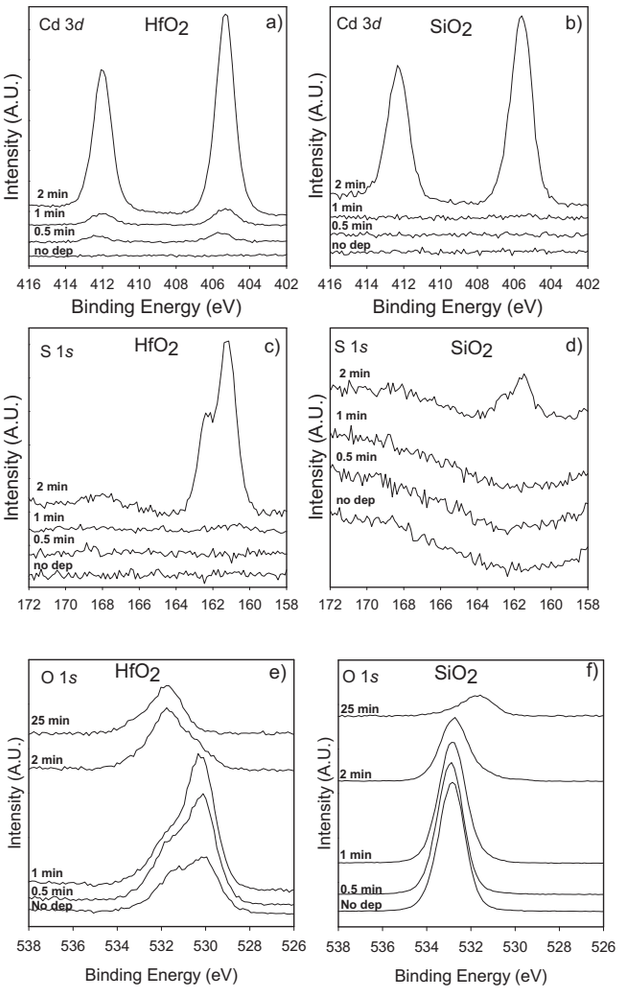

Figure 3. XPS for CdS films grown on either HfO_2 or SiO_2.

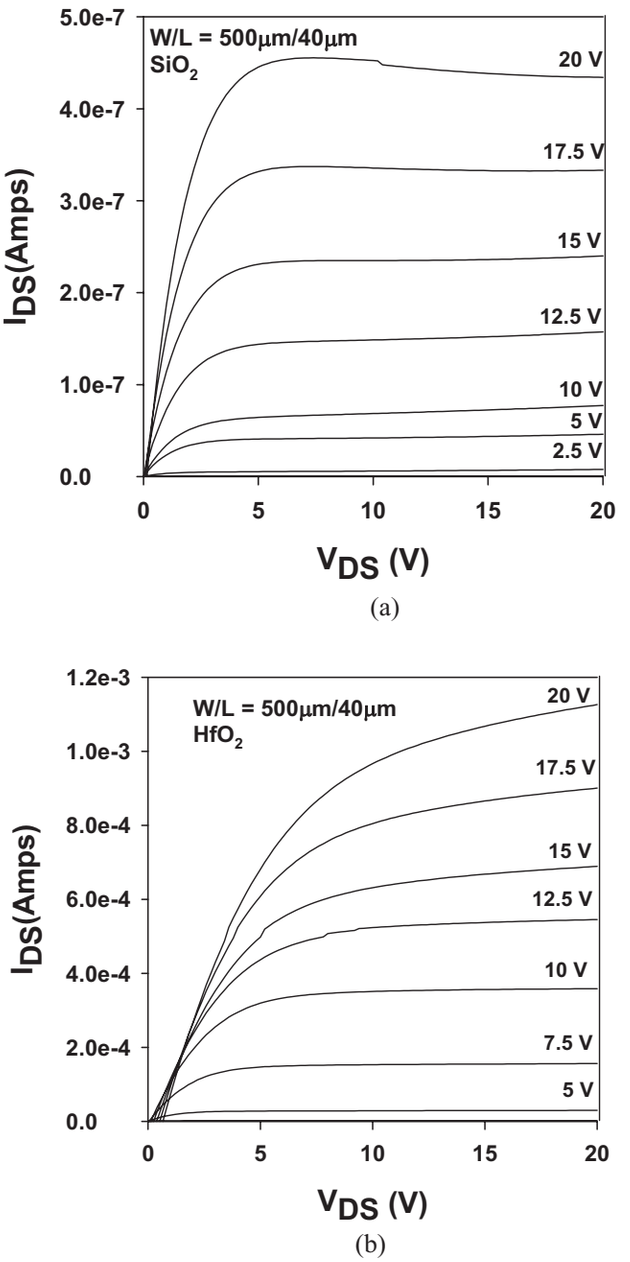

Figure 4. Characteristic I_D vs V_{DS} plots for several values of V_G for the CdS-based TFTs deposited on (a) SiO_2 and (b) HfO_2.

well as evidence of Cd (Fig. 3b) and S (Fig. 3d) seem to indicate the presence of Cd–S bonds for reactions with deposition times longer than 2 min.

The electrical characteristics of TFTs with CdS films deposited for 25 min (60 nm) on SiO_2 and HfO_2 are shown in Fig. 4 and 5. Figure 4 shows the drain current (I_D) vs source–drain voltage (V_{DS}) results, measured from 0 to 20 V for devices with (a) SiO_2 and (b) HfO_2 as the gate dielectric. An excellent transistor behavior is observed in devices deposited on either SiO_2 or HfO_2. The decrease in I_D with V_{DS} at high V_G observed for devices with SiO_2 as the dielectric material is likely due to a well-known effect in poly-Si-based TFTs and silicon on insulator devices where thermal effects caused by power dissipation in metal-oxide-semiconductor devices can alter their *I-V* characteristics and can even show a negative dynamic resistance in their saturation regions.[38] Our SiO_2 devices are fabricated on top of a thick insulator, which might limit power dissipation and result in increased temperature in the channel at high V_G, which results in lower mobility and reduced I_D at V_G. I_G in these devices is very low.

The I_D-V_G (solid lines) and the $\sqrt{I_D}$-V_G (dashed lines) for CdS films deposited for 25 min (60 nm) on SiO_2 and HfO_2 are shown in Fig. 5a and b, respectively. All measurements were performed at V_{DS} = 20 V. To determine the channel mobility (μ) and the threshold voltage (V_T) for the devices, the linear region of the curves were fitted to the equation[39]

$$I_D^{1/2} = \left(\frac{C_i W \mu_{sat}}{2L}\right)^{1/2} (V_G - V_T) \quad [1]$$

where V_G is the gate voltage, W is the channel width, L is the channel length, and C_i is the capacitance per unit area for the gate dielectric. The fitting is shown as dotted lines in Fig. 5. The threshold voltage, which corresponds to the intersections of the dotted lines with the V_G axis, is ~9 V for devices with SiO_2 and ~2 V for devices with HfO_2. One of the reasons for the lower V_T observed for CdS deposited on HfO_2 is the higher dielectric constant of HfO_2. More importantly, the electron mobility, extracted for devices with SiO_2 as the gate dielectric, is 2.3×10^{-2} cm^2 V^{-1} s^{-1}, whereas for devices with HfO_2 as the gate dielectric, the mobility is ~25 cm^2 V^{-1} s^{-1} or higher. The electron mobility of bulk CdS is 210 cm^2 V^{-1} s^{-1}.[19] The main reason for the lower mobility in

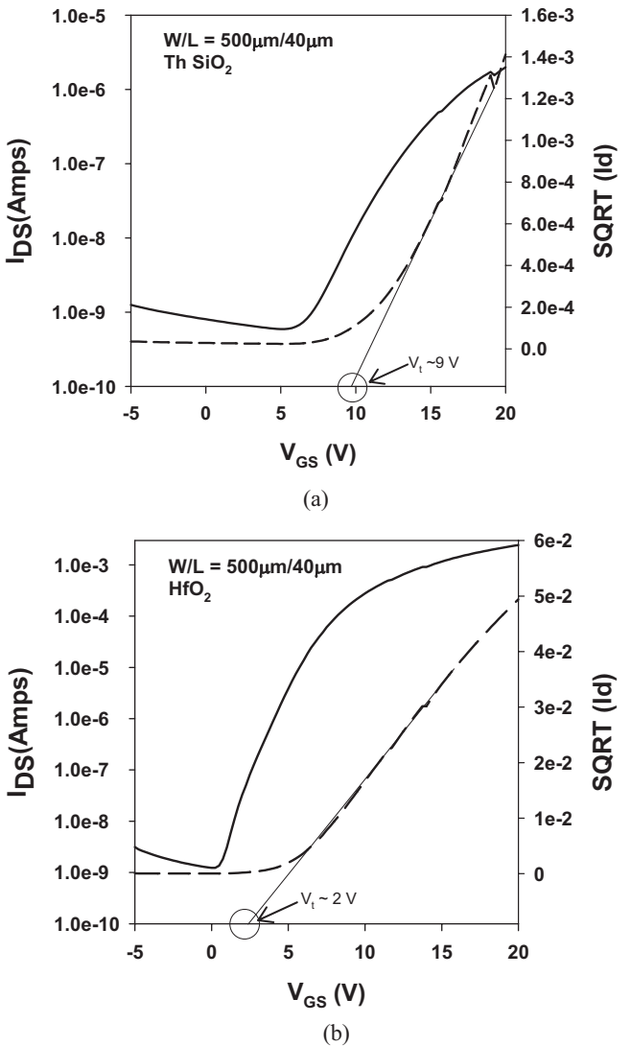

Figure 5. $\sqrt{I_D}$ vs V_G plots (right axis) for the CdS-based TFTs on different dielectrics (a) SiO_2 and (b) HfO_2. The straight lines correspond to the best linear fits to Eq. 1. Semilogarithmic plots of I_D vs V_G (left axis) for the same devices.

TFTs is the polycrystalline nature of the CdS layers. The electrical response of the HfO_2/CdS-based TFTs is considerably higher than that reported for SiO_2/CdS-based TFTs (μ_{sat} = 0.13–0.16 cm^2 V^{-1} s^{-1} and V_T = 8.8–25 V) [24] and the CdS deposited here on SiO_2 (0.023 cm^2 V^{-1} s^{-1}). The main reason for the better mobility of the devices fabricated on HfO_2 is likely the better interface between the dielectric and the semiconductor. This behavior is associated with the (OH^-)-rich surface of the HfO_2 that results from the ALD process. This CBD-friendly surface promotes better nucleation and growth and better oriented CdS films. The fabrication process for the CdS-based TFTs reported here does not include thermal annealing, and the highest temperature involved in the processing of the HfO_2/CdS-based TFTs is 100°C, which is quite compatible with the fabrication of electronic flexible devices.

In conclusion, we have studied the growth stages in the CBD process of CdS films on different dielectric layers and correlated film structure with device performance. CdS films as-grown on HfO_2 showed higher mobility (~25 cm^2 V^{-1} s^{-1}) and low threshold voltage (~2 V). HfO_2 seems to provide a better starting surface for CdS nucleation and growth. This is likely due to the presence of $(OH)^-$ on the surface of the HfO_2 as a result of the ALD process used to deposit the HfO_2 films. Based on these results we conclude that ALD HfO_2 is a promising dielectric for chalcogenide-based TFT devices for flexible electronics.

Acknowledgments

This work was partially supported by the Army Research Laboratory and CONACYT Mexico.

University of Texas at Dallas assisted in meeting the publication costs of this article.

References

1. C. D. Dimitrakopoulos and P. R. L. Malenfant, *Adv. Mater.*, **14**, 99 (2002).
2. A. Sazonov and A. Nathan, *J. Vac. Sci. Technol. A*, **18**, 780 (2000).
3. C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, *J. Vac. Sci. Technol. B*, **18**, 683 (2000).
4. R. E. I. Schropp, B. Stannowski, and J. K. Rath, *J. Non-Cryst. Solids*, **299–302**, 1304 (2002).
5. S. Bose and S. K. Saha, *Chem. Mater.*, **15**, 4464 (2003).
6. L. E. Brus, *Appl. Phys. A: Mater. Sci. Process.*, **53**, 465 (1991).
7. Y. Wang and N. Herron, *J. Phys. Chem.*, **95**, 525 (1991).
8. A. Henglein, *Top. Curr. Chem.*, **143**, 113 (1988).
9. R. B. Kale, S. D. Sartale, B. K. Chougule, and C. D. Lokhande, *Semicond. Sci. Technol.*, **19**, 980 (2004).
10. N. N. Greenwood and E. A. Earnshaw, *Chemistry of the Elements*, Pergamon Press, Oxford (1990).
11. A. Vadivel Murugan, R. S. Sonawane, B. B. Kale, S. K. Apte, and A. V. Kulkarni, *Mater. Chem. Phys.*, **71**, 98 (2001).
12. W. Hoheisel, V. L. Colvin, C. S. Johnson, and A. P. Alivisatos, *J. Chem. Phys.*, **101**, 8455 (1994).
13. C. B. Murray, C. R. Kagan, and M. G. Bawendi, *Science*, **270**, 1335 (1995).
14. R. Rossetti, R. Hull, J. M. Gibson, and L. E. Brus, *J. Chem. Phys.*, **82**, 552 (1985).
15. M. L. Steigerwald and L. E. Brus, *Annu. Rev. Mater. Sci.*, **19**, 471 (1989).
16. S. Mann, *Nature (London)*, **332**, 119 (1988).
17. C. B. Murray, D. J. Morris, and M. G. Bawendi, *J. Am. Chem. Soc.*, **115**, 8706 (1993).
18. J. I. Pankove, *Optical Processes in Semiconductors*, Dover, New York (1971).
19. W. E. Howard, in *Thin Film Transistors*, C. R. Kagan and P. Andry, Editors, Marcel Dekker, New York (2003).
20. F. Y. Gan and I. Shih, *IEEE Trans. Electron Devices*, **49**, 15 (2002).
21. C. Voss, S. Subramanian, and C.-H. Chang, *J. Appl. Phys.*, **96**, 5819 (2004).
22. B. Mereu, G. Sarau, E. Pentia, V. Draghici, M. Lisca, T. Botila, and L. Pintilie, *Mater. Sci. Eng., B*, **109**, 260 (2004).
23. Y.-J. Chang, C. L. Munsee, G. S. Herman, J. F. Wager, P. Mugdur, D.-H. Lee, and C.-H. Chang, *Surf. Interface Anal.*, **37**, 398 (2005).
24. J. H. Lee, J. W. Yoon, I. G. Kim, J. S. Oh, H. J. Nam, and D. Y. Jung, *Thin Solid Films*, **516**, 6492 (2008).
25. R. Ramírez-Bon, M. A. Quevedo-López, R. A. Orozco-Terán, F. J. Espinoza-Beltrán, and M. Sotelo-Lerma, *J. Phys. Chem. Solids*, **59**, 145 (1998).
26. R. A. Orozco-Terán, M. Sotelo-Lerma, R. Ramirez-Bon, M. A. Quevedo-López, O. Medoza-González, and O. Zelaya-Angel, *Thin Solid Films*, **343–344**, 587 (1999).
27. D. S. Boyle, A. Bayer, M. R. Heinrich, O. Robbe, and P. O. O'Brien, *Thin Solid Films*, **361–362**, 150 (2000).
28. D. Hariskos, M. Powalla, N. Chevaldonnet, D. Lincot, A. Schindler, and B. Dimmler, *Thin Solid Films*, **387**, 179 (2001).
29. H. Zhang, X. Ma, and D. Yang, *Mater. Lett.*, **58**, 5 (2004).
30. M. B. Ortuño-López, J. J. Valenzuela-Jáuergui, M. Sotelo-Lerma, A. Mendoza-Galván, and R. Ramírez-Bon, *Thin Solid Films*, **429**, 34 (2003).
31. M. B. Ortuño-López, M. Sotelo-Lerma, A. Mendoza-Galván, and R. Ramírez-Bon, *Thin Solid Films*, **457**, 278 (2004).
32. S. Gowrisanker, M. A. Quevedo-Lopez, H. N. Alshareef, B. Gnade S. Venugopal, R. Krishna, K. Kaftanoglu, and D. Allee, *Org. Electron.*, **10**, 1217 (2009).
33. A. Dodabalapur, L. Torsi, and H. E. Katz, *Science*, **268**, 270 (1995).
34. D. Lincot and R. Ortega-Borges, *J. Electrochem. Soc.*, **139**, 1880 (1992).
35. M. G. Sandoval-Paz, M. Sotelo-Lerma, A. Mendoza-Galvan, and R. Ramírez-Bon, *Thin Solid Films*, **515**, 3356 (2007).
36. K. L. Narayanan K. P. Vijayakumar K. G. M. Nair, and G. V. N. Rao, *Bull. Mater. Sci.*, **20**, 287 (1997).
37. D. A. Mazón-Montijo, M. Sotelo-Lerma, M. A. Quevedo-Lopez, M. El-Bouanani, H. N. Alshareef, F. J. Espinoza-Beltrán, and R. Ramírez-Bon, *Appl. Surf. Sci.*, **254**, 499 (2007).
38. D. Sharma, J. Gautier, and G. Merckel, *IEEE J. Solid-State Circuits*, **13**, 378 (1978).
39. J. Jang, in *Thin Film Transistors*, C. R. Kagan and P. Andry, Editors, Marcel Dekker, New York (2003).