

Impact of Grain Structure and Material Properties on Via Extrusion in 3D Interconnects

Tengfei Jiang,^{1,*} Chenglin Wu,² Jay Im,¹ Rui Huang,² and Paul S. Ho¹

Abstract—In this article, the effects of Cu microstructure on the mechanical properties and extrusion of through-silicon vias (TSVs) were studied based on two types of TSVs with different microstructure. A direct correlation was found between the grain size and the mechanical properties of the vias. Both an analytical model and finite element analysis (FEA) were used to establish the relationship between the mechanical properties and via extrusion. The effect of via/Si interface on extrusion was also studied by FEA. The results suggest small and uniform grains in the Cu vias, as well as stronger interfaces between the via and Si led to smaller via extrusion, and are thus preferable for reduced via extrusion failure and improved TSV reliability.

Keywords—3D integration, via extrusion, microstructure, FEA, interface

INTRODUCTION

Copper through-silicon via (TSV) is a key element for three-dimensional (3D) integration. The basic fabrication steps of the TSVs include drilling of via holes, deposition of liner and seed layers, filling of the via by electroplating, postelectroplating annealing, and chemical-mechanical planarization (CMP) to remove the Cu overburden. In the widely used via-middle scheme, the via fabrication is followed by the deposition of back-end-of-the-line (BEOL) layers, which subjects the TSVs to elevated temperatures. Via extrusion that occurs during the BEOL processing can deform the BEOL layers and cause mechanical and electrical failures in the interconnect structures [1-5]. The need to control and reduce via extrusion by process optimization has generated great interest in the development of 3D integration. In particular, high-temperature annealing after via filling has been proposed and adopted to stabilize the Cu grain structure and to minimize extrusion [3-5]. Various annealing conditions have been investigated, and it has been demonstrated that extrusion can indeed be reduced but not completely eliminated. Previous studies suggest that the stress and mechanical properties of the Cu via directly

affect via extrusion [6-8]. The underlying mechanism of via extrusion has been examined by considering plastic deformation in Cu and via/Si interfacial sliding [9, 10]. For the purpose of process optimization, it is important to establish a correlation between the microstructures and the mechanical properties of the Cu vias, which in turn can be correlated to via extrusion. In this work, the microstructures and mechanical properties of Cu TSVs were characterized, followed by measurement and modeling of via extrusion.

MICROSTRUCTURE OF CU TSVS

The TSV samples used in this study were blind via structures fabricated with the standard via-middle scheme. The via diameter was $D = 5.5 \mu\text{m}$, the via depth was $H = 55 \mu\text{m}$, and the Si wafer was $780 \mu\text{m}$ thick. During fabrication, the TSV samples were subjected to two different processing conditions. To differentiate the samples, the samples will be referred to as TSV-A and TSV-B. The cross sections for a number of vias of each type were examined by focused ion beam (FIB), and the microstructure of the TSV samples was studied by electron backscatter diffraction (EBSD) measurement. For both types of vias, random grain orientation was observed (Fig. 1a). However, the grain size distributions were rather different (Fig. 1b). Based on EBSD measurement, the grain size in each type of vias was calculated using both the numerical average,

$$\bar{D}_{\text{num}} = \frac{\sum_{i=1}^N D_i}{N},$$

and the area average

$$\bar{D}_{\text{area}} = \frac{\sum_{i=1}^N A_i D_i}{\sum_{i=1}^N A_i}.$$

Here D_i and A_i are the diameter and area of grain i , and N is the total number of grains. The closer these two values are to each other, the more uniform the grain size is. Quantitatively, the area average grain size, \bar{D}_{area} , was found to be $2.83 \mu\text{m}$ for TSV-A and $3.82 \mu\text{m}$ for TSV-B, and the numerical average grain size, \bar{D}_{num} , was $1.39 \mu\text{m}$ and $1.53 \mu\text{m}$ for TSV-A and TSV-B, respectively. The larger difference between \bar{D}_{num} and \bar{D}_{area} for TSV-B indicated that the grain size distribution was wider in TSV-B, where several large grains were mixed with small grains. The large grains in TSV-B sometimes spanned across the diameter of the entire via. For TSV-A, the grain sizes were relatively more uniform, although there was still a

The manuscript was received on November 19, 2014; revision received on May 18, 2015; accepted on May 19, 2015

The original version of this paper was presented at IMAPS 47th International Symposium on Microelectronics (IMAPS'2014), October 14-16, 2014, San Diego, CA.

¹Microelectronics Research Center and Texas Materials Institute, University of Texas, Austin, Texas 78712

²Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, Texas 78712

*Corresponding author; email: jiangt@mail.utexas.edu

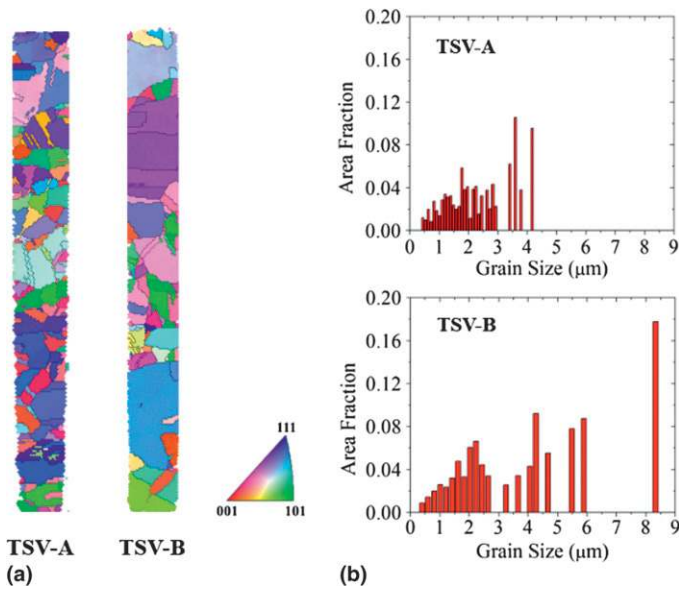


Fig. 1. Microstructure measurement by EBSD for TSV-A and TSV-B. (a) Grain mapping; (b) grain size distributions.

difference between \bar{D}_{num} and \bar{D}_{area} . The difference in grain size distribution between TSV-A and TSV-B can be seen from a representative grain mapping and grain size distribution in Fig. 1.

MECHANICAL PROPERTIES OF THE CU TSVs

To study the mechanical properties of the Cu vias, nanoindentation measurements were carried out on the top of the vias. The BEOL layers were first removed by FIB, then, for several vias of each type, quasi-static indentations were performed using a Hysitron TI 950 TriboIndenter[®] system equipped with a Berkovich diamond tip. A two-segment load versus time profile was used, and the loading/unloading rate was 100 nN/s with a peak load of 800 μ N. The measured load-displacement responses for both TSV-A and TSV-B are shown in Fig. 2. Based on EBSD analysis, both in this study and in other studies,

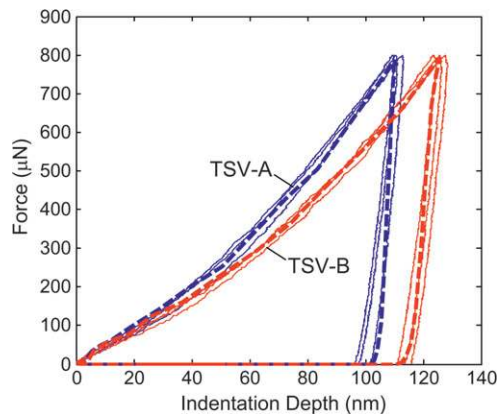


Fig. 2. Load-displacement response from the nanoindentation measurements for TSV-A and TSV-B (solid lines), in comparison with FEA simulations (dashed lines).

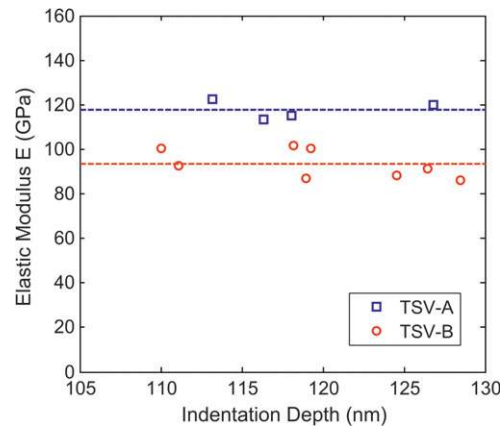


Fig. 3. Elastic modulus extracted from the nanoindentation measurements.

grain distribution in TSVs is random with no specific texture in the TSV [8, 11, 12]. The property measured from the top of the via provided a reasonable estimation of the overall via property [11] and was used in the following discussion. Using the Oliver-Pharr method [13], the elastic moduli of the vias were deduced from the unloading curves and plotted in Fig. 3. The average elastic modulus was found to be 117 GPa for TSV-A and 93 GPa for TSV-B. The elastic modulus of TSV-B was lower than what typically expected for electroplated Cu (\sim 110 GPa) [14], which may be related to the grain textures near the top surface of the via.

To deduce the plastic properties of the Cu vias, finite element analysis (FEA) was conducted. An axisymmetric FEA model was built to simulate the nanoindentation process with a diamond tip (Fig. 4). For the diamond tip and Si, the material properties used were $E_i = 1222$ GPa, $\nu_i = 0.2$, and $E_{Si} = 130$ GPa, $\nu_{Si} = 0.28$, respectively. For the Cu vias, $\nu_{Cu} = 0.35$ and the average elastic moduli obtained from the nanoindentation measurements were used. The interface between Cu and Si is assumed to be perfectly bonded.

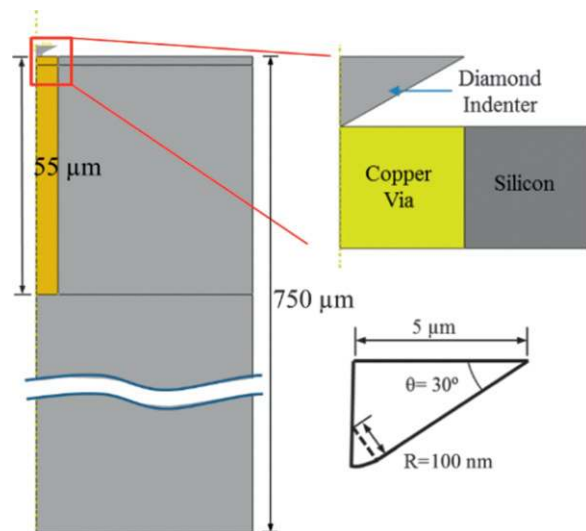


Fig. 4. Finite element simulations of the nanoindentation process with a diamond indenter.

A classical metal plasticity model in ABAQUS [15] with Mises yield surface and isotropic hardening was used to model plasticity in the Cu vias. The yield stress was specified as a function of plastic strain:

$$\sigma_y(\bar{\epsilon}_p) = \sigma_{y0} \left[1 + \frac{7E\bar{\epsilon}_p}{3\sigma_{y0}} \right]^{1/n} \quad (1)$$

where σ_{y0} is the initial yield strength, $\bar{\epsilon}_p$ is the equivalent plastic strain, and n is the hardening exponent. Using an iterative approach comparing the FEA simulations and the nanoindentation experiments, the hardening exponent n were deduced to be $n = 9.5$ for both vias. The initial yield strength σ_{y0} was 250 MPa for TSV-A and 190 MPa for TSV-B (Fig. 2). The lower yield strength for TSV-B was qualitatively consistent with the theoretical expectation based on the Hall–Petch relation, which states that the yield strength decreases with increasing grain size due to grain boundary strengthening.

VIA EXTRUSION

Via extrusion and damage of the BEOL layers were observed for both types of TSVs. The extent of the via extrusion was measured at the via cross section based on high-resolution scanning electron microscope images. On average, the extrusion was 117 nm for TSV-A and 147 nm for TSV-B. In Fig. 5, the grain size and extrusion were plotted for both TSVs. The amount of via extrusion for TSV-B was about 25% larger than for TSV-A, showing clear correlation to the average grain size of the Cu via. For TSV-A, which had smaller and more uniform grains, the amount of via extrusion was smaller than TSV-B. The difference could be traced to the different mechanical properties of the via due to the different grain structures resulted from the different processing conditions. The observed correlation suggests that TSVs with uniform small grains would be more favorable to have reduced via extrusion.

MODELING OF VIA EXTRUSION

To help understand the effects of mechanical properties on via extrusion, a simple analytical model was formulated [9], followed by FEA. In both the analytical model and FEA, a thermal cycle from the room temperature (T_R) to a high process temperature (T_H) and then back to the room temperature was considered, corresponding to a thermal load $\Delta T = T_H - T_R$ for the TSVs. First, assuming a free sliding interface, the mis-

match of thermal expansion between the Cu via and Si induces a biaxial compressive stress in Cu upon heating:

$$\sigma_r = \sigma_\theta = -\Delta T(\alpha_{Cu} - \alpha_{Si}) \left(\frac{1 - \nu_{Cu}}{E_{Cu}} + \frac{1 + \nu_{Si}}{E_{Si}} \right)^{-1} \quad (2)$$

where α_{Cu} and α_{Si} are the coefficients of thermal expansion for Cu and Si, respectively. The stress induces an elastic strain in the axial direction of the via, which results in an elastic extrusion ΔH_e at the high temperature T_H :

$$\begin{aligned} \frac{\Delta H_e}{H} &= \epsilon_{z,Cu} - \epsilon_{z,Si} \\ &= \Delta T(\alpha_{Cu} - \alpha_{Si}) \left(1 + \frac{2\nu_{Cu}}{E_{Cu}} \left(\frac{1 - \nu_{Cu}}{E_{Cu}} + \frac{1 + \nu_{Si}}{E_{Si}} \right)^{-1} \right) \end{aligned} \quad (3)$$

where H is the via height. The elastic extrusion increases linearly with temperature as $\Delta H_e = \beta_e H \Delta T$, with $\beta_e = 20.64$ ppm/ $^\circ\text{C}$ obtained using the typical values for the thermomechanical properties of Cu and Si ($\alpha_{Cu} = 17$ ppm/ $^\circ\text{C}$, $\alpha_{Si} = 2.3$ ppm/ $^\circ\text{C}$, $E_{Cu} = 110$ GPa, $E_{Si} = 130$ GPa, $\nu_{Cu} = 0.35$, and $\nu_{Si} = 0.28$).

If plastic yielding were absent in Cu, the elastic via extrusion would decrease with the same rate upon cooling and vanish at the room temperature after a full thermal cycle. On the other hand, assuming perfect plasticity with a yield strength σ_y for the Cu via, plastic yielding of Cu is predicted when heating above a critical temperature

$$\Delta T_y = \frac{\sigma_y}{\alpha_{Cu} - \alpha_{Si}} \left(\frac{1 - \nu_{Cu}}{E_{Cu}} + \frac{1 + \nu_{Si}}{E_{Si}} \right) \quad (4)$$

which is proportional to the yield strength of Cu. Beyond the critical temperature ($\Delta T > \Delta T_y$), the Cu via deforms plastically, resulting in a plastic extrusion ΔH_p :

$$\frac{\Delta H_p}{H} = (3\alpha_{Cu} - 2\alpha_{Si})(\Delta T - \Delta T_y) \quad (5)$$

The plastic extrusion also increases linearly with temperature, but with a higher rate as, $\Delta H_p = \beta_p H (\Delta T - \Delta T_y)$, where $\beta_p = 46.4$ ppm. The plastic extrusion rate is more than twice that of the elastic extrusion rate, leading to more significant via extrusion at high temperatures. More importantly, the plastic

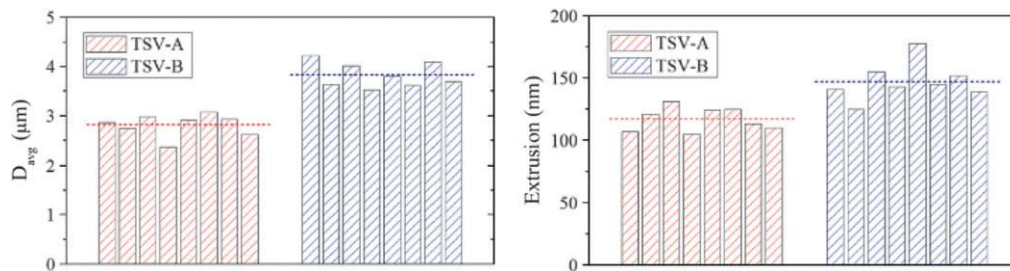


Fig. 5. Correlation between grain size and via extrusion for TSV-A and TSV-B.

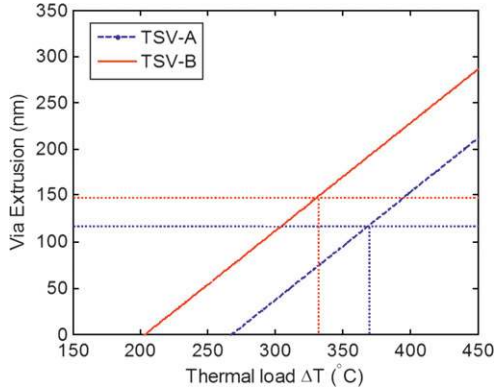


Fig. 6. Via extrusion versus maximum process temperature predicted by the analytical model.

extrusion does not vanish after cooling, resulting in a nonzero residual extrusion, ΔH_r , after a full thermal cycle:

$$\Delta H_r = H(\beta_p - \beta_c)(\Delta T - \Delta T_y) \quad (6)$$

The analysis shows that the magnitude of the residual extrusion depends on the highest temperature during the thermal cycle and the plastic yield strength of the Cu via. Increasing the yield strength of Cu would increase the yield temperature, ΔT_y , and thus decrease the residual extrusion for the same thermal load of ΔT .

Using the mechanical properties obtained from the nano-indentation experiments, the magnitude of via extrusion versus the maximum processing temperature are calculated and plotted in Fig. 6 for both TSV-A and TSV-B. Since the yield strength is lower for TSV-B, the critical thermal load for via extrusion is lower. For the same thermal load ($\Delta T > \Delta T_y$), the analytical model predicts that the amount of via extrusion for TSV-B is higher than that for TSV-A, consistent with the experimental observations (Fig. 5).

An axisymmetric FEA model similar to that in Fig. 4 was constructed to simulate the via extrusion during a thermal cycle, also using the elastic-plastic properties extracted from nanoindentation. As shown in Fig. 7, the numerical results were consistent with the analytical model, showing the residual via extrusion after the thermal cycle was higher for TSV-B

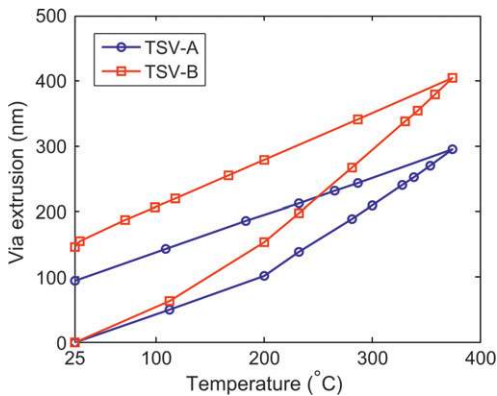


Fig. 7. FEA simulations of via extrusion during a thermal cycle for TSV-A and TSV-B.

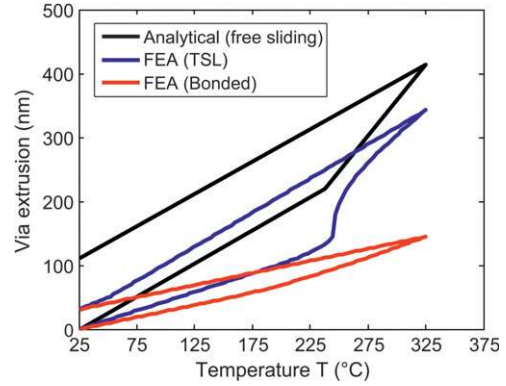


Fig. 8. Comparison of via extrusion for different interfacial properties: free sliding, perfect bonding, and cohesive with a bilinear TSL.

than for TSV-A for the same thermal load $\Delta T = 350^\circ\text{C}$. It was found that the analytical model slightly overestimated the via extrusion due to the assumption of perfect plasticity and uniform stress field in the Cu vias.

In the end, the effect of interfacial properties on Cu extrusion was analyzed by FEA considering two different bonding behaviors at the via/liner interface. The first case assumed a perfectly bonded interface between the via and silicon, the second case considered weaker interface modeled by a bilinear traction-separation law at the interface. The calculated via extrusion during a thermal cycle was plotted in Fig. 8. When the via/Si interface was perfectly bonded, the residual extrusion was significantly reduced, by $\sim 3\times$, at room temperature, compared to the analytical model, which assumed free sliding at the interface. This suggests that the contribution of plasticity to extrusion was reduced by the strong interfacial bonding between via and silicon. For the second case, assuming a cohesive via/Si interface with an adhesion energy of 2.5 J/m^2 and a shear strength of 50 MPa, the via extrusions at both room temperature and maximum temperatures were considerably higher than that for the bonded case although still lower than that predicted by the analytical model. The analysis shown in Fig. 8 indicates that both the Cu plasticity and interfacial adhesion affect the via extrusion and therefore should be considered in process optimization.

CONCLUSIONS

In summary, the effect of the average grain size on the elastic-plastic properties of Cu TSV has been examined and correlated to via extrusion based on two TSV structures with different microstructures. It was found that smaller and more uniform grains resulted in higher yield strength and therefore is more favorable for reducing the via extrusion. The effect of interface strength at the Cu/Si interface on extrusion was also studied by modeling analysis. The findings in this study suggest that in the fabrication of TSVs, it will be beneficial to control the processing parameters to achieve more uniform and small grains and stronger interfaces to improve via extrusion reliability.

ACKNOWLEDGMENTS

This work was supported by Semiconductor Research Corp.

REFERENCES

- [1] J. Van Olmen, C. Huyghebaert, J. Coenen, J. Van Aelst, E. Sleeckx, A. Van Ammel, S. Armini, G. Katti, J. Vaes, W. Dehaene, E. Beyne, and Y. Travalay, "Integration challenges of copper through silicon via (TSV) metallization for 3D-stacked IC integration," *Microelectronic Engineering*, Vol. 88, No. 5, pp. 745-748, 2010.
- [2] S. Kang, S. Cho, K. Yun, S. Ji, K. Bae, W.S. Lee, E. Kim, J. Kim, H. Mun, and Y.L. Park, "TSV optimization for BEOL interconnection in logic process," Proceedings of the IEEE International 3D Systems Integration Conference (3DIC), pp.1-3, 2012.
- [3] I. De Wolf, K. Croes, O. Varela Pedreira, R. Labie, A. Redolfi, M. Van De Peer, K. Vanstreels, C. Okoro, B. Vandevelde, and E. Beyne, "Cu pumping in TSVs: effect of pre-CMP thermal budget," *Microelectronics and Reliability*, Vol. 51, pp. 1856-1859, 2011.
- [4] A. Heryanto, W.N. Putra, A. Trigg, S. Gao, W.S. Kwon, F.X. Che, X.F. Ang, J. Wei, R.I. Made, C.L. Gan, and K.L. Pey, "Effect of copper TSV annealing on via protrusion for TSV wafer fabrication," *Journal of Electronic Materials*, Vol. 41, No. 9, pp. 2533-2542, 2012.
- [5] J. De Messemaeker, O.V. Pedreira, B. Vandevelde, H. Philipsen, I. De Wolf, E. Beyne, and K. Croes, "Impact of post-plating anneal and through-silicon via dimensions on Cu pumping," Proceedings of the IEEE Electronic Components and Technology Conference, pp. 586-591, 2013.
- [6] S.K. Ryu, T. Jiang, K.H. Lu, J. Im, H.-Y. Son, K.-Y. Byun, R. Huang, and P.S. Ho, "Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique," *Applied Physics Letters*, Vol. 100, p. 041901, 2012.
- [7] D. Zhang, K. Hummler, L. Smith, and J.-Q. Lu, "Backside TSV protrusion induced by thermal shock and thermal cycling," Proceedings of the IEEE Electronic Components and Technology Conference, pp. 1407-1413, 2013.
- [8] T. Jiang, S.K. Ryu, Q. Zhao, J. Im, R. Huang, and P.S. Ho, "Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon vias," *Microelectronics and Reliability*, Vol. 53, pp. 53-62, 2013.
- [9] T. Jiang, C. Wu, L. Spinella, J. Im, N. Tamura, M. Kunz, H.-Y. Son, B.G. Kim, R. Huang, and P.S. Ho, "Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects," *Applied Physics Letters*, Vol. 103, p. 211906, 2013.
- [10] S.K. Ryu, T. Jiang, J. Im, P.S. Ho, and R. Huang, "Thermo-mechanical failure analysis of through-silicon via interface using a shear-lag model with cohesive zone," *IEEE Transactions on Device and Materials Reliability*, Vol. 14, pp. 318-326, 2014.
- [11] C. Okoro, K. Vanstreels, R. Labie, O. Lühn, B. Vandevelde, B. Verlinden, and D. Vandepitte, "Influence of annealing conditions on the mechanical and microstructural behavior of electroplated Cu-TSV," *Journal of Micromechanics and Microengineering*, Vol. 20, p. 045032, 2010.
- [12] H. Kadota, R. Kanno, M. Ito, and J. Onuki, "Texture and grain size investigation in the copper plated through-silicon via for three-dimensional chip stacking using electron backscattering diffraction," *Electrochem Solid State*, Vol. 5, No. 14, pp. D48-D51, 2011.
- [13] W.C. Oliver and G.M. Pharr, "Measurement of hardness and elastic modulus by instrumented indentation: advances in understanding and refinements to methodology," *Journal of Materials Research*, Vol. 19, No. 1, pp. 3-20, 2004.
- [14] D.W. Gan, R. Huang, P.S. Ho, J. Leu, J. Maiz, and T. Scherban, "Isothermal stress relaxation in electroplated Cu films. I. Mass transport measurements," *Journal of Applied Physics*, Vol. 97, p. 103531, 2005.
- [15] *ABAQUS Theory and Analysis User's Manuals (Version 6.13)*, Dassault Systèmes Simulia Corp., Providence, RI, 2013.