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Research Article

Impact of Interface Traps on Direct and Alternating Current in Tunneling Field-Effect Transistors

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We demonstrate the impact of semiconductor/oxide interface traps (ITs) on the DC and AC characteristics of tunnel field-effect transistors (TFETs). Using the Sentaurus simulation tools, we show the impacts of trap density distribution and trap type on the n-type double gate- (DG-) TFET. The results show that the donor-type and acceptor-type ITs have the great influence on DC characteristic at midgap. Donor-like and acceptor-like ITs have different mechanism of the turn-on characteristics. The flat band shift changes obviously and differently in the AC analysis, which results in contrast of peak shift of Miller capacitor C_{gd} for n-type TFETs with donor-like and acceptor-like ITs.

1. Introduction

Tunneling field-effect transistor (TFET) is one of low-power electronics due to lower off-current and steeper slope. The mechanism of tunneling current was produced by band-to-band tunneling (BTBT) in a TFET, so TFET device can break the fundamental subthreshold swing (SS) limit of MOSFET [1–3]. Owing to its extremely low off-state current, the turn-on characteristic of TFET would be superior to MOSFET. Therefore, TFET devices can be recognized as one of the most possible candidates of MOSFETs [4–9]. However, TFET has a drawback of low on-state current (I_{on}). To solve this issue, high-κ dielectric was proposed to enhance I_{on} [10]. Unfortunately, the semiconductor/oxide interface quality is severely tested, and the existence of ITs could introduce instability. Besides, it was not clear how interface traps (ITs) can influence TFET performance [11–15]. What is more, they did not explain influence machine of Miller capacitance and power dissipation. Resolving this issue is important not only to better understand the device operation but also to further research the impacts of interface traps on turn-on and capacitance characteristics of TFETs. In this paper, we address a detailed investigation of the role of trap type, trap density, and trap energy levels on dependence of DG-TFET characteristics with HfO_2 high-κ gate insulator.

2. Device Model and TCAD Simulation

In this paper, the investigated device structure for the DG n-channel tunnel field-effect transistor (n-TFET) is shown in Figure 1. The device structure consists of a highly doped p-region (10^{20} atoms·cm^{-3}), a lightly doped intrinsic region (10^{16} atoms·cm^{-3}), and a highly doped n-region (10^{20} atoms·cm^{-3}). The intrinsic region acts as the channel, p-region acts as the source, and n-region acts as the drain and all lengths are 50 nm. The bulk Si thickness (T_{Si}) is 10 nm, the high-κ gate insulator thickness (T_{ox}) is 2 nm, and gate work function Φ is 4.0 eV. According to the uniform electric field limit and Kane's model, the band-to-band tunneling (BTBT) generation rate G is $G = A(F/F_0)^P \exp(-B/F)$, $A = g(m_c m_v)^{3/2}(1 + 2N_{TA})D_{TA}^2(qF_0)^{5/2}/2^{21/4}h^{5/2}m_r^{5/4}\rho\varepsilon_{TA}E_g^{7/4}$, $B = 2^{7/4}\pi m_r^{1/2}E_g^{3/2}/3qh$, and $P = 2.5$ for the indirect tunneling [16]. Specifying $\varepsilon_{TA} > 0$ selects the phonon-assisted tunneling process for Si. The results A and B are 1.4×10^{20} cm^{-3} s^{-1} and 1.12×10^8 V/cm, respectively. For the phonon-assisted tunneling process, the prefactor A and the exponential factor B take into account the material characteristics and external condition (such as optical phonon scattering (OP) and acoustic phonon scattering (AP)). Obviously, the factor B has more impact than A.

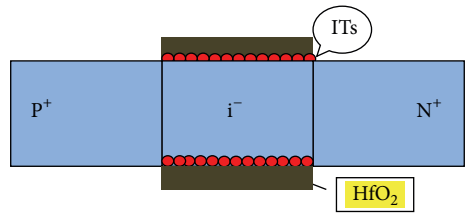

Figure 1: Device structures of n DG-TFET with steep doping profiles.

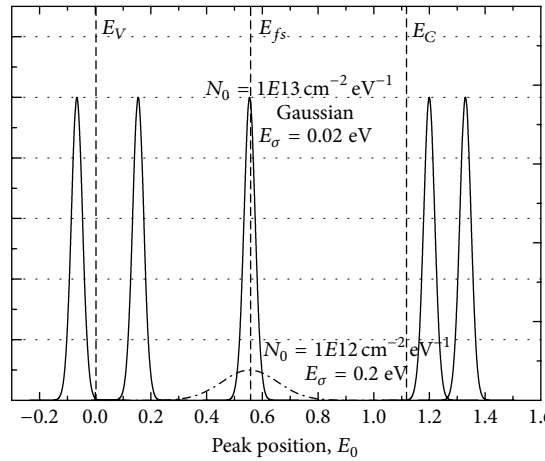

Figure 2: High and low Gaussian distributions are $E_\sigma = 0.02$ and 0.2, which have 1×10^{13} cm^{-2} eV^{-1} and 1×10^{12} cm^{-2} eV^{-1} interface traps concentration, respectively. The peak position of Gaussian distribution ranges from E_v to E_c and extends beyond the forbidden band.

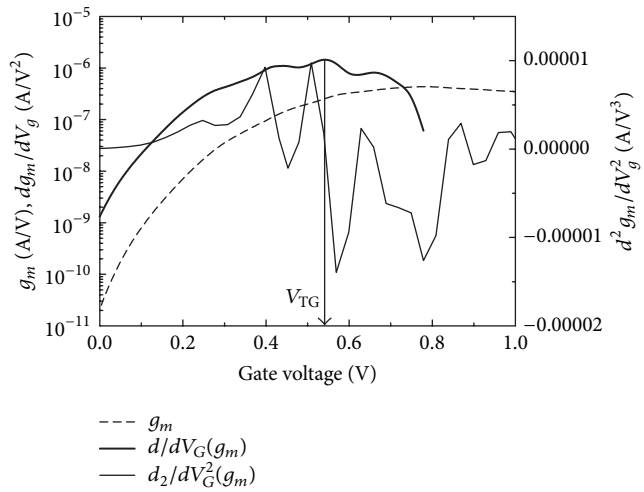

Figure 3: First derivative of drain current is g_m, its second derivative is dg_m/dV_g, and its third derivative is dg_m^2/dV_g^2; $V_{DS} = 0.5$ V; the channel length is 50 nm.

In order to make simulation results more reliable, the doping-dependent mobility model, the dynamical nonlocal-path band-to-band tunneling (BTBT) model, the modified local-density approximation (MLDA) model, the surface SRH recombination model, and the Schenk trap-assisted tunneling (TAT) model are included.

Because high electric fields and silicon process can cause hot-carrier injection (HCI) effects and traps in this semiconductor/oxide interface, we assume that these localized ITs were just located at Si/HfO_2 interface and the capture cross section σ ($\sigma_n = \sigma_p$) is 10^{-14} cm^{-2}, as shown in Figure 1. The trap energy and trap distribution consist of the high and low Gaussian distributions, and the peak position (E_0) could be moved in the forbidden band. Hereafter, we study the impact of ITs type, ITs energy level position, and ITs distribution on the turn-on DC characteristics. Besides, AC characteristics were also studied, including the impact of concentrations and type of ITs on Miller capacitance (C_{gd}).

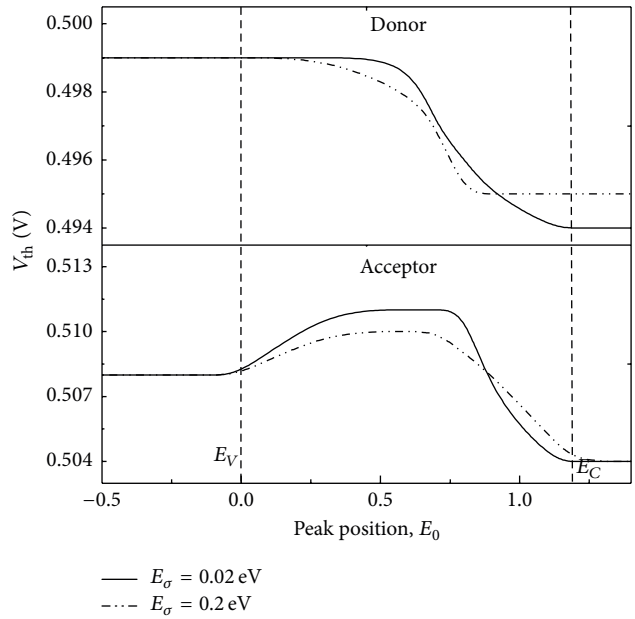

FIGURE 4: Threshold voltage V_{th} versus the peak position E_0 of high distribution and low distribution with donor-type ITs and acceptor-type ITs; $V_{GS} = V_{DS} = 0.5$ V.

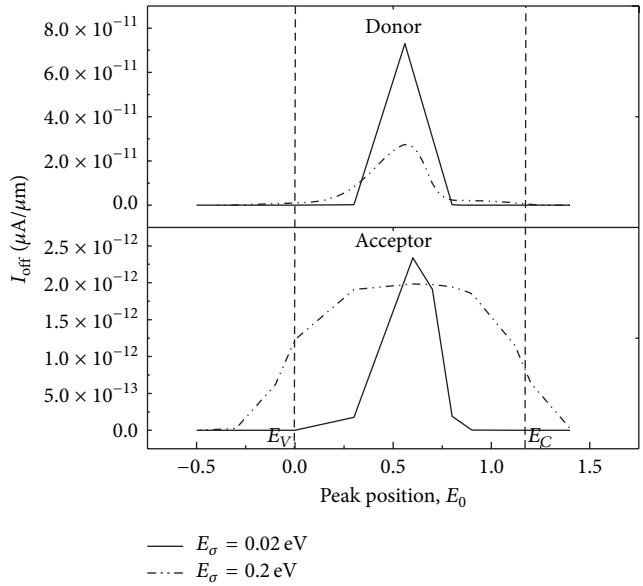

FIGURE 5: The extracted off-state current I_{off} as a function of the peak position E_0 of high distribution and low distribution with donor-type ITs and acceptor-type ITs; $V_{GS} = V_{DS} = 0.5$ V.

3. Results and Discussion

3.1. The Impact of ITs on DC Characteristics of DG-TFET. The high-κ materials have great advantages such as improving the on-state current and reducing the gate leakage current. However, because of the lattice mismatch between HfO_2 and Si, they would introduce many interface state defects by depositing with HfO_2 on nanocrystalline silicon film. It is necessary to discuss issues of the impact of interface traps on the performances of TFETs.

Figure 2 shows two typical Gaussian distributions of ITs energy and peak position. The shape of the Gaussian distribution can be decided by the trap basic vacancy and antisite states. Due to the different proportion of vacancy and antisite states, the thin and tall or fat and short cases are the basic cases. The threshold voltage (V_{th}), the off-state current (I_{off}), the minimum subthreshold swing (miniSS), the on-state current (I_{on}), and I_{on}/I_{off} ration are studied by moving peak position and changing value E_σ of Gaussian distribution. A maximum density $D_{IT}(N_0) = 1 \times 10^{13}\,\text{cm}^{-2}\,\text{eV}^{-1}$ and

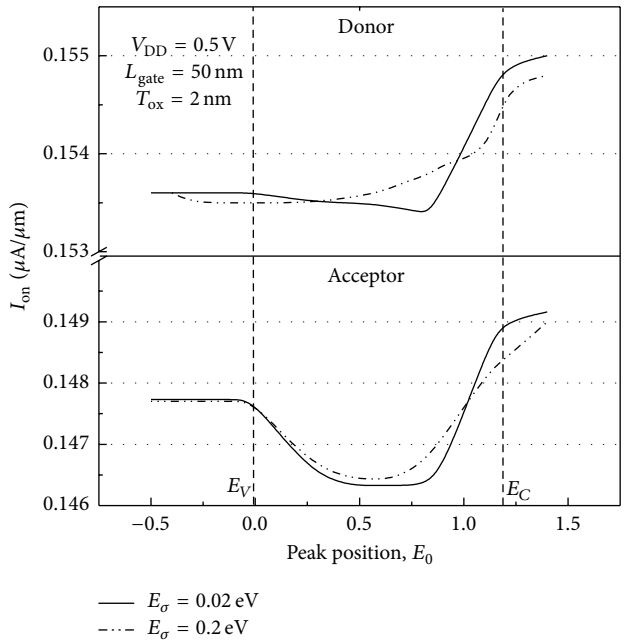

FIGURE 6: The extracted on-state current I_{off} as a function of the peak position E_0 of high distribution and low distribution with donor-type ITs and acceptor-type ITs; $V_{GS} = V_{DS} = 0.5$ V.

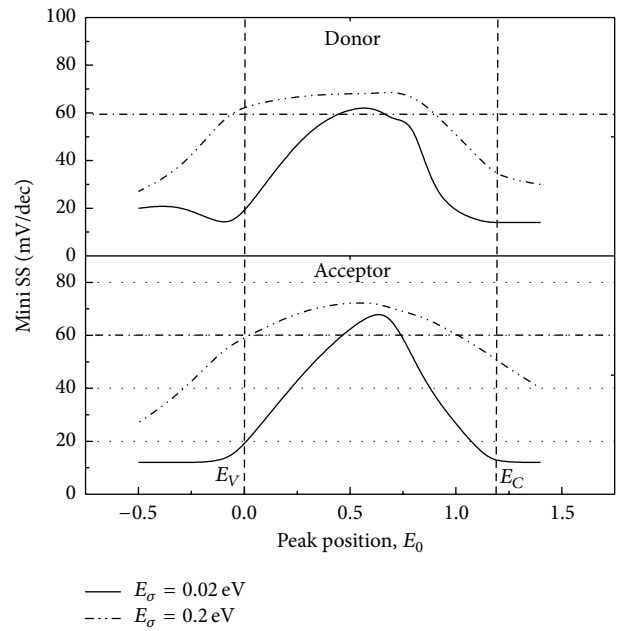

FIGURE 7: Mini SS is extracted as the minimum SS value in the interval between off-state and the threshold voltage V_{th}. Mini SS versus the peak position for DG-TFET at $V_{GS} = V_{DS} = 0.5$ V.

a minimum $D_{IT}(N_0) = 1 \times 10^{12}\,\text{cm}^{-2}\,\text{eV}^{-1}$ are employed. Different trends of two trap types were compared in the following simulation. It is worth noting that V_{th} is extracted with the transconductance change method [17]. The method has definitely physical meaning in Figure 3.

Figure 4 shows the V_{th} shifts in acceptor-type trap and donor-type trap DG n-TFET. The impact of acceptor-type trap on V_{th} is greater than donor-type trap. The donor-type interface traps can make V_{th} smaller from midgap to conduction band (E_c). When the donor-type interface trap level is under the Fermi level, the trap has no effect on V_{th}. Donor-type ITs having lost electrons will be positively charged, which resulted in a small threshold voltage. However, V_{th} will be increased from valence band (E_v) to the Fermi level. This is because acceptor-type ITs capture electron, and then the traps become negatively charged which lead to higher threshold

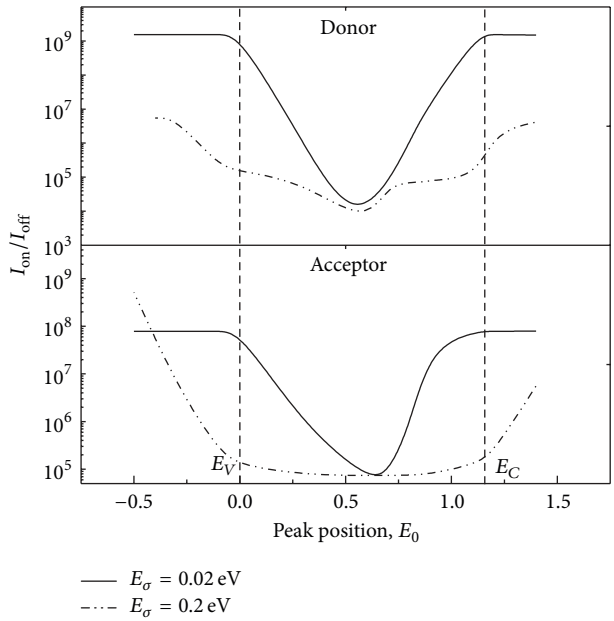

FIGURE 8: Comparison of I_{on}/I_{off} versus the peak position of high and low distribution ITs for DG-TFET.

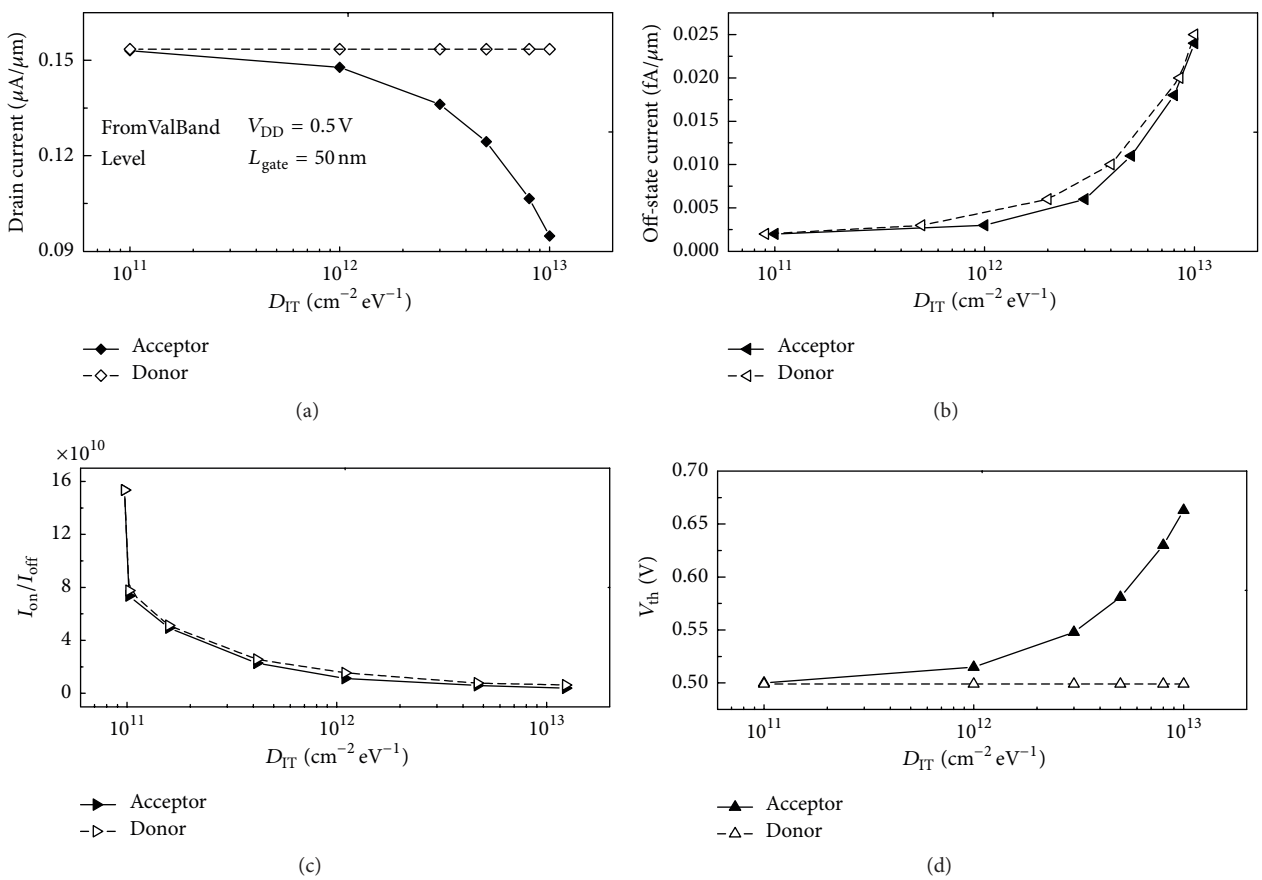

FIGURE 9: (a) Drain current I_{on} at $V_{GS} = V_{DS} = 0.5$ V, (b) off-state I_{off} at $V_{GS} = 0$ V, $V_{DS} = V_{DD} = 0.5$ V, (c) calculated I_{on}/I_{off}, and (d) V_{th} versus ITs density at valence band.

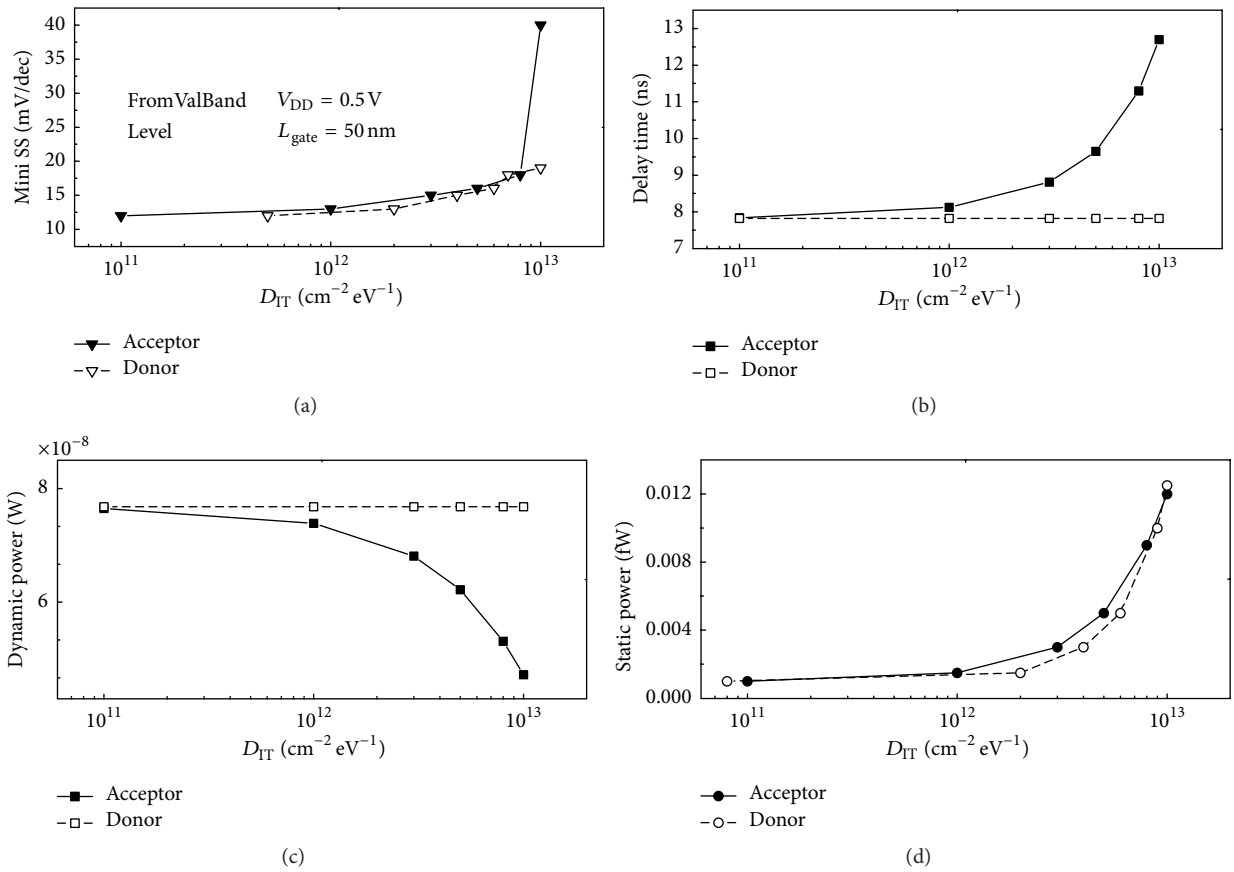

FIGURE 10: (a) The calculated mini SS, (b) delay time, (c) dynamic power, and (d) static power versus ITs density at valence band. Delay time τ is given by $C_L V_{DD}/I_{on}$. The donor-type ITs need more energy in static state than the acceptor-type ITs.

voltage. When acceptor-type trap level goes beyond the Fermi level, the traps having release electrons will be positively charged, which lead to lower threshold voltage again. Besides, it is clearly shown in Figure 4 that small E_σ has more influence than big E_σ.

The extracted off-state current will be increased when traps level is near the Fermi level in Figure 5. The acceptor-type ITs still have greater impact than donor-type. When the trap level is near the Fermi level, the drain-channel junction electric field will be increased (such ambipolar current is not shown under the negative-bias), and this position of trap level would influence electric field gravely between E_v and E_c. It can be observed that donor-type ITs have greater influence than acceptor-type ITs, and the peak position of channel-drain (c/d) tunneling junction field can be determined when traps level was located at midgap, if the electric field appears near the drain end, which results in greater device ambipolar current and off-current. In addition, the low Gaussian distributions of interface trap density E_σ induce smaller peak electric field than high E_σ. It can be seen in Figure 6 that the interface traps can make on-state current degradation between valence band and conduction band. In particular, when the acceptor-like and donor-like traps are located at the energy level 0.3 eV above the Si midgap, the on-state current deteriorates extremely. When ITs are near the channel-source (c/s) junction, they can change the junction electric field. When traps level is below Fermi level, the donor-type ITs cannot release electrons. Thus, I_{on} could hardly be affected.

Meanwhile, because the acceptor-type ITs capture electrons and c/s junction electric field decreases, I_{on} decrease between the valence band and Fermi level. But when acceptor-type ITs level beyond Fermi level can lose electrons, tunneling field would be increased. After donor-type ITs level is higher than the Fermi level and releases electrons, as a result, the tunneling field increases and I_{on} also rise up rapidly. According to the BTBT (Kane's) model, a small change may increase or decrease abruptly the tunneling rate in the electric field.

The minimum (mini) point SS is defined as SS $= 1000/(d/dV_g)\log I_d$ [16]. Figure 7 shows the extracted mini SS. Through the above analysis, the on-state current decreases since the effective source tunneling barrier width increases. The results indicate that the degradation of mini SS is subject to the position of traps level. The source tunneling width attains its maximum value when the traps level is located at Si midgap. It can be seen in Figure 8 that I_{on}/I_{off} rations have reduced between E_c and E_v. On-state current worsens and bipolarity current is produced, which results in smaller value of I_{on}/I_{off} ration for the DG-TFET.

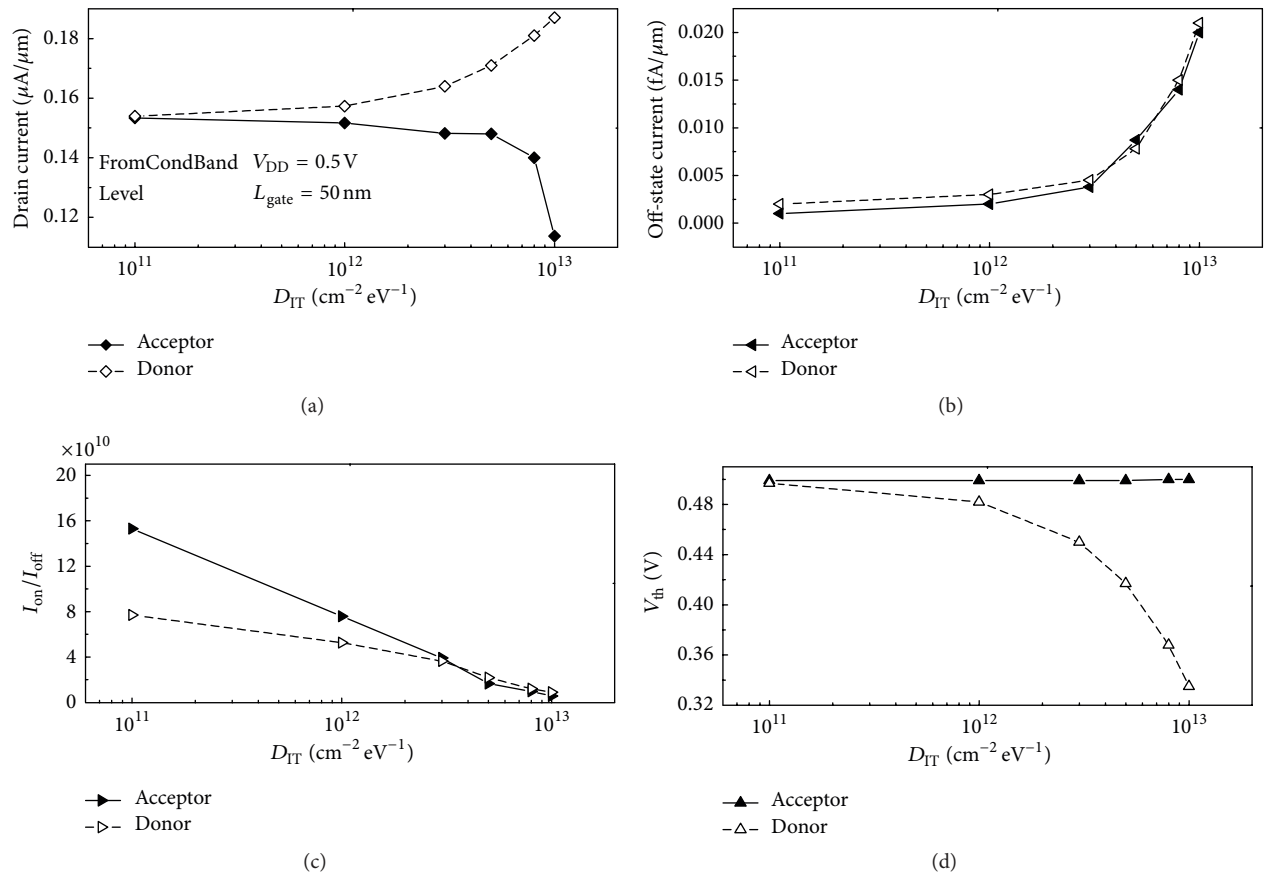

FIGURE 11: (a) Drain current I_{on} at $V_{GS} = V_{DS} = 0.5$ V, (b) off-state I_{off} at $V_{GS} = 0$ V, $V_{DS} = V_{DD} = 0.5$ V, (c) calculated I_{on}/I_{off}, and (d) V_{th} versus ITs density at conduction band. The donor-type ITs contribute to the on-state current which is different from acceptor-type ITs.

In order to get an insight, the impacts of donor-type and acceptor-type ITs density (D_{IT}) located at valence band (FromValBand), middle band (FromMidBandGap), and conduction band (FromCondBand) on drive current were examined. Off-state current, I_{on}/I_{off} ration, threshold voltage (V_{th}), minimum point SS, transistor delay time (τ), dynamic power, and static power were also investigated in Figures 9–14, respectively. For n-type TFETs, the capacitance magnitude is about a few fF/μm. For a DG-TFET device (gate channel length $L_g = 50$ nm, gate width $W = 50$ nm), the TFET capacitance (C_L) is about 9 fF, which is shown in Figure 15 where the maximum capacitance value is obtained in most cases.

We can see in Figures 9–14 that donor-type ITs D_{IT} will not have any effect on the drain current, V_{th}, delay time, and dynamic power. The rough delay time is given by $C_L V_{DD}/I_{on}$ ($V_{DD} = V_{DS} = V_{GS}$), and the dynamic power is roughly obtained by $C_L V_{DD}^2/\tau$. The *DG*-TFET is more immune to donor-type ITs but more susceptible to acceptor-type ITs. It can be seen that the BTBT rate at c/s tunneling junction is not affected obviously by donor-type ITs and I_{on} degradation due to ionized acceptor-type ITs, as shown in Figure 9(a). On the other hand, it is worth noticing that donor-like ITs level is below the Fermi level, and donor-type ITs would not be ionized at the Si midgap (see Figures 13 and 14). Results shown in Figures 9(a) and 13(a) indicate that donor-type ITs D_{IT} slightly increases I_{on}, which confirm the results previously drawn in Figure 6. However, the acceptor-like ITs will capture electrons under the Fermi level and then reduce the c/s tunneling junction field, so the tunneling current decreases with increasing D_{IT}, as shown in Figure 9(a). For DG-TFET, ambipolarity current was increased by increasing donor-like or acceptor-like D_{IT}. However, traps level is in the middle band which has a larger impact than in the valence band. The off-state current can achieve 0.025 fA/μm in the middle band level and 2.75 pA/μm in the valence band level, as observed in Figures 9(b) and 12(b). According to the above study, the on/off ratio can be drawn from Figures 9(a) and 13(a). Figure 9(c) shows that it has a steeper curve than Figure 13(c). It can be explained that the electron probability occupancy is higher in the valence band than in the middle band. Besides, the acceptor-type ITs can influence V_{th} in Si midgap and the donor-type ITs can change V_{th} in both valence band and conduction band, as evident in Figures 9(d), 11(d), and 13(d).

According to the above formula, the donor-like traps would not affect drain current, so τ and dynamic power are nearly invariable. But the acceptor-like traps increase the delay time and reduce the dynamic power, as shown in Figures 10(b), 10(c), 14(b), and 14(c). The donor-type ITs and acceptor-type ITs have the same properties in Figures 10(a),

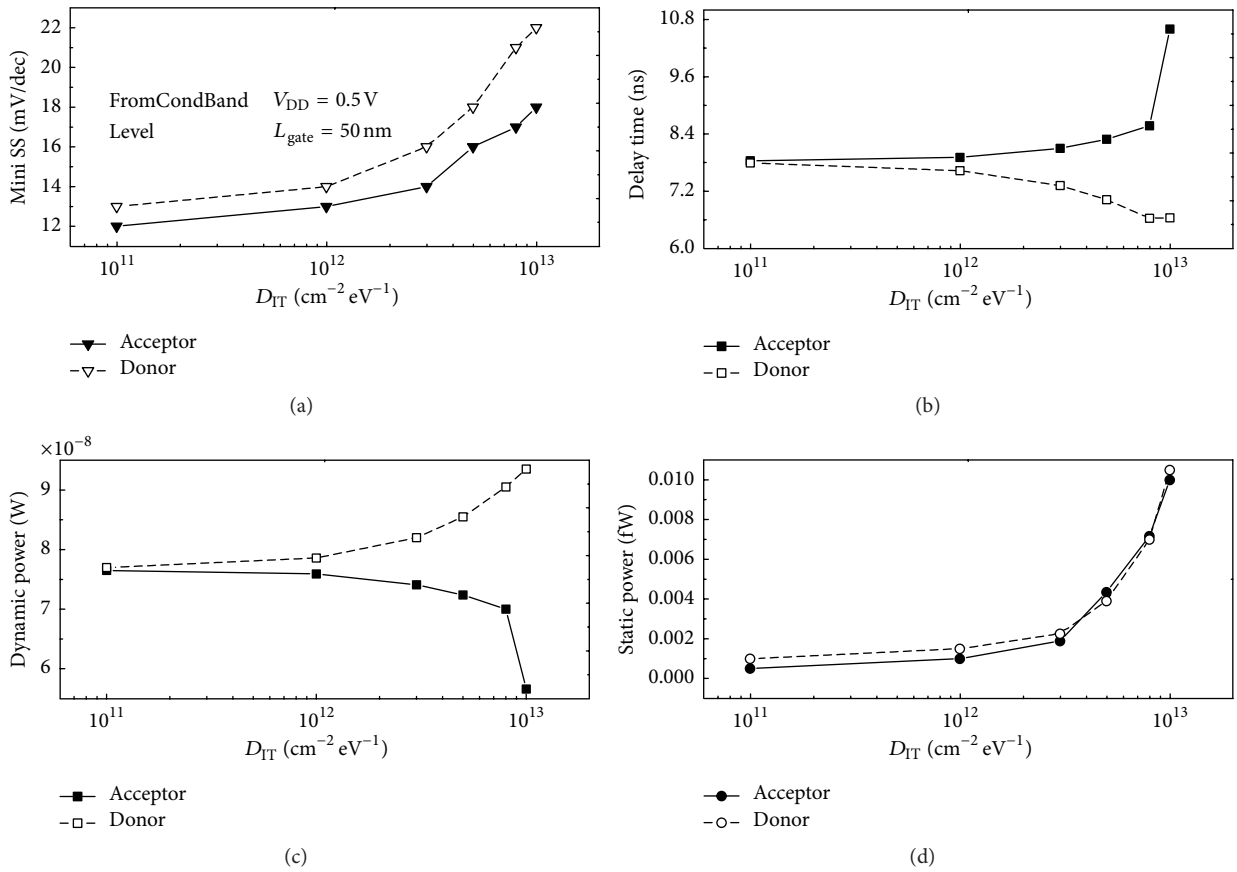

FIGURE 12: (a) The calculated mini SS, (b) delay time, (c) dynamic power, and (d) static power versus ITs density at valence band. Delay time τ is given by $C_L V_{DD}/I_{on}$. The acceptor-type ITs can reduce the dynamic power and the mini SS is more immune to acceptor-type ITs.

10(d), 12(a), 12(d), 14(a), and 14(d). The static power and mini SS would be increased no matter where the ITs level is. Divergent trends in drain current can be seen in Figure 11(a). When traps level is located at the conduction band, drain current would be reduced with increasing acceptor-type D_{IT}. However, drain current increases with increasing donor-type D_{IT}. The simulation results show that the electrons accelerated due to greater tunneling electric field, which was induced through impact ionization. The traps will capture or lose electrons and then weaken or enhance the c/s tunneling junction electric field. The drain current shifts right with increasing the acceptor ITs density. The electrical intensity gradually becomes weak, and then the tunneling carriers decrease. Under the same gate voltage, the tunneling width would not change, so the subthreshold swing would not change obviously. Donor-type ITs inside conduction band can reduce V_{th}. Delay time, dynamic power, and static power have the same changing trend (Figures 12(b), 12(c), and 12(d)).

3.2. The Impact of ITs on Miller Capacitance of DG-TFET. It may be indicated in TFETs that high-κ gate insulator would result in higher fringe capacitance due to the enhanced Miller effects. For the TFET, the gate capacitance is completely controlled by the gate-to-drain capacitance (C_{gd}), C_{gd} makes up a majority of gate capacitance (C_{gg}) [18–20]. For high-κ gate insulator, traps may exist in Si/high-κ dielectric material interface or high-κ dielectric material. In this case, interface traps affect not only tunneling junction electric field but also capacitive characteristics. Next, in order to obtain further insight, we investigate the impact of ITs density (N_{it}), traps type, and traps level on capacitance characteristics of DG-TFET (see Figures 15–17).

This analysis assumes that all trap capture cross sections are 1×10^{-14} cm^{-2}. Small-signal AC analysis is used to analyze the Miller capacitive characteristics (C_{gd}) of DG-TFET, and the scanning frequency is 100 MHz.

Figure 15 shows the simulated C_{gd}-V_{GS} curves with the acceptor-like ITs. Traps are distributed at the energy levels 0.4 eV and 0.6 eV above/below the Si midgap and the Si midgap. When V_{GS} scans to −0.5 V, electrically neutral acceptor-type ITs are in a releasable state and can capture electrons. ITs can contribute to distribution capacitance. The contribution is proportional to ITs density, as shown in Figures 15(b) and 15(c). Later, surface of channel is in strong inversion state and AC small-signal frequency is very high, which results in time not enough for acceptor-type traps to capture electrons. In this case, the traps reduce the contribution of capacitance value. When traps level is located at the Si midgap, Figure 15(c) shows that gate voltage moves

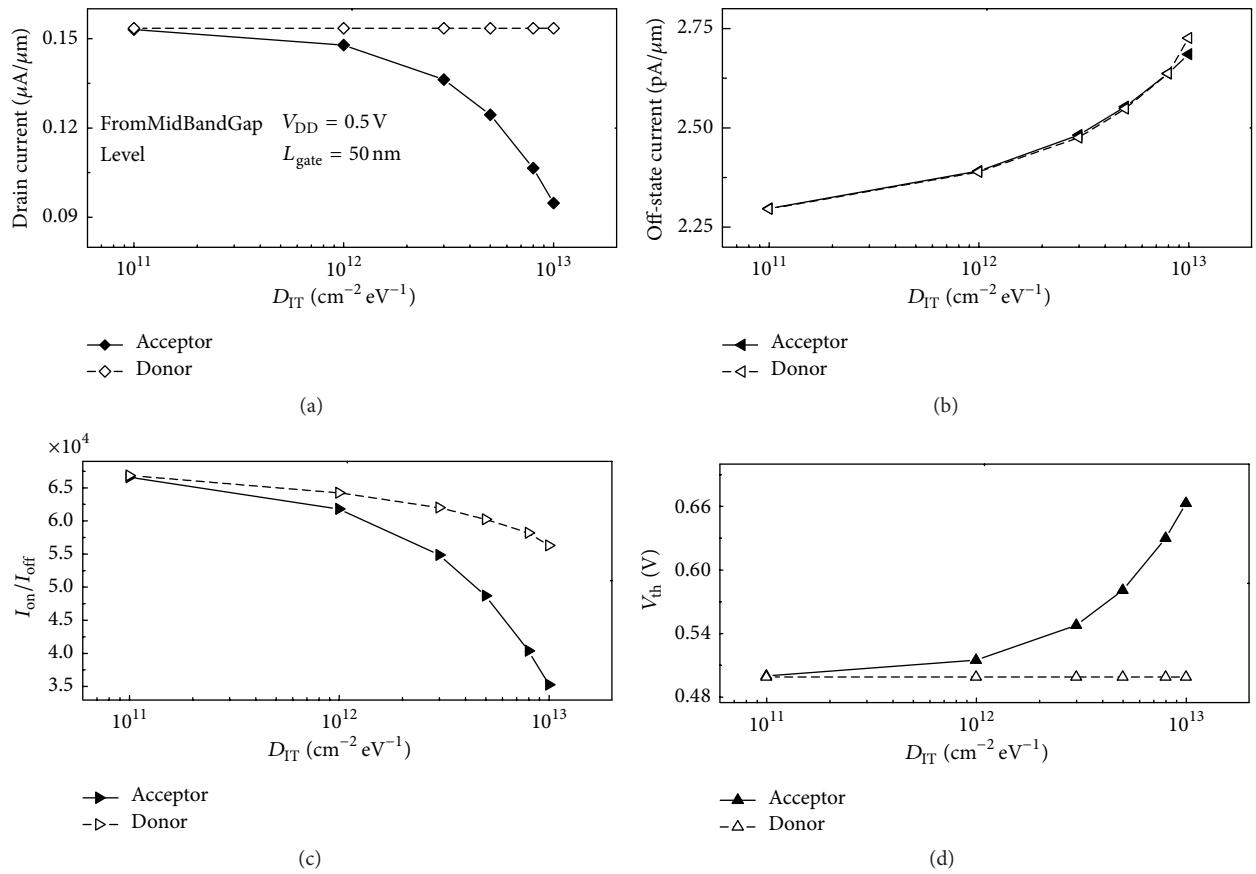

FIGURE 13: (a) Drain current I_{on} at $V_{GS} = V_{DS} = 0.5$ V, (b) off-state I_{off} at $V_{GS} = 0$ V, $V_{DS} = V_{DD} = 0.5$ V, (c) calculated I_{on}/I_{off}, and (d) V_{th} versus ITs density at midgap band. The acceptor-type ITs deteriorates the on-state current which is the same effect at E_c and E_v.

left corresponding to the maximum capacitance contribution value. It is, however, necessary to note that, in Figure 15(c), the maximum capacitance contribution value is also down when traps distribute from E_c to midgap. In addition, the change trend is obvious when $N_{it} = 1 \times 10^{13}$ cm^{-2} eV^{-1}. Gate voltage changes from −1 V to 1 V, and the Fermi level moves from E_v to E_c. Because the Fermi level is below Si midgap, the acceptor-type traps will not capture electrons, which results in having no effect on C_{gd}.

When the Fermi level reaches the Si midgap, the acceptor-type traps begin to capture electrons and make a significant contribution to C_{gd}. With the raising of Fermi level, it enhances capacitance contribution. The position of the Fermi level moves down and improvement of the surface potential is due to negatively charged acceptor-type traps, which results in reduction of capacitance contribution.

The peak point shift of distribution capacitance between donor- and acceptor-type trap is different. The formation energies (E_{form}) $E_{form} = E_0 - qE_F$, and q is the charged defects of charge. Capturing or releasing electrons can result in positive and negative E_{form}, so the Fermi energy can reach firstly the formation energies of the donor-like trap. At the same time, $N_{it} \propto \exp(-E_{form}/kt)$. δE_{form} increase with increasing N_{it}, and the greater the density, the greater the contribution to distribution capacitance. When V_{GS} is less than 0.5 V, distribution capacitance attains its peak value for higher density.

For the acceptor-like trap, the more the negative E_{form} is, the later it reaches the maximum distribution capacitor. It is the same for the donor-like trap; the greater the density, the greater the contribution of acceptor-like to distribution capacitance.

Figure 15(e) shows an extreme case where traps level is located at energy 0.6 eV below the Si midgap, as shown in Figure 15(d). ITs level has been completely shifted in E_v, which means that Fermi level is always higher than ITs level. Traps can be fully filled by electrons, and then the flat voltage (V_{FB}) will turn right, which indicates that ITs of Si/HfO_2 have the same effect with the fixed charges. On the other hand, C_{gd} shift right with increasing traps concentration.

For oxide bulk trap, there are usually a lot of positive fixed charge hydrogen ions (H^+) in insulation, and C-V curve moves in the direction of the negative axis. In contrast to C_{gd} curves in Figure 15(e), the acceptor-like trap has the same effect as the negative interface fixed charge trap, and C-V curve moves to the opposite direction. The final effect is the flat band shift. The only difference is the drift direction.

The plots of gate-drain capacitance as a function of V_{GS} for five different level positions of donor-type ITs are shown in Figure 16. Donor-type ITs energy levels are occupied totally

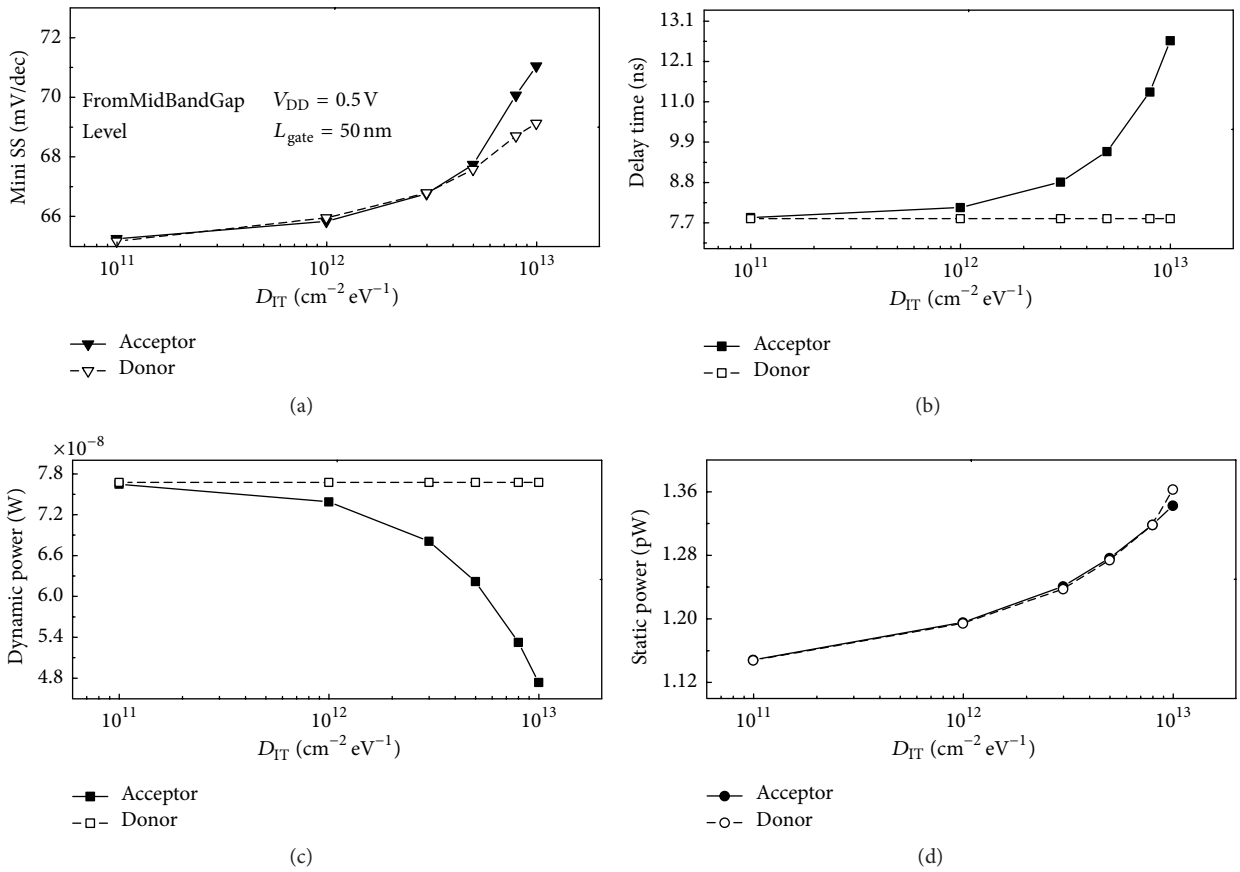

FIGURE 14: (a) The calculated mini SS, (b) delay time, (c) dynamic power, and (d) static power versus ITs density at valence band. Delay time τ is given by $C_L V_{DD}/I_{on}$. The acceptor and acceptor-type ITs are essentially the same effect at midgap band and valence band.

by electrons, so that ITs are electrically neutral. After liberating electrons, the ITs are positive. Figure 16(a) shows that the ITs levels are distributed at the energy level 0.6 eV above the midgap; the Fermi level is under trap level. The result indicates that ITs exert an influence on Miller capacitance. When the gate voltage V_{GS} changes from −1.0 V to 0.2 V, then the Fermi level keeps rising relative to traps level. The influence of traps level on C_{gd} would be shifted left with lowering of the trap level position, as shown in Figures 16(a), 16(b), and 16(c). V_{GS} reaches to −0.6 V, and the Fermi level is near the trap level. The donor-type ITs begin to exchange electrons with channel in Figure 16(d). When the traps level is distributed at the energy level 0.3 eV under the midgap, it can be seen clearly in Figure 16(e) that C_{gd} is hardly affected. C_{gd} fluctuated by donor-type ITs is smaller than acceptor-type ITs, which implies that DG-TFET is more immune to donor-type ITs. Besides, it is found that the peak position shifts left for donor-type ITs and shifts right for acceptor-type ITs.

It is worth noticing that the impact of the different energy distribution of charged traps on Miller capacitance is also necessary to be studied. We assume that the peak concentration of interface traps (donor-type and acceptor-type) is 5×10^{12} cm^{-2} eV^{-1}, and four types of energetic distribution (level, uniform, exponential, and Gaussian) are located at E_i + 0.4 eV, E_i, and E_i − 0.4 eV, respectively. High Gaussian distributions (E_σ0.2) are adopted, as shown in Figure 17 and Figure 18. First, it was found that the signal level of acceptor or donor traps has the most effect on the C-V curve in Figures 17(a) and 18(a). The shape of ITs energy density distribution has a great influence on capacitance contribution. The smoother the curve is, the smaller the capacitance contribution value is. Due to variations in the positions of traps level and the Fermi level, the electron occupation rate of ITs is different. The greater the occupation chance of ITs is, the more obvious the capacitance effect is. For the uniform, exponential, and Gaussian distribution of ITs, the capacitance effects are almost alike, as shown in Figures 17(b) and 18(b). However, the ITs level is located at the energy level 0.4 eV under the midgap, and the impact of the exponential and Gaussian distribution of ITs is obviously different, as shown clearly in Figure 17(c) and Figure 18(c). In addition, it is clearly shown in Figures 17 and 18 that the effect of acceptor-type ITs on C_{gd} is still more obvious than that of donor-type ITs:

$$C_{ITs} \propto D_{IT} f'_{it}, \tag{1}$$

where C_{ITs} is ITs capacitance contribution and D_{IT} and f'_{it} are ITs density and derivative of occupation rate of ITs,

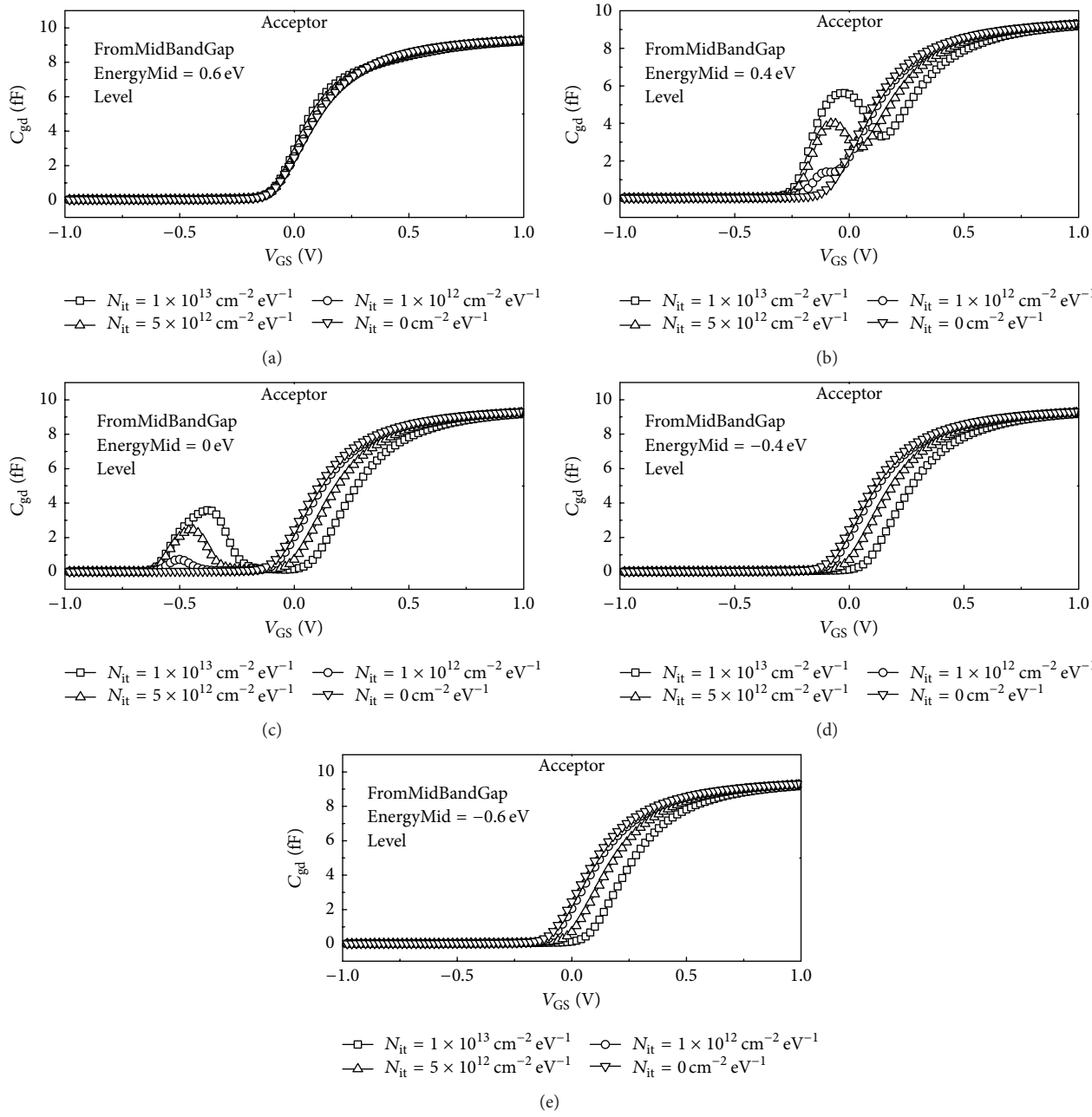

FIGURE 15: Five C-V curves of a single level ITs are plotted. Miller capacitance C_{gd} of DG-TFET for acceptor-type ITs is studied at $V_{DS} = 0.5$ V with variable ITs density N_{it}. (a) The trap is distributed at the energy level 0.6 eV above the midgap, (b) at the energy level 0.4 eV above the midgap, (c) at the midgap, (d) at the energy level 0.4 eV under the midgap, and (e) at the energy level 0.6 eV under the midgap.

respectively. The electron occupancy probability of donor-type or acceptor-type ITs can be expressed as

$$f_{it}(E) = \frac{1}{1 + (1/g)\exp\left((E_{it} - E_F)/kT\right)}, \tag{2}$$

where E_{it} is ITs energy; g is a degeneracy factor; k is Boltzmann's constant; and T is temperature. As mentioned above, the derivative of electron occupation of ITs can be given as follows:

$$f'_{it} = \frac{1}{1 + (1/g)\exp\left((E_{it} - E_F)/kT\right)^2}\frac{1}{g} \cdot \exp\left(\frac{E_{it} - E_F}{kT}\right)E'_{it}. \tag{3}$$

According to formula (3), it can be found that ITs contribute a lot to C_{gd} for fixed relative positions between ITs level and the Fermi level, where E'_{it} is relatively large.

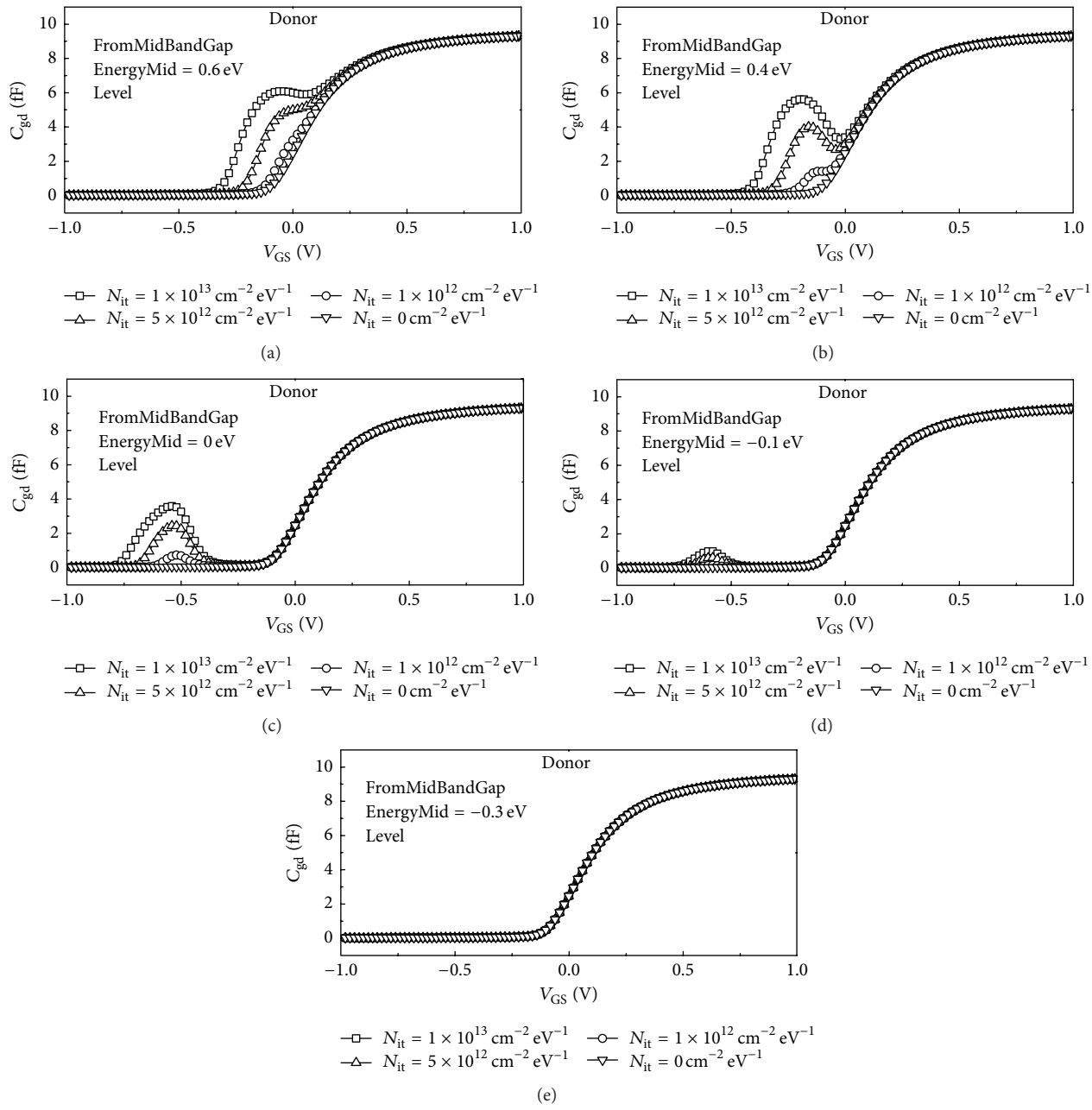

FIGURE 16: Miller capacitance C_{gd} of DG-TFET for donor-type ITs is studied at $V_{DS} = 0.5$ V with variable ITs density N_{it}. (a) The trap is distributed at the energy level 0.6 eV above the midgap, (b) at the energy level 0.4 eV above the midgap, (c) at the midgap, (d) at the energy level 0.4 eV under the midgap, and (e) at the energy level 0.6 eV under the midgap.

4. Conclusion

The impact of donor-type and acceptor-type ITs density with different levels and distributions on DC and AC characteristics has been investigated. Peak position of traps is located between E_v and E_c which results in degradation of I_{on}/I_{off} ratio. In particular, the attenuation of tunneling current is fierce when the ITs are distributed at the Si midgap. The donor-type ITs are with the valence band and the Si midgap, which would not affect the drain current, the threshold voltage, delay time, and dynamic power. However, the donor-type ITs and acceptor-type ITs in the conduction band exhibited an opposite trend, and the donor-type ITs have contributed to the drain current. In addition, the impacts of the different types and energy level positions of ITs on the *C-V* characteristics are qualitatively investigated. A single energy distribution has the most impact on Miller capacitance. For ITs level that is below the Fermi level, ITs have a very small impact on *C-V* curve, but the exponential and Gaussian distribution of trap now start playing a role in determining the *C-V* characteristics at $V_{GS} = -0.5$ V.

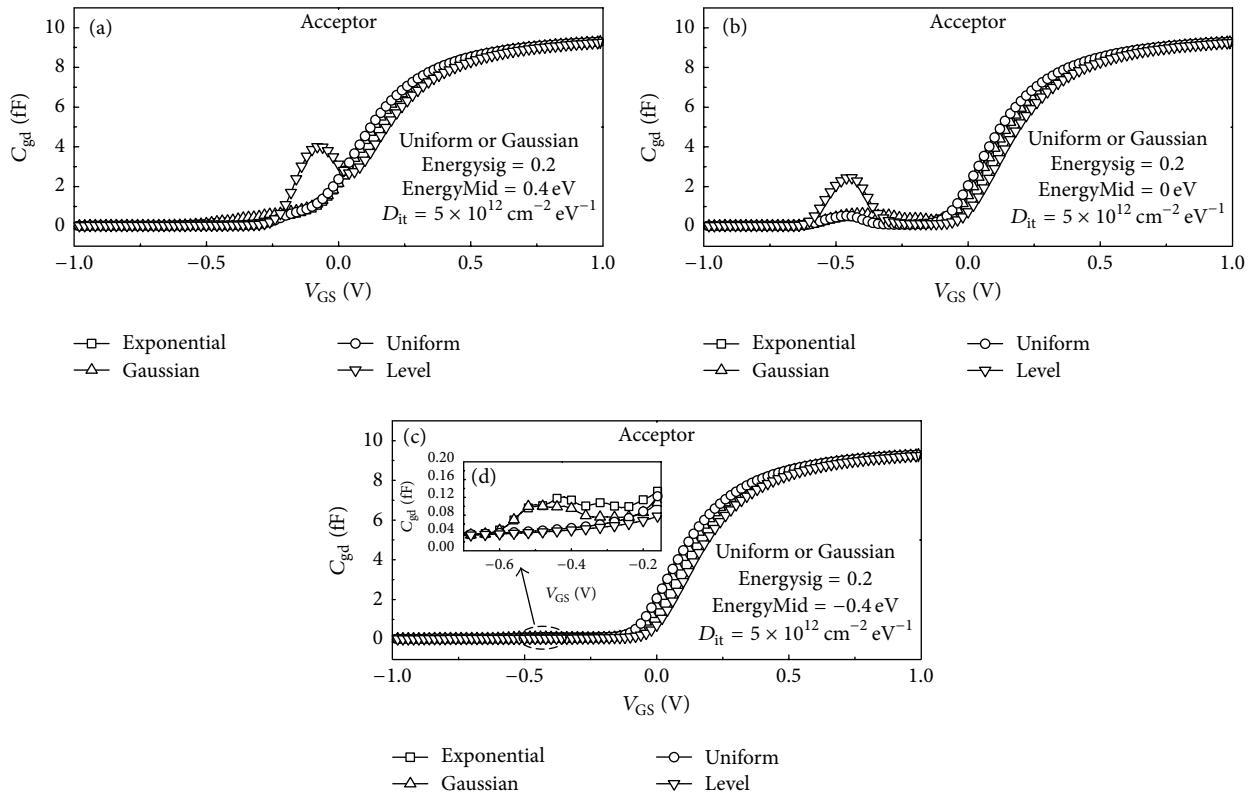

Figure 17: Four types of energetic distribution for acceptor-type are located at three representative level positions which are (a) EnergyMid = 0.4 eV (E_i + 0.4 eV), (b) EnergyMid = 0.0 eV, and (c) EnergyMid = 0.4 eV, respectively.

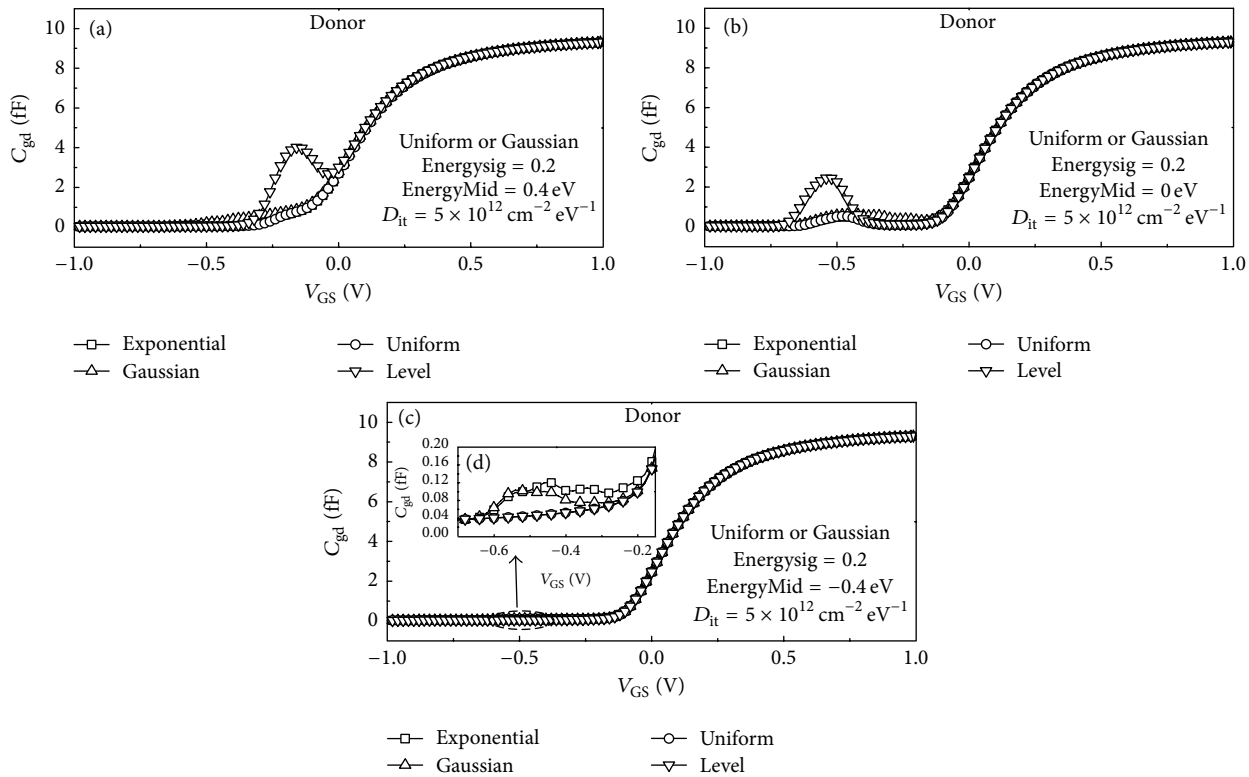

Figure 18: Four types of energetic distribution for donor-type are located at three representative level positions which are (a) EnergyMid = 0.4 eV (E_i + 0.4 eV), (b) EnergyMid = 0.0 eV, and (c) EnergyMid = 0.4 eV, respectively.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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