Impact of Lateral Asymmetric Channel Doping on Deep Submicrometer Mixed-Signal Device and Circuit Performance

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***Abstract*—In this paper, we have systematically investigated the effect of scaling on analog performance parameters in lateral asymmetric channel (LAC) MOSFETs and compared their performance with conventional (CON) MOSFETs for mixed-signal applications. Our results show that, in LAC MOSFETs, there is significant improvement in the intrinsic device performance for analog applications (such as device gain, $g_{\rm m}/I_{\rm D}$ etc.) down to the 70–nm technology node, in addition to an improvement in drive current and other parameters over a wide range of channel lengths. A systematic comparison on the performance of amplifiers and CMOS inverters with CON and LAC MOSFETs is also performed. The tradeoff between power dissipation and device performance is explored with detailed circuit simulations for both CON and LAC MOSFETs.**

***Index Terms*—Analog, CMOS optimization, lateral asymmetric channel (LAC), mixed signal CMOS, radio frequency (RF) CMOS, system on chip (SoC).**

I. Introduction

FOR THE LAST two to three decades, the entire semiconductor industry market is dominated by semiconductor memories, microprocessors, and other digital circuits. CMOS has become the technology of choice for all integrated circuit applications. However, modern integrated circuits (ICs) such as those used in wireless communication products require integration of analog as well as digital circuits in the same IC, in order to decrease the cost and improve the performance. Also, with the advancement in CMOS technology, the MOSFETs made in silicon have achieved cutoff frequencies suitable for radio frequency (RF) applications [1]. This has made CMOS attractive for system on chip (SoC) applications, where RF analog communication circuits are integrated with the digital logic and memory circuits. Quite a few researchers have looked at the performance of scaled MOSFETs for mixed-signal applications, including an evaluation of novel technologies for SoC applications [2]–[10].

However, in the sub-100-nm regime, short-channel effects (SCEs) are of primary concern, which degrade the performance significantly, making scaled device design quite challenging. A scaled device design for SoC applications is of particular significance, since device performance requirements for low power digital and analog applications are often conflicting. The CMOS technology optimized for the best digital performance may not give good analog performance for mixed-signal applications [5]. Hence, with the logic device technology poised for the 90 nm technology generation, it has become essential to look for alternative solutions to meet the analog performance requirements for mixed mode applications. One such solution is using channel engineering to boost the analog performance of a MOS transistor. A few researchers have reported lateral asymmetric Channel (LAC) or single halo (SH) MOSFETs for analog applications [11]–[15]. Though some preliminary studies have been done earlier on SH MOSFETs (or LAC), this work, for the first time, systematically looks at the impact of these MOSFETs on analog/digital circuit performance for mixed mode applications.

In this paper the performance improvement of LAC MOSFETs over conventional (CON) MOSFETs is systematically investigated with extensive process, device and circuit simulations. These two technologies have been chosen for comparison because of their near identical process flow. The results are reported in Sections II and III. Section IV deals with performance improvement of circuits such as basic amplifiers, cascode amplifiers and CMOS inverters with LAC MOSFETs. Section V summarizes the work.

II. Device Intrinsic Performance

In this section the effect of Lateral Asymmetric Channel doping on MOS transistor device performance is discussed. The process flow for LAC MOSFETs is identical to that of conventional MOSFETs except for the threshold adjust implant, which is done through a tilted angle implantation, after the gate electrode formation [11]. Pocket implant parameters such as dose, energy, and tilt angle are optimized to maximize the device performance parameters $I_{\rm on}/I_{\rm off}, g_m, g_{\rm m}/I_{\rm D}$, output resistance $(R_{\rm o})$, and *gain*. These optimized devices are used for circuit simulations in the Section IV. In this section, the relative performance of LAC MOSFETs over conventional (CON) MOSFETs is systematically explored. All the two–dimensional (2-D) simulations have been carried out using ISE TCAD. DIOS process simulator was used for simulating the device structure and DESSIS tool was used for device simulations [16].

Manuscript received June 25, 2003; revised September 19, 2003. The review of this paper was arranged by Editor J. N. Burghartz.

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Digital Object Identifier 10.1109/TED.2003.820120

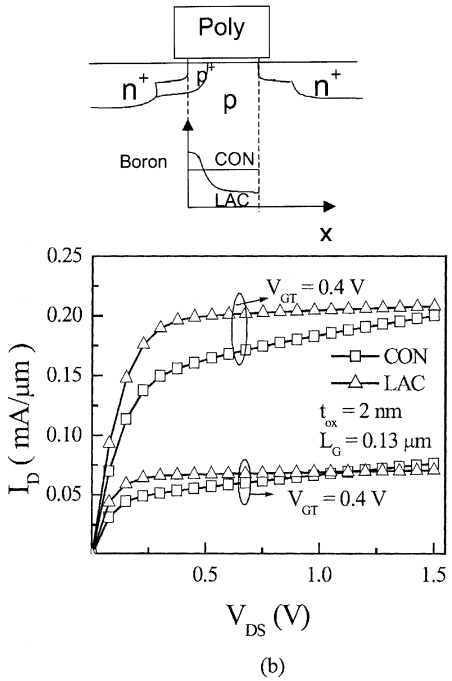

Fig. 1. (a) Cross-sectional diagram of LAC nMOSFET with boron doping variation along the channel, (b) Output characteristics of CON and LAC devices at $V_{\rm GT}$ =0.2 V and $V_{\rm GT}$ =0.4 V.

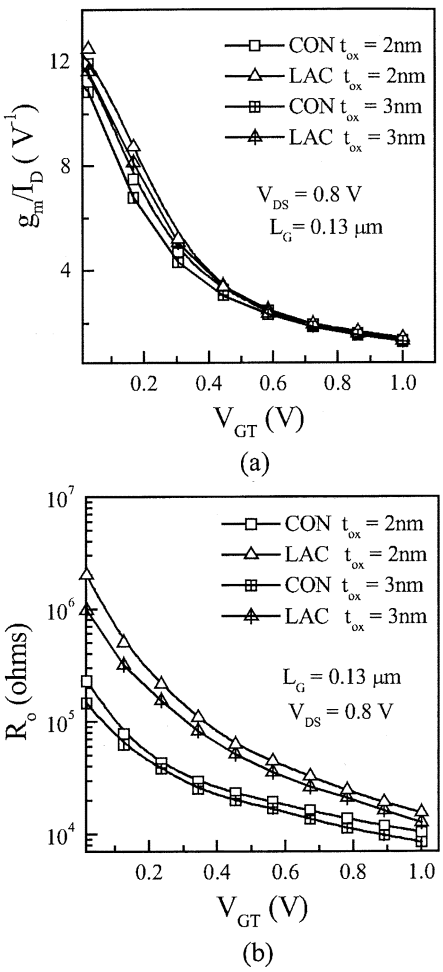

Fig. 2. (a) Transconductance generation factor $(g_{\rm m}/I_{\rm D})$ as a function of $V_{\rm GT}$, and (b) Device output resistance $(R_{\rm O})$ as function of $V_{\rm GT}$ for CON and LAC transistors with $W = 1$ μm, at a drain bias of 0.8 V.

Energy balance model has been used for device simulations to take the nonlocal effects into account. In order to take surface quantization effects into account, Van-Dort's model is used for device simulations. For the LAC MOSFETs used for simulations, the pocket has been realized (Boron for n-MOSFETs and Arsenic for p-MOSFETs) at a tilt angle implantation of 7°. The standard threshold adjust implant has been done with BF_2 at an energy of 12.5 KeV for CON devices. For both CON and LAC devices, the implantation dose is adjusted to achieve identical $V_{\rm T}$s of 0.25 V. Unless otherwise specified, for all the comparison studies involving CON and LAC MOSFETs, the $V_{\rm T}$ has been adjusted to be identical for the two technologies. We have simulated both n- and p-channel MOSFETs.

Fig. 1(a) shows device cross section with the body doping profile along the channel for LAC and CON devices and Fig. 1(b) shows I_D–V_D characteristics of the devices with gate length of 0.13 μm ($L_{\rm eff}$ is around 95 nm) at two different gate overdrive voltages $(V_{\rm GT})$ of 0.2 and 0.4 V. The characteristics show that LAC MOSFETs in forward mode (heavily doped pocket at the source side) result in significant improvement in the output resistance $(R_{\rm o})$. Reduced Drain-Induced-Barrier-Lowering (DIBL) and Channel Length Modulation (CLM) in these devices contribute to this improvement. As can be seen, at the 0.13 μm gate length regime, improvement in the drive current is marginal. Fig. 2 shows the effect of gate overdrive voltage on the performance parameters $g_{\rm m}/I_{\rm D}$ and $R_{\rm o}$ at a drain bias of 0.8 V for devices with $L_{\rm G} = 0.13$ μm and gate oxide thicknesses of 2 nm and 3 nm with the other technology parameters chosen as per the SIA Roadmap. It can be observed that, LAC devices in the forward mode of operation consistently outperform the conventional devices at all different gate overdrive voltages. Good control of short-channel effects in LAC MOSFETs results in increased $g_{\rm m}/I_{\rm D}$ and $R_{\rm o}$ values. Fig. 3(a) shows the tradeoff between device intrinsic gain and $f_{\rm T}$, and Fig. 3(b) shows device power dissipation as a function of $f_{\rm T}$ for devices studied with two different gate oxide thicknesses. One can observe that, LAC devices consistently exhibit higher voltage gains and lower power dissipation (as given by I_D) over CON devices at any given value of $f_{\rm T}$ and gate overdrive voltages. This can be attributed to the suppression of short-channel effects and an improved transconductance, in addition to a slightly lower parasitic capacitances in LAC MOSFETs. As our simulations results for y-parameters in LAC and CON MOSFETs show, we observed about 10% lower total parasitic capacitance in LAC MOSFETs as compared to CON devices. The improvement in transconductance due to an improved average carrier velocity in the channel has been reported for LAC MOSFETs [17]. Notice the turn around behavior in the characteristics at higher $f_{\rm T}$ is due to mobility degradation. Fig. 4 shows device threshold voltage and $g_{\rm mb}/g_m$ as a function of substrate bias $(V_{\rm SB})$ for both LAC and CON devices with $L_{\rm G} = 0.13$ μm, where $g_{\rm mb}$ is defined as $\partial I_D/\partial V_{\rm SB}$. LAC devices show a higher body bias

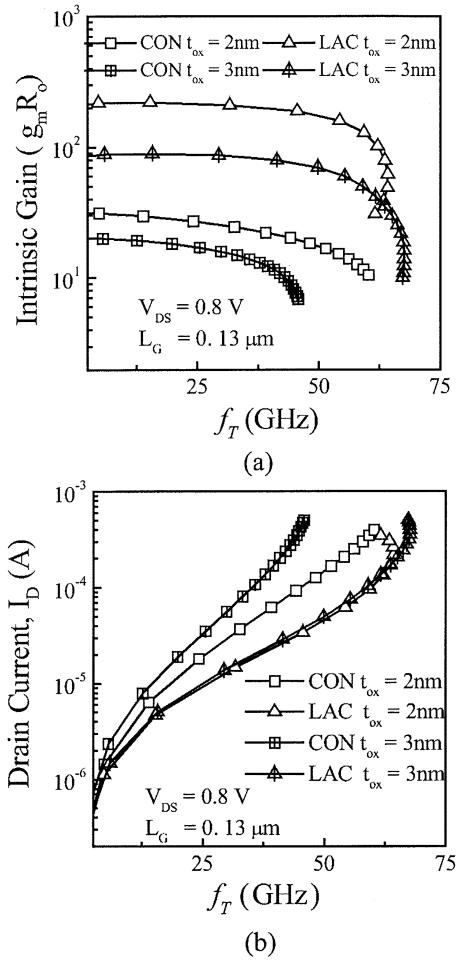

Fig. 3. (a) DC intrinsic gain for CON and LAC MOSFETs as a function of f_{T}, and (b) Drain current requirement for achieving a given f_{T}. The width of the transistors (W) is 1 μm.

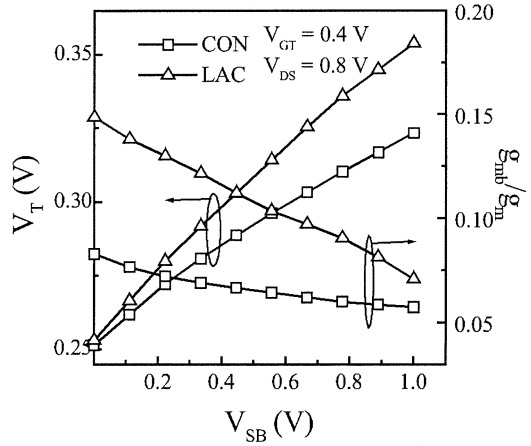

Fig. 4. Threshold voltage (V_{T}) and body bias sensitivity factor (g_{mb}/g_m) as a function of V_{SB} at a drain bias of 0.8 V and a gate over drive voltage of 0.4 V, for both CON and LAC MOSFETs. The width of the transistors (W) is 1 μm.

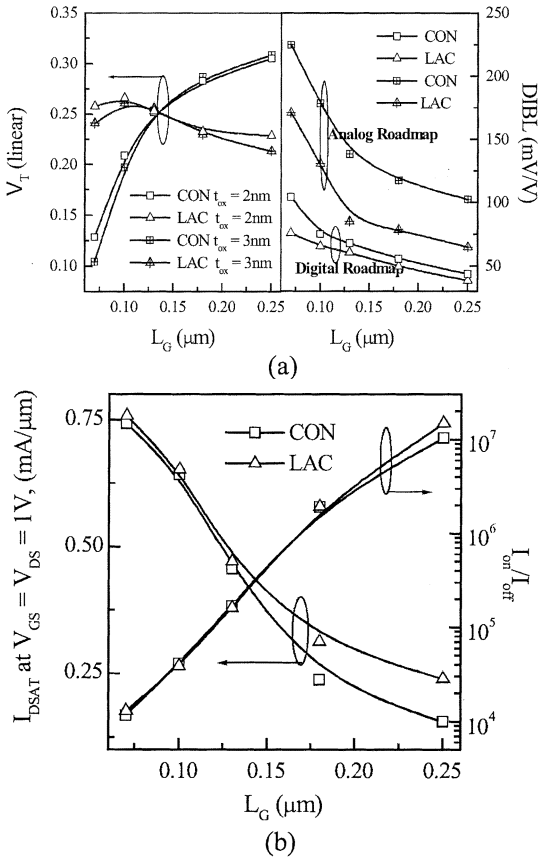

Fig. 5. (a) V_{T} roll-off and DIBL as a function of gate length. For DIBL estimation, the technology parameters as given in Table I are used for each channel length. (b) I_{DSAT} and $I_{\mathrm{on}}/I_{\mathrm{off}}$ as a function of gate length for both CON and LAC MOSFETs. V_{T} is calculated at $V_{\mathrm{DS}} = 50$ mV. The oxide thickness and V_{T} are scaled for according to SIA Logic roadmap as given in Table I.

sensitivity compared to CON devices because of higher peak doping near the source region. The effect of higher body bias sensitivity will be further elaborated in Section IV using circuit simulations.

III. Impact of Scaling on the Device Performance

Fig. 5(a) shows V_{T} roll-off for the devices with oxide thickness of 2 nm and 3 nm, with V_{T} adjusted to be identical for both CON and LAC devices at $L_{\mathrm{G}} = 0.13$ μm. DIBL is also plotted in this same figure as a function of channel length, for the devices scaled as per the analog and logic roadmaps, shown in Table I. LAC MOSFETs show roll-up characteristics initially, and then show V_{T} roll-off as expected. The roll-up in LAC devices has been attributed to the initial increase in the average channel dopant concentration with decreasing channel length. Conventional devices show degraded short channel performance compared to LAC devices. Also, DIBL in LAC devices is considerably lower compared to CON devices. This is due to the pocket doping which is known to suppress the short-channel effects in LAC MOSFETs. Fig. 5(b) shows I_{DSAT} and $I_{\mathrm{on}}/I_{\mathrm{off}}$ as a function of channel length for the devices scaled as per the logic roadmap shown in Table I. The I_{DSAT} is taken at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1$ V. It can be seen that, though there is not much improvement in the I_{DSAT} in the sub-100 nm regime, there is significant improvement for channel lengths above $L_{\mathrm{G}} = 0.13$ μm.

TABLE I
TECHNOLOGY PARAMETERS AND VOLTAGE SCALING USED FOR CIRCUIT AND DEVICE SIMULATIONS, ANALOG: SCALED ACCORDING TO THE SIA ANALOG ROADMAP, DIGITAL: SCALED AS PER THE SIA ROADMAP FOR LOGIC TECHNOLOGIES

L_G (um)	0.25	0.18	0.13	0.1	0.07
V_{DD} (V)	2.5	1.8	1.5	1.2	0.8
T_{ox} (nm) Analog	5	4	3.5	3	3
V_T (V) Analog	0.45	0.4	0.35	0.3	0.3
V_{DS} (V)	1.25	0.9	0.75	0.6	0.4
T_{ox} (nm) Digital	3	2.5	2	1.5	1.2
V_T (V) Digital	0.35	0.3	0.25	0.2	0.2
X_J (nm)	65	50	40	30	25

Larger signal swings required in the analog circuits necessitate the use of higher supply voltages and thicker gate oxides [10], [20] as shown in Table I. We have looked at the CON and LAC device performance with analog scaling parameters (Table I) and the results are presented in this section. The effect of scaling on the device parameters $g_m/I_D, R_o$, voltage gain and f_T of the devices is shown in Fig. 6, at a bias voltage of $V_{GT} = 0.4$ V and $V_{DS} = 0.8$ V. V_T and gate oxide thicknesses have been adjusted to be identical at each technology node for CON and LAC devices and have been chosen as per the analog technology roadmap given in Table I. These same parameters are also used in Section IV for circuit simulations except for inverter circuits. LAC MOSFETs have shown improved performance for all these analog parameters for gate lengths down to the sub-100 nm regime. This can be attributed to reduced DIBL and CLM as a result of optimized pocket doping in LAC MOSFETs. Though there is not much improvement in f_T for LAC MOSFETs in the sub-100 nm regime, there is a significant improvement of nearly 25% and 36% for LAC devices optimized at 0.18 μm and 0.25 μm nodes respectively. However, there is nearly a factor of two improvement in the output resistance, which leads to an increase in the intrinsic gain of LAC MOSFETs even in the sub-100 nm regime. Also, one can observe from Fig. 6(a) that the resulting output resistance with CON MOSFETs at 0.25 μm gate length is realizable with LAC MOSFETs, using a scaled 0.13 μm technology. This results in a significant improvement in the intrinsic gain of the scaled devices.

Gain times gain-bandwidth product (G^2BW), which is a figure of merit for a given technology, is nearly independent of device bias and dimensions, in strong inversion [18]. Fig. 7 shows this parameter as a function of bias current, and its dependence on the device gate length. Higher values of this parameter are observed with LAC MOSFETs compared to conventional devices, at all biasing currents and channel lengths. Note that, though the digital and analog performance parameters of both the devices are quantified with two different scaling scenarios according to Table I, we have observed similar improvement in analog performance of LAC MOSFETs even with aggressively scaled gate oxides.

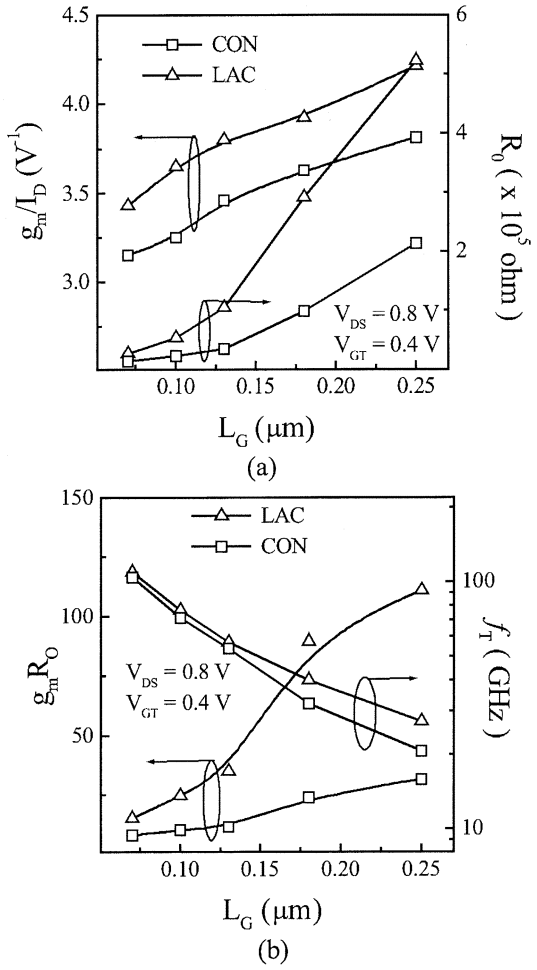

Fig. 6. (a) Transconductance generation factor (g_m/I_D) and output resistance (R_O) as a function of channel length (L_G) and (b) Intrinsic gain and cutoff frequency, f_T as a function of gate length for both CON and LAC transistors with $W = 1\,\mu$m at a drain bias of 0.8 V and gate over drive voltage of 0.4 V. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

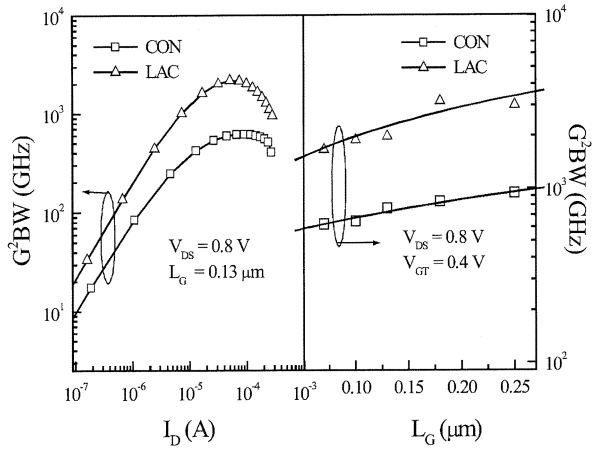

Fig. 7. Gain times gain-bandwidth product (G^2BW) of CON and LAC devices as a function of I_D and gate length (L_G) at $V_{DS} = 0.8$ V and $V_{GT} = 0.4$ V. The width of the transistor used is $W = 1\,\mu$m. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

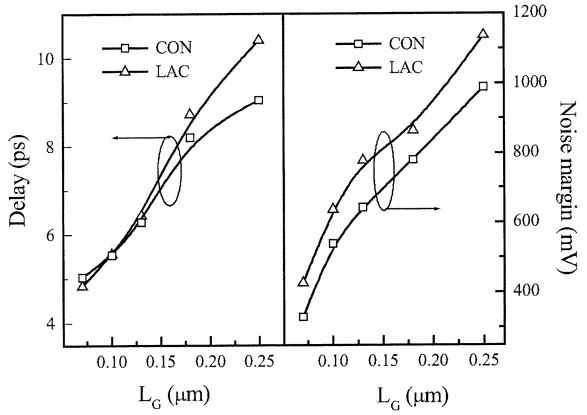

Fig. 8. CMOS inverter delay and noise margin as a function of gate length. The technology parameters are chosen according to SIA digital roadmap as given in Table I. Driver: inverter with $W_{\rm n} = 5\ \mu$m and $W_{\rm p} = 10\ \mu$m, Load: inverter with $W_{\rm n} = 1\ \mu$m $W_{\rm p} = 2\ \mu$m.

IV. Circuit Performance With LAC MOSFETs

To investigate the advantages of LAC MOSFETs at the circuit level, we have simulated a few basic analog circuits such as single stage amplifiers, cascode amplifiers and source followers. We have also simulated LAC CMOS inverter circuits and compared the circuit performance trends with CON technologies. ISE TCAD Mixed mode simulator was used for simulations. For circuit simulations, the doping information, mesh, material properties, electrode contact and model information for the NMOS and PMOS transistors were extracted from the process simulation module, DIOS and MDRAW of ISE TCAD.

A. CMOS Inverters

Fig. 8 shows CMOS inverter delay and noise margins as a function of channel length scaled according to logic roadmap in Table I, and with a load of one inverter. The inverters were realized with both CON and LAC MOSFETs using widths $W_{\rm n} = W_{\rm p}/2 = 5\ \mu$m. It can be seen that as the technology is scaled down, until about 0.13 μm, LAC devices exhibit superior performance in terms of delay and noise margins. This can be attributed to increased current drive due to an increase in the average carrier velocity in the channel and output resistance of the devices. The excess DIBL in CON MOSFETs reduces the delay in sub-100 nm regime, at the cost of increased standby power. One can observe that, even in the sub-100 nm regime, there is an improvement in noise margins for LAC MOSFETs.

B. Amplifiers With Capacitive Load

A simple capacitively loaded amplifier (Fig. 9(a), $C_{\rm L} = 1$ pF) is simulated as it provides an insight into the consequences of nonideal scaling of transconductance and the degradation of output resistance at shorter gate lengths. In each case, the bias current of the amplifier is kept at 0.1 mA. Fig. 10 shows the voltage gain and the gain-bandwidth product for an amplifier as a function of MOSFETs W/L. The transistors have a

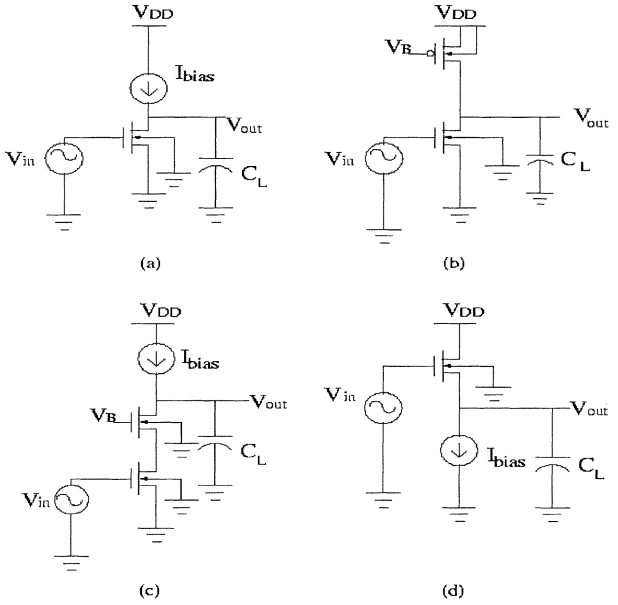

Fig. 9. (a) Common source amplifier with ideal current bias, (b) Common source amplifier with PMOS load, (c) Cascode amplifier, and (d) Source follower with a load capacitance $C_{\rm L}$ of 1 pF.

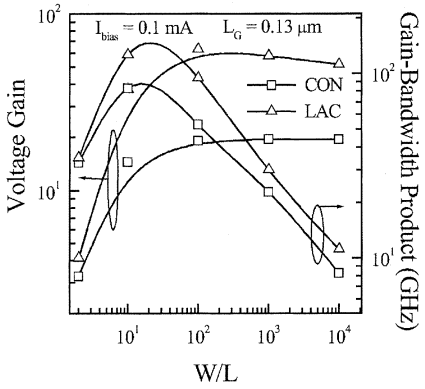

Fig. 10. Voltage gain and gain-bandwidth product of a common source amplifier with a capacitive load of 1 pF as a function of the transistor W/L, at $I_{\rm bias} = 0.1$ mA.

channel length of 0.13 μm. Fig. 11 shows voltage gain ($A_{\rm V}$) and gain-bandwidth product as a function of channel length for two values of W/L, 10 and 100, at a bias current of 0.1 mA. It can be observed that there is significant improvement in $A_{\rm V}$, even down to the 70 nm technology node. The power supply and the transistor bias voltages were adjusted as given in Table I. A factor of three improvement is observed in the voltage gain for LAC MOSFETs.

Fig. 12 shows the transistor W required to achieve an identical voltage gain of 10 with both CON and LAC MOSFETs, at a bias current of 0.1 mA. The required W is plotted as a function of technology generation. As expected, in scaled MOSFETs, because of excess short-channel effects (SCE) and mobility degradation, larger transistor sizes are required to achieve the same gain. The trend is similar for LAC MOSFETs. However, due to

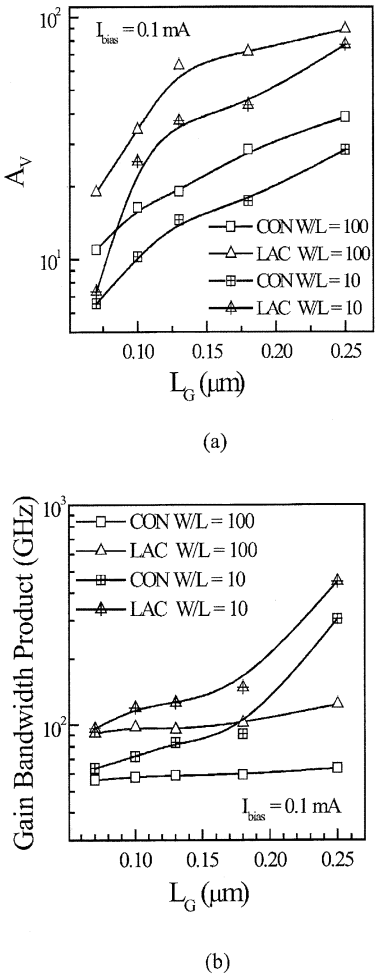

Fig. 11. (a) Voltage gain $(A_{\rm v})$ versus gate length, and (b) Gain-bandwidth product versus gate length at a constant $I_{\rm bias}$ of 0.1 mA and $V_{\rm DS} = V_{\rm DD}/2$. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

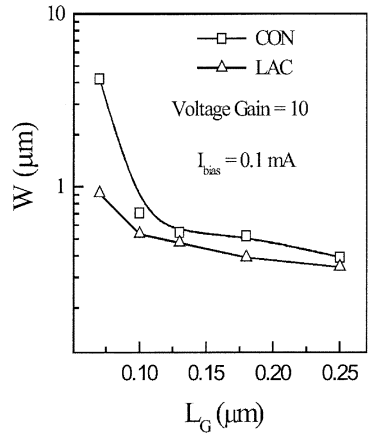

Fig. 12. Width of the transistor required to achieve a voltage gain of 10 as a function of channel length at a constant $I_{\rm bias}$ of 0.1 mA. A signal frequency of 1 KHz and capacitive load of 1 pF are used for simulations. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

suppression of SCEs, relatively smaller transistors are required with LAC MOSFETs to achieve the required gain, which also leads to reduced parasitic capacitances.

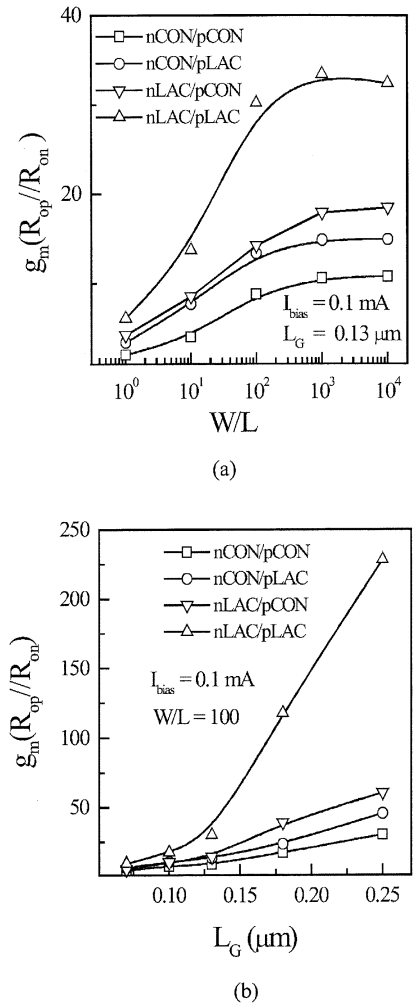

Fig. 13. (a) Voltage gain $(A_{\rm v})$ of amplifier versus $\rm W/L$ of driver transistor for a constant current bias of 0.1 mA, and (b) Voltage gain of the same amplifier as a function of channel length at a frequency of 1 KHz. $R_{\rm on}$ and $R_{\rm op}$ are the respective output resistances of PMOS and NMOS transistors at this biasing point respectively. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

C. Amplifiers With PMOS Active Loads

In practice, all the IC amplifiers utilize active loads for higher load resistances in order to achieve larger signal swings, reduced power dissipation and lower area. In this section we look at the performance of NMOS amplifiers with PMOS active loads [Fig. 9(b)]. This combination also provides an insight into the performance of LAC differential amplifiers, when two such stages are connected differentially. As these differential stages are the primary stages of operational amplifiers, one needs to understand the effect of LAC transistors on such circuits. As part of this study we have simulated four kinds of amplifiers, namely, amplifiers with CON driver-CON Load, CON driver-LAC load, LAC driver-CON load, and LAC driver-LAC load, to investigate the advantage of LAC technologies in terms of parasitics.

Fig. 13(a) shows the voltage gain of the circuit as a function of $\rm W/L$ for all the four amplifier combinations. It can be seen that amplifiers with LAC driver-LAC load give the best

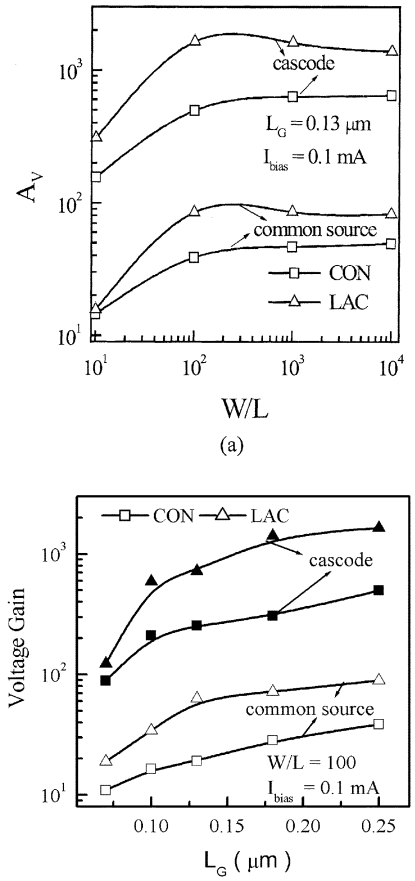

Fig. 14. (a) Voltage gain (A_v) versus W/L of driver transistor, and (b) Voltage gain as a function of gate length, for both common source and cascode amplifiers at a constant bias current of 0.1 mA and at a frequency of 1 KHz. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

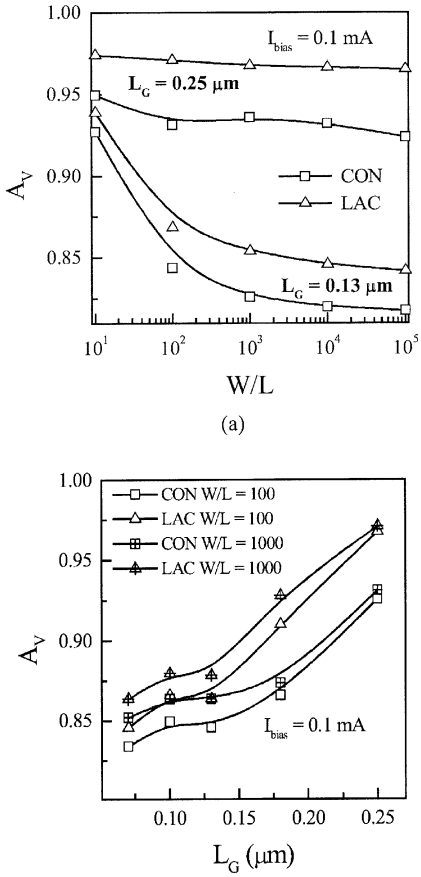

Fig. 15. (a) Voltage gain (A_v) versus W/L, and (b) Voltage gain versus channel length of a source follower with a constant bias current of 0.1 mA and a capacitive load of 1 pF. The technology parameters are chosen according to SIA analog roadmap as given in Table I.

performance, whereas amplifiers with CON driver-CON load show the worst performance. However, amplifiers with LAC driver-CON load fall between the above two cases. These results further prove the advantages of LAC technology over the CON technology for analog applications. Fig. 13(b) shows the voltage gain of all the above configurations as a function of channel length for a constant W/L(=100) of driver transistors. From this figure it can be observed that for identical voltage gains, amplifiers with LAC driver-LAC load can be scaled aggressively, thus enabling high frequency applications using CMOS. The performance of PMOS amplifiers with NMOS loads, which is the traditionally preferred combination for input stage of an OPAMP, also shows a similar improvement in performance with LAC technologies.

D. Cascode Amplifiers

Cascode amplifiers (Fig. 9(c)) are used as wide band amplifiers in applications where larger voltage gains are required without sacrificing bandwidth. These are necessary in VLSI circuits, as the device output resistance is severely degraded in the sub-micron regime. Also, cascode circuits improve the noise level of the circuit and result in lower channel length modulation [19]. However, inherent body bias present because of the stacked structure limits the gain of cascode amplifiers. As shown in Section II, LAC MOSFETs exhibit higher body bias sensitivity compared to CON devices. This necessitates a thorough study on the performance of cascode amplifiers with LAC technologies. In this section we show results on cascode amplifiers realized with LAC MOSFETs. Fig. 14(a) shows the voltage gain of cascode and common source amplifiers as a function of W/L, at a bias current of 0.1 mA and Fig. 14(b) shows the voltage gain of a cascode amplifier with transistor W/L of 100, as a function of channel length, at the same bias current. It can be seen that improvement in voltage gain of cascode amplifiers with LAC MOSFETs is not so significant, due to the increased body bias effect in the sub-100 nm regime.

E. Source Followers

We have also simulated source followers (Fig. 9(d)) using LAC MOSFETs to study the effect of body bias on the voltage gain. Fig. 15(a) shows A_V as a function of W/L of driving transistor, for a capacitive load of 1 pF. It is observed that, as the channel length is reduced, large deviation in voltage gain occurs from its ideal value of unity for CON MOSFETs. However, this deviation becomes less in the case of LAC MOSFETs due to the increased output resistance

of the device. Fig. 15(b) shows the effect of scaling on the performance of source followers. As can be seen, LAC MOSFETs consistently outperform CON MOSFETs down to the 70 nm technology regime but the improvement in voltage gain is to some extent offset by the higher body bias sensitivity in LAC devices, as discussed in Section II.

V. Conclusion

In this paper, we have systematically compared the conventional and LAC MOS technologies and looked at their performance advantages for mixed-signal applications. As our results show, nearly a factor of three improvement in intrinsic voltage gain and an improvement of nearly 36% in f_T of the MOSFET are realizable at a channel length of 0.25 μm using the LAC technology. In this work, we have quantified the tradeoffs between device performance, area, and power dissipation. We show that, a factor of three improvement in device intrinsic gain is realizable with 0.13 μm LAC technology at an f_T of 40 GHz with a marginal improvement in power dissipation. Almost a factor of two minimum improvement in gain-bandwidth product is observed at all the technology nodes studied in this work for the optimized LAC MOSFETs. The improved circuit performance with LAC technologies has been attributed to the higher drive currents, higher output resistance, and also due to lower parasitic capacitances as shown by circuit simulations using a combination of LAC and CON amplifiers.

Acknowledgment

One of the authors, Mr. K. Narasimhulu is supported through a fellowship by Intel Corporation at IIT Bombay.

References

[1] M. Saito, M. Ono, R. Fuzimoto, and T. Yostitomi, "0.15 μm RF CMOS technology compatible with logic CMOS for low-voltage operation," *IEEE Trans. Electron Devices*, vol. 45, pp. 737–741, Mar. 1998.

[2] J. J. P. Bruines, "Process outlook for analog and RF applications," *Microelectron. Eng.*, vol. 54, pp. 35–48, Dec. 2000.

[3] C. Fiegna, "The effect of scaling on the performance of small signal MOS amplifiers," in *Proc. ISCAS 2000*, May 2000, pp. 733–736.

[4] D. Buss, "Device issues in the integration of analog/RF functions in deep sub-micron digital CMOS," in *IEDM Tech. Dig.*, Dec. 1999, pp. 423–426.

[5] K. Imai, K. Yamaguchi, T. Kudo, N. Kimizuka, and H. Onishi, "CMOS device optimization for system-on-a-chip applications," in *IEDM. Tech. Dig.*, 2000, pp. 455–458.

[6] A. J. Annema, "Analog circuit performance and process-scaling," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 717–725, 1999.

[7] W. Sansen, "Analog circuit design in scaled CMOS technology," in *VLSI Symp. Tech. Dig.* , 1996, pp. 8–11.

[8] K. Bult, "Analog design in deep-sub-micron CMOS," in *Proc. ESSCIRC*, 2000, pp. 1–17.

[9] M. J. M. Pelgrom and M. Vertregt, "CMOS technology for mixed signal ICs," *Solid-State Electron.*, vol. 41, no. 7, pp. 967–974, 1997.

[10] K. Bult, "Analog broadband communication circuits in pure digital deep sub-micron CMOS," in *IEEE ISSCC Tech. Dig.*, 1999, pp. 76–77.

[11] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1-μm MOSFET with asymmetric channel profile," *IEEE Trans. Electron Devices*, vol. 44, pp. 595–600, Apr. 1997.

[12] B. Cheng, A. Inani, V. R. Rao, and J. C. S. Woo, "Channel engineering for high-speed sub-1.0 V power supply deep sub-micron CMOS," in *VLSI Symp. Tech. Dig.*, 1999, pp. 69–70.

[13] H. V. Deshpande, B. Cheng, and J. C. S. Woo, "Analog device design for low-power mixed mode applications in sub-micron technology," *IEEE Electron Dev. Lett.*, vol. 22, Dec. 2001.

[14] D. G. Borse, K. N. M. Rani, N. K. Jha, A. N. Chandorkar, J. Vasi, V. R. Rao, B. Cheng, and J. C. S. Woo, "Optimization and realization of sub-10-nm channel length single halo p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, pp. 1077–1078, June 2002.

[15] N. K. Jha, M. S. Baghini, and V. R. Rao, "Performance and reliability of single halo deep sub-micron p-MOSFETs for analog applications," *Proc. IPFA* , pp. 35–39, July 2002.

[16] *ISE-TCAD Manuals*, 2000. Release 6.0.

[17] B. Cheng, V. R. Rao, and J. C. S. Woo, "Exploration of velocity overshoot in a high-performance deep sub 100 nm SOI MOSFET with asymmetric channel profile," *IEEE Electron Device Lett.*, vol. 20, pp. 538–540, Oct. 1999.

[18] M. Ismail and T. Fiez, *Analog VLSI Signal and Information Processing*. New York: McGraw-Hill, 1994.

[19] R. Geiger, P. E. Allen, and N. R. Strader, *Analog and Digital VLSI Design Techniques*: McGraw-Hill, 1994.

[20] *International Technology Roadmap for Semiconductors*, 2001.

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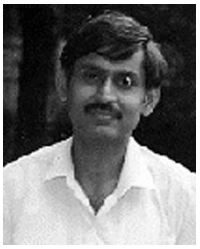

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