

Impact of Layer Configuration and Doping on Electron Transport and Bias Stability in Heterojunction and Superlattice Metal Oxide Transistors*Dongyoon Khim*, Yen-Hung Lin, Thomas D. Anthopoulos**

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E-mail: thomas.anthopoulos@kaust.edu.sa**Keywords:** Metal oxide semiconductors; thin-film transistors; doping; heterojunction transistor; solution processing**Abstract**

The astonishing recent progress in the field of metal oxide thin-film transistors (TFTs) and their debut in commercial displays was accomplished using vacuum-processed multi-component oxide semiconductors. However, emulating this success with their solution-processable counterparts poses numerous scientific challenges. Here, we report the development of high mobility n-channel TFTs based on ultra-thin (<10 nm) alternating layers of In₂O₃ and ZnO that are sequentially deposited to form heterojunction and superlattice channels. The resulting TFTs exhibit high electron saturation mobility (13 cm²V⁻¹s⁻¹), excellent current on/off ratios (>10⁸) with nearly zero onset voltages and hysteresis-free operation despite the low temperature processing (≤200 °C). The enhanced performance is attributed to the formation of a quasi-two-dimensional electron gas-like system at the In₂O₃/ZnO heterointerface due to the conduction band offset. We show that altering the oxide deposition sequence has an adverse effect on electron transport due to formation of trap states. Optimised multilayer TFTs are shown to exhibit improved bias-stress stability compared to single layer TFTs. Modulating the electron concentration within the superlattice channel via selective n-doping of the ZnO interlayers, leads to almost 100% saturation mobility increase (≈25 cm²V⁻¹s⁻¹) even when the TFTs are fabricated on flexible plastic substrates.

Metal-oxide semiconductors represent an important technology for application in thin-film transistors (TFTs) for next generation, large-area electronics.^{[1] [2] [3] [4] [5] [6]} Multicomponent metal oxides such as the indium-zinc oxide (IZO) and indium-gallium-zinc oxide (IGZO) have been attracting particular attention because of the combination of high electron mobility, optical transparency and processing versatility.^{[1] [2] [3] [7] [8]} Unfortunately, solution processing of such complex metal oxides often relies on high temperature annealing (>300 °C) in order to promote metal-oxygen-metal (M-O-M) heterometal condensation upon decomposition of the precursors and form uniform and dense semiconducting layers required for TFT applications.^{[9] [10]} Inevitably, most of the multicomponent oxides are incompatible with inexpensive temperature sensitive substrate materials, such as plastic, that are increasingly required for application in emerging flexible, lightweight electronics.^[11] Furthermore, the difficulty in controlling their stoichiometry often results to layer with excessive electrical conductivity that adversely affects key TFT characteristics such as on-off ratio and threshold voltage (V_{TH}). In an effort to reduce the process temperature different approaches have been proposed including, combustion synthesis,^[5] solution combustion synthesis,^[12] aqueous-based solution process,^[13] sol-gel on-chip process,^[1] and photo-chemical conversion methods.^[2]

With a similar objective in mind, we have recently introduced the multilayer metal oxide TFT concept that can be implemented via a combination of solution processing and low thermal annealing or via rapid photonic processing of the channel layer.^{[14] [15] [16]} Irrespective of the process methodology, the resulting TFTs were shown to consist of multilayer channels featuring sharp In_2O_3/ZnO or $In_2O_3/Ga_2O_3/ZnO$ heterointerfaces. These interfaces were shown to be able to support the formation of quasi-two-dimensional electron gas (q2DEG)-like systems that led to remarkable improvement in the electron mobility when compared to devices made using the individual oxide layers.^{[14] [15]} The ability to solution-process such heterointerfaces has paved the way to a plethora of innovative channel designs that can be realised from solution using scalable and low-temperature processing paradigms^{[15] [16] [17]} for

use in the emerging field of printed large-area opto/electronics. Similar heterojunction-based oxide channels have also been demonstrated via sputtering and was shown to enhance both the electron mobility and current on-off ratio of the resulting TFTs,^[18] further highlighting the potential of the multi-layer channel approach.

Here we report on the development of metal oxide transistors based on multilayer channels composed of alternating layers of In_2O_3 and ZnO processed from solution at temperatures $<200^\circ\text{C}$ in ambient air. We show that the electrical characteristics of the resulting TFTs depend heavily on the exact layer configuration and the number of $\text{In}_2\text{O}_3/\text{ZnO}$ heterojunctions in the channel. Our results reveal that heterojunction channels based on the dielectric/ $\text{In}_2\text{O}_3/\text{ZnO}$ configuration exhibit significantly higher electron mobility than TFTs made with the dielectric/ $\text{ZnO}/\text{In}_2\text{O}_3$ heterojunction configuration due to the superior interface quality determined by the ultra-smooth surface of the bottom In_2O_3 layer. Increasing the number of sequentially deposited layers in the former channel configuration, is found to increase both the electron mobility ($13\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and current on/off ratio ($>10^8$). By going a step further and intentionally n-doping the ZnO interlayers with Li (ZnO-Li), we are able to grow modulation-doped (MOD) $\text{In}_2\text{O}_3/\text{ZnO-Li}/\text{In}_2\text{O}_3/\text{ZnO-Li}$ superlattice TFTs with electron mobility approaching $25\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Finally, by taking advantage of the low process temperature, we demonstrate superlattice TFTs on plastic substrates using printed high- k dielectrics, which in turn enable low-voltage transistor operation ($\leq 1.5\text{ V}$). This is the first demonstration of modulation-doped superlattice oxide TFTs to date and highlights the tremendous potential of the approach for the development of next generation large-area TFT technologies.

The possible impact of layer intermixing between In_2O_3 and ZnO during sequential solution processing, was first examined by studying the operating characteristics of TFTs based on intentionally mixed In_2O_3 and ZnO (IZO) precursors and those of $\text{In}_2\text{O}_3/\text{ZnO}$ heterojunction TFTs. Details regarding the device fabrication and characterization are provided in the *Experimental* section. **Figure 1a** displays a set of representative transfer characteristics for the

single blend IZO layer and heterojunction ($\text{In}_2\text{O}_3/\text{ZnO}$) transistors. The IZO device exhibits poor electron transport characteristics manifested as low saturation currents ($\approx 10^{-6}$ A) and a large onset voltage (V_{ON}) of ≈ 26 V. The poor device performance is attributed to incomplete decomposition of the precursors to In-O-Zn due to insufficient thermal energy. Only when the IZO layer is annealed at 400 °C in air, well performing TFTs can be obtained (**Figure S1**). On the contrary and in agreement with our previous work,^[15] the $\text{In}_2\text{O}_3/\text{ZnO}$ device exhibit superior n-channel characteristics with high on/off ratio and an appreciable electron mobility of 6.25 cm^2/Vs (**Table 1**). The improved performance has been previously linked to the existence of a q2DEG-like system present at the vicinity of the $\text{In}_2\text{O}_3/\text{ZnO}$ heterointerface.^[19] The existence of this confined electron system was shown to influence not only the mobility but also the nature of electron transport, changing from a trap-limited to percolation-limited conduction process for single layer and heterojunction channel-based TFTs, respectively.^[19]

Table 1. Summary of operating parameters of various transistor channel architectures investigated. The electron mobility (μ_{SAT}) was estimated in saturation at $V_{\text{D}} = 40$ V using the gradual channel approximation. The channel width/length of all transistors was kept constant and equal to $W/L = 1/0.1$ mm.

| Channel | | μ_{SAT}^* (cm^2/Vs) | V_{TH} (V) | V_{ON} (V) | on/off ratio | $I_{\text{ON}}(V_{\text{D}}=40 \text{ V})$ (A) |
|---------|---|---|------------------------|------------------------|--------------------|---|
| Type-I | In_2O_3 (I) | 1.6 (± 0.3) | 13.5 (± 3.1) | 6.8 | 1.27×10^6 | 1.8×10^{-4} |
| | $\text{In}_2\text{O}_3/\text{ZnO}$ (IZ) | 6.25 (± 0.4) | 9.3 (± 0.8) | 0 | 3.1×10^6 | 8.9×10^{-4} |
| | IZI | 7.7 (± 1.6) | 11.8 (± 2.4) | 3.6 | 3.1×10^6 | 9.7×10^{-4} |
| | IZIZ | 11.4 (± 0.5) | 8.1 (± 0.4) | 0 | 9.6×10^7 | 1.8×10^{-3} |
| Type-II | ZnO (Z) | 1.43 (± 0.1) | 13.3 (± 1.1) | 2.9 | 2.3×10^5 | 1.6×10^{-4} |
| | ZnO/ In_2O_3 (ZI) | 0.013 (± 0.3) | 35.7 (± 1.0) | 35 | 1.2×10^2 | 3.3×10^{-8} |
| | ZIZ | 1.75 (± 0.3) | 15 (± 0.8) | 1.7 | 1.1×10^5 | 1.7×10^{-4} |
| | ZIZI | 0.008 (± 0.002) | 37.6 (± 0.5) | 38.3 | 27.4 | 1.0×10^{-8} |

*Mobility values represent averages calculated from at least 10 devices.

To investigate whether electron confinement takes place at the critical heterointerfaces, we performed capacitance-voltage (C - V) measurements using metal-insulator-semiconductor (MIS) capacitors based on the $\text{In}_2\text{O}_3/\text{ZnO}$ heterojunction as the semiconductor (**Figure 1b**). Data analysis allows estimation of the apparent charge carrier density (N_{CV}) as a function of the semiconductor depth (x), starting from the Al electrode ($x = 0$ nm) all the way to the $\text{SiO}_2/\text{In}_2\text{O}_3$ interface (inset in **Figure 1b**).^{[20] [21]} Indeed, the evolution of N_{CV} versus semiconductor layer thickness shown in **Figure 1c** reveals the existence of a significantly higher electron concentration ($\approx 5.2 \times 10^{17} \text{ cm}^{-3}$) at the critical $\text{In}_2\text{O}_3/\text{ZnO}$ heterointerface as compared to concentrations measured within the ZnO ($\approx 4.7 \times 10^{16} \text{ cm}^{-3}$) and In_2O_3 ($\approx 2.6 \times 10^{16} \text{ cm}^{-3}$) layers. No such discontinuity in N_{CV} is observed in MIS capacitors comprising of single layer In_2O_3 and ZnO , in agreement with previous reports.^[14] Our working hypothesis is that mobile electrons from the conduction band (CB) of ZnO are transferred to the corresponding band in In_2O_3 upon physical contact due to the CB off-set/discontinuity (N_{CV}).^{[19] [15]} **Figure 1d** depicts the energy band diagram of the $\text{In}_2\text{O}_3/\text{ZnO}$ heterointerface reconstructed by combining the experimentally determined energetics of the individual layers and the heterojunction. Electrons confined at the heterointerface are expected to delocalize along the channel plane on the In_2O_3 side but confined in the out of plane (z) direction. The large discontinuity in N_{CV} closely resembles that of a 2-dimensional electron gas (2DEG) in traditional III-V semiconductor heterointerfaces^{[22] [23]} and can be viewed as direct evidence of the presence of free electrons confined at the $\text{In}_2\text{O}_3/\text{ZnO}$ heterointerface in agreement with our previous reports.^{[19], [14]}

Next, we investigated the dependence of electron transport on the heterojunction layer configuration and the number of critical ($\text{In}_2\text{O}_3/\text{ZnO}$) heterointerfaces. **Figure 2a-b** show the device schematics of the two types of TFTs fabricated. Details on the transistor fabrication and characterization are provided in the *Experimental* section. Type-I series includes, In_2O_3 (I), $\text{In}_2\text{O}_3/\text{ZnO}$ (IZ), $\text{In}_2\text{O}_3/\text{ZnO}/\text{In}_2\text{O}_3$ (IZI), and $\text{In}_2\text{O}_3/\text{ZnO}/\text{In}_2\text{O}_3/\text{ZnO}$ (IZIZ) devices (**Figure 2a**),

while Type-II series encompass ZnO (Z), ZnO/In₂O₃ (ZI), ZnO/In₂O₃/ZnO (ZIZ), and ZnO/In₂O₃/ZnO/In₂O₃ (ZIZI) TFTs (**Figure 2b**). Note that Type-I TFTs rely on In₂O₃ as the first layer deposited on the SiO₂ gate dielectric, while Type-II devices on ZnO. Further details on the fabrication process used are provided in the *Experimental* section. The representative transfer characteristics and corresponding $I_D^{0.5}$ vs V_G plots for all channel configurations for Type-I and Type-II TFTs are shown in **Figure 2c** and **Figure 2d**, respectively. The electron mobility measured in saturation (μ_{SAT}) for the single layer In₂O₃ TFTs yields an average value of 1.6 cm²V⁻¹s⁻¹; an expected value for spin-coated devices annealed at 200 °C. The TFT exhibits relatively high threshold (V_{TH}) and onset voltage (V_{ON}) of 13.5 V and 6.8 V, respectively. On the other hand, formation of the In₂O₃/ZnO heterojunction via sequential deposition of a ZnO layer atop leads to remarkable improvement in the TFT performance. Specifically, μ_{SAT} is found to increase to 6.2 cm²V⁻¹s⁻¹ while the V_{TH} reduces to 9.3 V. Noteworthy is the dramatic reduction in V_{ON} to ≈0 V, which highlights the drastic impact of the top ZnO layer on the electron transport across the heterojunction channel.

Next, we deposited a layer of In₂O₃ onto the In₂O₃/ZnO (IZ) heterojunction to form the trilayer IZI system shown in **Figure 2a**. Although, the resulting TFTs exhibit higher μ_{SAT} (7.7 cm²V⁻¹s⁻¹) both V_{TH} and V_{ON} shift towards more positive V_G . We attribute this to a reduced concentration of mobile electrons upon gate-field doping, which in turn can be ascribed either to trapping of electrons at the additional top ZnO/In₂O₃ heterointerface, or to electrons transferred to the second In₂O₃ layer above the ZnO. Analysis of the different interfaces by intermittent AFM measurements provide some clues on the origin of this effect and will be discussed later.

Finally, a fourth layer of ZnO was deposited atop the IZI to form the tetralayer IZIZ superlattice channel shown in **Figure 2a**. An interesting feature of this particular superlattice is that it contains three critical In₂O₃/ZnO heterointerfaces, which are expected to enhance electron transport even further. Indeed, IZIZ transistors exhibit improved operating

characteristics that include a higher μ_{SAT} of $11.4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and reduced V_{TH} and V_{ON} of 8.3 and 0 V, respectively (**Table 1**). The dramatic impact of the channel configuration on μ_{SAT} , V_{ON} , V_{TH} , channel on-current (at $V_{\text{D}} = 40 \text{ V}$) and on-off ratio, is better illustrated in **Figure S2**. To this end, the characteristic return of V_{ON} back to 0 V highlights the ability to modulate the electron concentration within the active channel region by simply controlling the number and alternating In_2O_3 and ZnO layers. Thus, it becomes apparent that the formation of superlattice-like channels incorporating alternating In_2O_3 and ZnO layers leads to enhanced TFT performance while providing accurate control over V_{TH} and V_{ON} . This is an important discovery and underlines a new strategy towards high performance metal oxide TFT that until now has remained unexplored.

To study the influence of the layer configuration on the electron transport in the channel, we fabricated a series of Type-II devices (**Figure 2b**), where the bottom In_2O_3 layer has now been replaced by ZnO. **Figure 2d** displays a representative set of the transfer characteristics of the various TFTs. The devices exhibit stark differences in their operating characteristics when compared with Type-I TFTs shown in **Figure 2c**. In particular, single layer ZnO TFTs yield $\mu_{\text{SAT}} = 1.43 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with $V_{\text{TH}} = 13.3 \text{ V}$, both of which are comparable with values measured for single layer In_2O_3 TFTs (**Table 1**). Unlike the IZ heterojunction TFT (Type-I), however, deposition of an In_2O_3 layer atop the first bottom ZnO channel to form the Type-II ZI heterojunction channel, results to a dramatic reduction (100 \times) of the electron mobility to $0.013 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, accompanied by a significant increase in V_{TH} (35.7 V) and V_{ON} (35 V) (**Table 1**). Spin-coating of an additional ZnO layer atop the ZI heterojunction results to the formation of a ZIZ channel with a surprisingly positive effect on μ_{SAT} ($1.75 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), V_{TH} (15 V) and V_{ON} (1.7 V). Addition of a fourth In_2O_3 layer atop the ZIZ trilayer yields the Type-II ZIZI superlattice TFTs shown in **Figure 2b**. Unlike Type-I IZIZ-based devices, however, the ZIZI TFTs exhibit dramatically degraded characteristics with the μ_{SAT} plummeting to $0.008 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and V_{TH} and V_{ON} reaching very high values of 37.6 and 38.3 V, respectively. The

extraordinary effect of the layer configuration on μ_{SAT} , V_{ON} , V_{TH} , channel on-current (at $V_{\text{D}} = 40$ V) and on-off ration, is better illustrated in **Figure S3**. Here, all device parameters are shown to fluctuate between values extracted for the single layer ZnO TFTs (Z) and those extracted for worse-performing TFTs based on multilayer channels with even numbers of oxide layers, namely ZI and ZIZI. In contrast, the trilayer ZIZ device exhibits performance characteristics equal to that of the single layer ZnO device. These findings reveal that the bottom ZnO layer governs the overall performance of Type-II TFTs.

To understand the origin of the starkly different operating characteristics, the surface topographies of the various oxide layers were investigated via intermittent AFM measurements. In the case of multilayer devices, the surface of the layer beneath was assumed to define the roughness of the formed heterointerface since solution deposited In_2O_3 and ZnO layers do not intermix.^{[14] [19] [15]} Representative surface topography AFM images for single layer In_2O_3 (I), ZnO (Z), ZnO/ In_2O_3 (ZI), and In_2O_3 /ZnO (IZ) and their corresponding height histogram are shown in **Figure 3a-d** and **Figure 3e**, respectively. Single layers of In_2O_3 and ZnO deposited on SiO_2 exhibit ultra-smooth surfaces with 0.15 nm and 0.67 nm of RMS roughness (R_{RMS}), respectively. Notably, the surface of the bilayer In_2O_3 /ZnO shows an R_{RMS} of 0.59 nm, which is slightly lower than that of single ZnO layer (0.67 nm). The latter observation highlights the beneficial role of the In_2O_3 layer beneath which acts as a buffer. In contrast, deposition of In_2O_3 onto ZnO leads to a rough heterojunction surface as evident by its high surface $R_{\text{RMS}} = 1.55$ nm (**Figure 3e**). Based on the results presented so far it becomes apparent that deposition of ZnO on In_2O_3 leads to smooth and extremely flat IZ heterointerfaces, whilst deposition of In_2O_3 onto ZnO yields to significantly rougher ZI heterojunctions. Combining the AFM analysis from **Figure 3a-e** with the measured transistor characteristics from **Figure 2c-d**, one can classify the formed heterointerfaces into ‘good’ and ‘bad’ ones indicated respectively by the green ticks and red crosses in **Figure 3f-g**. The only difference between Type-I and Type-2 channels, is that in Type-I channels the formation of several ‘good’ heterointerfaces has a characteristic

accumulative positive effect, whilst for Type-II, the subsequent formation of ‘good’ heterointerfaces only help to offset the negative influence of the ‘bad’ heterointerface(s) beneath.

From the results and relevant analysis presented so far several important conclusions can be drawn regarding the operation principles of these multilayer TFTs:

1. The sequence with which the In_2O_3 and ZnO layers are deposited plays a crucial role on the operating characteristics and performance of the resulting TFTs.
2. Type-I devices based on In_2O_3 as the bottom layer show continuous improvement in electron mobility with increasing channel layer complexity, despite significant V_{TH} and V_{ON} fluctuations (**Figure 3a-c**). In addition, a significant increase in the channel current on/off ratio is also observed (**Figure 3d**).
3. In Type-II channel TFTs (**Figure 2b**) the maximum performance is limited to that of the single layer ZnO transistor and, unlike Type-II devices, does not improve with the subsequent deposition of additional In_2O_3 and ZnO layers. On the contrary, device performance is found to degrade exclusively when an even number of layers is used (i.e. ZI and ZIZI) and recovers back to the ZnO TFT level when an odd number of layers is employed (i.e. Z and ZIZ).

In addition to carrier mobility, transistor parameter fluctuation and bias-stability present additional challenges to technology commercialization.^[24] To address this we studied the parameters fluctuation in best-performing superlattice TFTs and compare them against those of single and bilayer channel TFTs. **Figure 4a** shows the transfer characteristics for ten IZIZ TFTs with identical channel geometry fabricated on the same substrate. The transistors exhibit similar transfer characteristics with current spread ($\Delta V < 1$ V) and high current on/off ratios (10^6 - 10^7). Importantly, IZIZ TFTs show small variation in V_{ON} (-5 to 0 V) and μ_{SAT} (11 - $13 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) with channel length (L) scaling between 30-100 μm (**Figure 4b**). This behavior is better

illustrated in **Figures 4c** and **S4**, where unlike single layer ZnO and In₂O₃ devices, IZ and IZIZ transistors exhibit an L -independent mobility behaviour, which is a prerequisite for practical applications. We note that the relatively high V_{TH} for single layer ZnO and In₂O₃ devices, is largely attributed to the low temperature annealing (≤ 200 °C) employed and to the incomplete conversion of the metal oxide precursor materials.

The nature of electron transport in single and multilayer TFTs was further studied by analysing the V_G -dependence of μ_{SAT} using a generalized form of the power law with appropriate values of K and γ :^[25]

$$\mu_{FE} = K(V_G - V_{TH,P})^\gamma \quad (1)$$

Here, μ_{FE} , V_G , V_{TH} , and V_P are the field-effect mobility, gate, threshold voltages and percolation voltage, respectively. **Figure S5** displays the V_G -dependence of μ_{FE} for ZnO, In₂O₃ IZ and IZIZ TFTs with the corresponding power law fittings (solid lines). The γ was fitted in two distinct bias regions, the low field ($V_G - V_T$) and the high field ($V_G - V_P$) one. The values of the prefactor K used for the different fittings are summarized in **Figure S6**. It has previously been shown that both K and γ are related to nature of the charge transport mechanism in the semiconductor channel.^[25] For example, a value for γ close to 0.7 is indicative of a trap limited conduction (TLC) process, whilst a value of close to 0.11 a percolation dominated conduction (PC) mechanism. As evident from **Figure S5**, the γ values for In₂O₃, IZ, and IZIZ transistors in the low field bias regime are 0.28, 0.26, and 0.24, respectively, and 0.12, 0.12, and 0.11 in the high field regime. For ZnO the γ value is 0.84 in the low field and equal to 0.4 in high field regime, respectively. These results indicate that electron transport in In₂O₃ TFTs is a PC dominated process while in ZnO TFTs a TLC process dominates.^[8] Notably, even though the μ_{FE} values for In₂O₃/ZnO ($6.25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and IZIZ ($11.4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) TFTs are significantly higher than that of In₂O₃ TFTs ($1.6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), the conduction process appears to be governed by the same mechanism (i.e. PC). This rather interesting finding corroborates the central role that the first

In₂O₃ layer plays in electron transport across Type-II devices and particularly the heterojunction and superlattice channel TFTs.

In an effort to understand the origin of the different conduction mechanisms, we studied the subthreshold swing (*SS*) for both types of TFTs. The analysis allows estimation of the total electron trap density in the channel and includes interface and bulk trap states. As expected, the *SS* value for ZnO TFTs (1.92 V/dec) is significantly higher than for In₂O₃ TFTs (0.89 V/dec), indicative of a higher concentration of electron traps ($1.01 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ and 4.53×10^{11} for ZnO and In₂O₃, respectively)^[26]. As the channel complexity increases with the introduction of the heterojunction IZ and superlattice IZIZ structures, the *SS* decrease further to 0.56 and 0.43 V/dec, respectively. This trend correlates with the increasing μ_{SAT} seen in IZ and IZIZ transistors (**Table 1**). Possible reasons for the lower trap concentrations seen in these multilayer TFTs include; (i) trap filling due to the excess free electrons induced at the vicinity of the In₂O₃/ZnO heterointerface(s) upon heterojunction formation, and/or (ii) passivation of trap states located on the surface of the ultra-thin In₂O₃ layer due to interaction with the subsequently deposited ZnO. To this end, our observations are in agreement with the previously reported studies on the temperature dependence measurement of electron transport in multilayer oxide TFTs based on the same materials combination, which has revealed trap deactivation upon formation of the In₂O₃/ZnO interface.^[14]

Next, we investigated the positive bias-stress (PBS) characteristics of the multilayer TFTs and compared them to single layer devices. **Figure 4d** show the transfer characteristics for In₂O₃, ZnO, In₂O₃/ZnO and IZIZ TFTs measured at different bias stress periods, while **Figure 4e** displays a summary of the threshold voltage shift (ΔV_{TH}) versus stress time for all types of devices studied. Evidently, In₂O₃/ZnO and IZIZ TFTs exhibits the smallest ΔV_{TH} when compared to single layer In₂O₃ and ZnO devices. On the other hand, analysis of the turn-on voltage shift (ΔV_{ON}) reveals an even smaller shift (**Figure S7a**), in magnitude, to that of V_{TH} .

The improved stability of the In₂O₃/ZnO over IZIZ TFT is attributed to the presence of a single interface and the difference in the density of deep traps. This advantage however comes at the expense of μ_{FET} as IZIZ TFTs maintain their superior performance during bias stressing (**Figure S7b**). A further noteworthy observation in **Figures 4e** and **S7a** is that both the IZ and IZIZ TFTs exhibit good recovery. Specifically, the transfer curves for the In₂O₃/ZnO TFT measured after recovery appear almost identical to that measured at $t = 0$ s (as prepared TFT). On the other hand, the bias stress of single layer In₂O₃ and ZnO is significantly higher but with different recovery behavior. The In₂O₃ TFTs recover almost fully after removal of the bias while ZnO device does not (**Figure 4e**). To gain further insights into the bias-stress behaviour of the different TFTs, the experimental data of **Figure 4d** were analysed using the stretched exponential function:

$$\Delta V_{\text{TH}}(t) = \Delta V_{\text{O}} [1 - e^{-(\frac{t}{\tau})^\beta}] \quad (2)$$

where $\Delta V_{\text{O}} = V_{\text{TH}}(30\text{ k s}) - V_{\text{TH}}(0\text{ s})$, with $V_{\text{TH}}(0)$ and $V_{\text{TH}}(30\text{ k s})$ being the threshold voltage prior to and after bias stress for 30k s, respectively, τ is the relaxation time, β the stretching parameter with a numerical value ranging from 0 to 1, and t the stress time.^[27]

Figure S8 shows the fits of the stretched exponential function to V_{TH} as a function of PBS time for four channel configurations, namely In₂O₃, ZnO, IZ, IZIZ. In₂O₃ and ZnO transistors exhibit similar β and τ values of 0.51 and 0.50, and 2.34×10^5 and 2.32×10^5 s, respectively. Multi-layered IZ and IZIZ devices, on the other hand, show lower $\beta \approx 0.30$ and 0.28 and longer $\tau \approx 2.69 \times 10^7$ and 1.46×10^7 s, respectively. These differences suggest that multilayer TFTs requires longer times to reach an equilibrium condition under continuous bias stress.

Finally, we have explored the possibility of improving the electron mobility in heterojunction and superlattice oxide TFTs via modulation doping (MOD). Effective n-type doping of the ZnO layers was achieved using lithium (Li) following previously described

Adv. Funct. Mater. **2019**, 1902591
 methods.^[28] ^[15] **Figure 5a** displays representative transfer characteristics of In₂O₃/Li-ZnO/In₂O₃/Li-ZnO (Li-IZIZ) (red solid line) and pristine (undoped) IZIZ TFTs (blue line). Li-IZIZ TFTs exhibit significantly improved μ_{SAT} ($\approx 18 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) accompanied by V_{Th} shift towards more negative V_{G} , with devices showing improved parameter uniformity. **Figure 5b** and **5c** display transfer characteristics of 10 TFTs and variation of μ_{SAT} and V_{TH} , respectively. The MOD Li-IZIZ TFTs exhibit consistently higher μ_{SAT} and small device-to-device variation with an average $\mu_{\text{FET}} \approx 18 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (standard deviation of 0.79), a maximum $\mu_{\text{FET}} \approx 19.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and an average V_{TH} of 2.59 V (standard deviation of 0.54).

An important advantage of the multilayer MOD oxide TFTs is that high μ_{FET} values can be achieved even at modest annealing temperatures ($\leq 200 \text{ }^\circ\text{C}$), hence making the technology compatible with inexpensive but temperature sensitive substrate materials such as plastic. To demonstrate the opportunities offered by this processing advantage we developed flexible, low-voltage Li-IZIZ TFTs on polyethylene naphthalate (PEN) substrates. **Figure 5d** show a schematic of the low-voltage MOD Li-IZIZ TFT architecture developed together with a photograph of an actual transistor array. The solution-processed AlOx/ZrOx bilayer was employed as the gate dielectric as it combines excellent insulating characteristics with high dielectric permittivity.^[14] A set of representative transfer and output characteristics are presented in **Figure 5e** and **5f**, respectively. The high areal capacitance of AlOx/ZrOx (235 nF cm^{-2}) enables low-voltage operation ($\pm 1.5 \text{ V}$) and high μ_{FET} values of up to $25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ measured at $V_{\text{D}} = 1 \text{ V}$.

In conclusion, we developed heterojunction and superlattice n-channel metal oxide TFTs via sequential solution deposition of ultra-thin (5-10 nm) layers of In₂O₃ and ZnO. A remarkable dependence of the electron transport on the sequence with which the oxide layers are deposited, was discovered. We showed that depositing In₂O₃ first followed by the ZnO layer, yields optimal device performance. Reversing the layer order resulted to a dramatic degradation in the electron transport. The observation was attributed to: (i) the atomically smooth and highly

crystalline nature of In_2O_3 layer which facilitates the formation of an ultra-smooth heterointerface following the deposition of the ZnO layer, and (ii) the formation of a q2DEG-like system at the vicinity of the heterointerface driven by the conduction band discontinuity and/or the interface chemistry. Moreover, the multilayer TFTs exhibited improved bias-stress stability when subjected to continuous bias ($V_G = 40$ V, $V_D = 20$ V) for 30k s. N-doping of ZnO layers with Li was used to further enhance the electron mobility of the superlattice TFTs to values approaching $20 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Finally, by combining the solution-processed $\text{AlO}_x/\text{ZrO}_x$ bilayer dielectric^[24] and the modulation-doped superlattice channels, we demonstrated low operating voltage ($V_D = 1$ V, $V_G = -1 \sim 1.5$ V) TFTs with an outstanding maximum electron mobility of $\approx 25 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

Experimental Section

Oxide Precursor Preparation: In_2O_3 precursor solutions were prepared by dissolving anhydrous indium nitrate ($\text{In}(\text{NO}_3)_3$, 99.99%; Indium Corporation) in 2-Methoxyethanol at 20 mgmL^{-1} and stirred at room temperature for 24 hours before processing. ZnO precursor solutions were prepared by dissolving ZnO nanopowder (>97 % Sigma-Aldrich) in ammonium hydroxide (50% v/v; Alfa Aesar) at 8 mgmL^{-1} and stirred at room temperature for 24 hours before using. Lithium acetate (LiOOCCH_3) was used as the source of Li and was dissolved in a (1:1) blend of ammonium hydroxide and 2-Methoxyethanol). Li-doping of the ZnO and In_2O_3 precursor formulations was implemented via solution blending with the Lithium acetate solution at appropriate mol%. For ZrO_2 deposition, the precursor solution was synthesized by dissolving Zr (IV) acetylacetonate ($\text{Zr}(\text{C}_5\text{H}_7\text{O}_2)_4$) (98%; Sigma-Aldrich) in N,N dimethylformamide (DMF, $\text{C}_3\text{H}_7\text{NO}$) (Sigma-Aldrich) at a concentration of 0.15 M in inert gas atmosphere with the addition of an equal molar concentration of ethanolamine (MEA, $\text{C}_2\text{H}_7\text{NO}$) ($\geq 99\%$; Sigma-Aldrich). The solution was then subjected to rigorous stirring at 70–80 °C for 1 h before use.

Transistor Fabrication: Wafers composed of heavily doped silicon (Si^{++}), acting as the gate electrode, and a thermally grown SiO_2 layer (400 nm or 100 nm thick) as the gate dielectric were used as the substrates. As-received wafers were cleaned in ultra-sonic baths of deionized water, acetone, and iso-propanol, sequentially, for 10 min each. The substrates were then subject to the UV ozone treatment in order to improve the wettability of the surfaces before spin-cast of the precursor formulations. In_2O_3 and ZnO were both deposited by spin-coating in air. In_2O_3 precursor solution was first coated onto $\text{Si}^{++}/\text{SiO}_2$ wafers at 4000 rpm for 30s and annealed at 200°C for 15 min. The In_2O_3 layer was then subjected to a 5-min UV ozone treatment in order to increase its surface wettability and improve the material stoichiometry. ZnO (or Li-ZnO) precursor solution was spin-coated at 6000 rpm for 30 s and annealed at 200°C for 15 min. The entire film deposition process was carried out in ambient atmosphere. $\text{In}_2\text{O}_3/\text{ZnO}$ heterojunctions were grown through sequential deposition of the two materials using the same conditions. Transistor fabrication was completed with the deposition of the top Al (40 nm) source/drain electrodes via thermal sublimation through metal stencil masks in high vacuum (10^{-6} mbar). For flexible, low-voltage device, PEN plastic substrates was used. Following substrate cleaning, 40 nm thick Al gate electrodes were deposited by thermal evaporation through a shadow mask. The native aluminium oxide was grown on the surface of the Al gate electrodes using a low pressure mercury UV lamp, which emits at wavelengths of 253.7 nm (97% of overall power) and of 184.9 nm (3% of overall power) at total output power of approximately 5 mWcm^{-2} (at a distance of 1 cm). The entire UV illumination was taken in ambient air for 10-12 h. Following, the ZrO_2 film was grown by spin-coating the precursor solution at 3000 rpm for 60 s in nitrogen followed by curing the samples using a metal halide lamp of 250 mWcm^{-2} , equipped with a UVA spectrum filter, for 90 min in ambient air.

Atomic Force Microscopy (AFM) Measurement : Atomic force micrographs of the films were taken in the tapping mode using an Agilent 5500 AFM in air.

Transistor characterization: The FET electrical characterisation was carried out using an Agilent B2902A parameter analyzer in a nitrogen-filled glove box. The μ_{FET} and V_{Th} values were extracted at the saturation region using the gradual channel approximation equation.

Capacitance-voltage (C-V) measurement: C-V measurements were carried out on metal-insulator-semiconductor (MIS) structures in order to investigate the electron concentration throughout the $\text{In}_2\text{O}_3/\text{ZnO}$ films. These MIS devices were fabricated and evaluated using an $\text{Al}/\text{AlOx}/\text{ZrOx}/\text{In}_2\text{O}_3/\text{ZnO}/\text{Au}$ structure. The MIS structure was fabricated by an Al bottom electrode (oxidised via UV/ozone exposure to create a thin layer of AlOx) and a film of solution processed zirconium oxide. The semiconducting layers of In_2O_3 and ZnO were sequentially deposited by spray and spin coating processes, respectively, and finally a thermally evaporated Au top electrode concluded the device fabrication.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

D.K., Y.H.L., and T.D.A. are grateful to the European Research Council (ERC) AMPRO project no. 280221 for financial support. T.D.A. is grateful to King Abdullah University of Science and Technology (KAUST) for the financial support.

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

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Figures

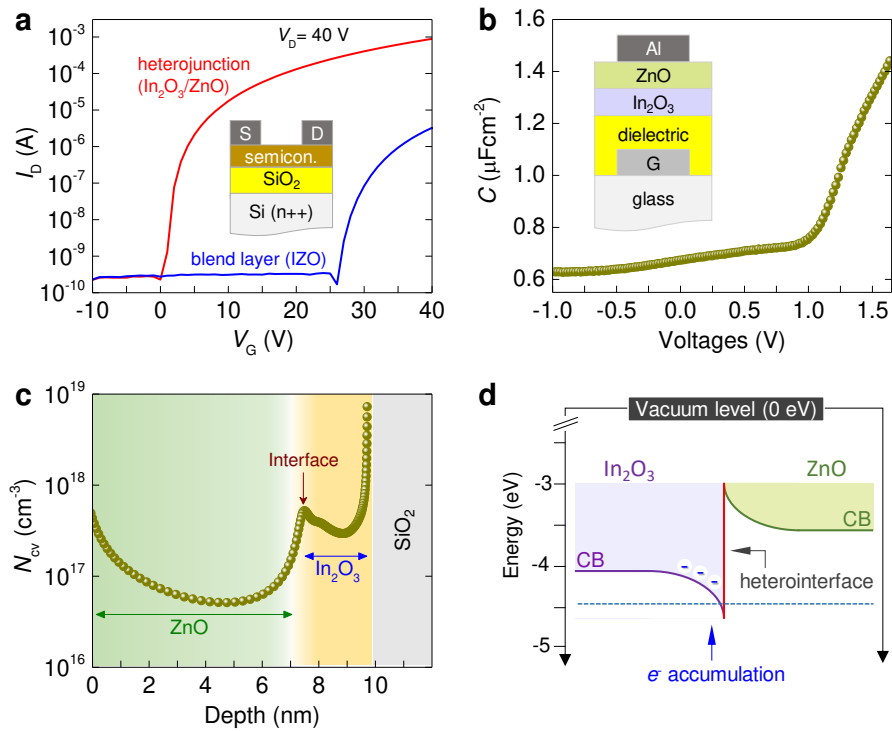


Figure 1. (a) Transfer characteristics measured for a heterojunction In₂O₃/ZnO and a single blend In₂O₃:ZnO (IZO) layer TFTs both annealed at 200 °C in ambient atmosphere. Inset: Schematic of the TFT architecture employed. (b) capacitance-voltage (C-V) characteristic of a metal-insulator-semiconductor (MIS) capacitor based on the bilayer In₂O₃/ZnO as the semiconductor layer. Inset: Schematic cross-section of the MIS device. (c) Distribution of apparent charge carrier density (N_{cv}) estimated from the C-V data as a function of heterojunction depth (x), where $x = 0$ nm represents the ZnO/Al interface. (d) Energy band diagram of the In₂O₃/ZnO heterointerface.

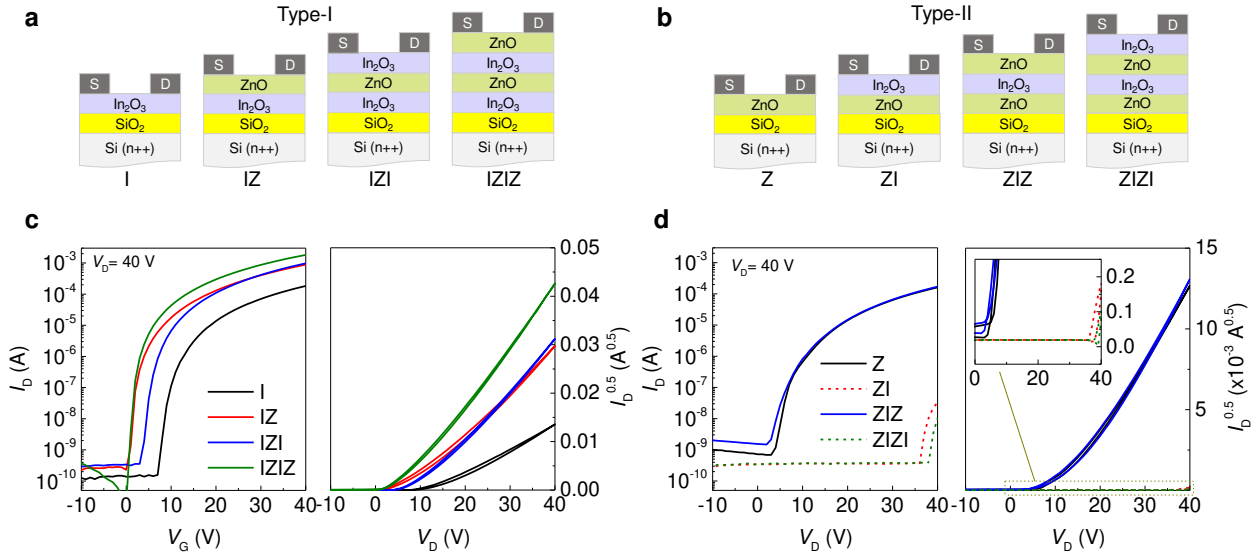


Figure 2. (a) Schematics of Type-I series of the metal-oxide transistors including single layer In_2O_3 (I), $\text{In}_2\text{O}_3/\text{ZnO}$ (IZ), $\text{In}_2\text{O}_3/\text{ZnO}/\text{In}_2\text{O}_3$ (IZI), and $\text{In}_2\text{O}_3/\text{ZnO}/\text{In}_2\text{O}_3/\text{ZnO}$ (IZIZ). (b) Schematics of the Type-II transistor architectures developed including single layer ZnO (Z), $\text{ZnO}/\text{In}_2\text{O}_3$ (ZI), $\text{ZnO}/\text{In}_2\text{O}_3/\text{ZnO}$ (ZIZ), and $\text{ZnO}/\text{In}_2\text{O}_3/\text{ZnO}/\text{In}_2\text{O}_3$ (ZIZI) TFTs. (c) Transfer characteristics and corresponding $I_D^{0.5}$ vs. V_G plots for Type-I TFTs. (d) Transfer characteristics and corresponding $I_D^{0.5}$ vs. V_G plots for Type-II TFTs. Inset: Zoom in region of the plot highlighting the huge difference between Type-II TFTs based on odd and even number of alternating oxide layers.

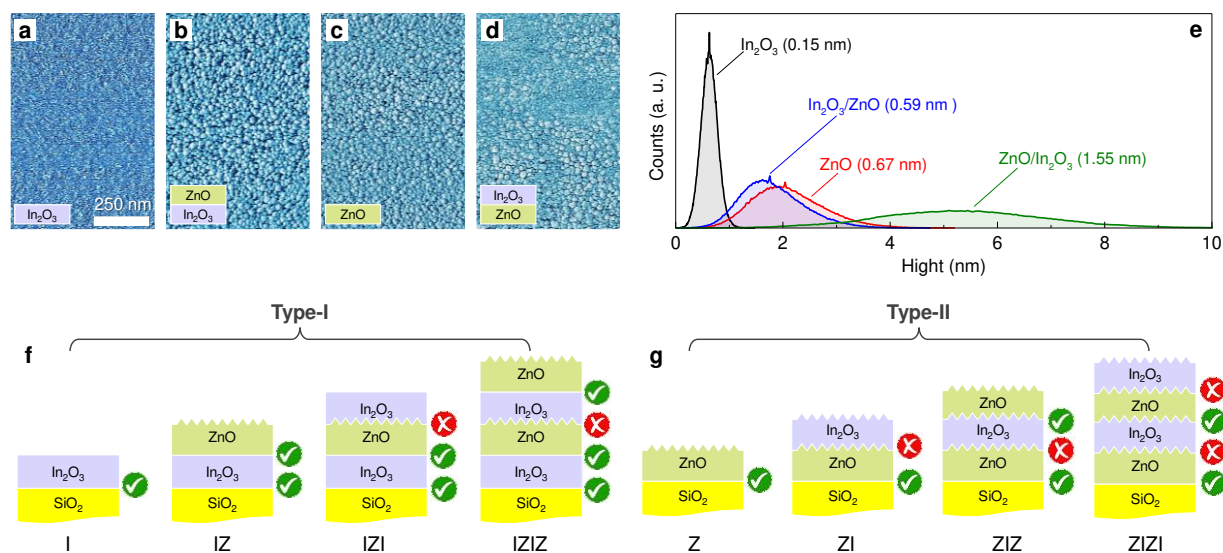


Figure 3. Atomic force microscope (AFM) images of the surface topography of: (a) In_2O_3 , (b) $\text{ZnO}/\text{In}_2\text{O}_3$ (ZI), (c) ZnO , and (d) $\text{In}_2\text{O}_3/\text{ZnO}$ (IZ) layers, respectively, and (e) the corresponding height histograms. Illustrations of Type-I (f), and Type-II (g) heterointerfaces. Smooth/low-quality $\text{In}_2\text{O}_3/\text{ZnO}$ heterointerfaces are indicated with green tick marks, whilst rougher/lower-quality $\text{ZnO}/\text{In}_2\text{O}_3$ heterointerfaces are indicated with red crosses.

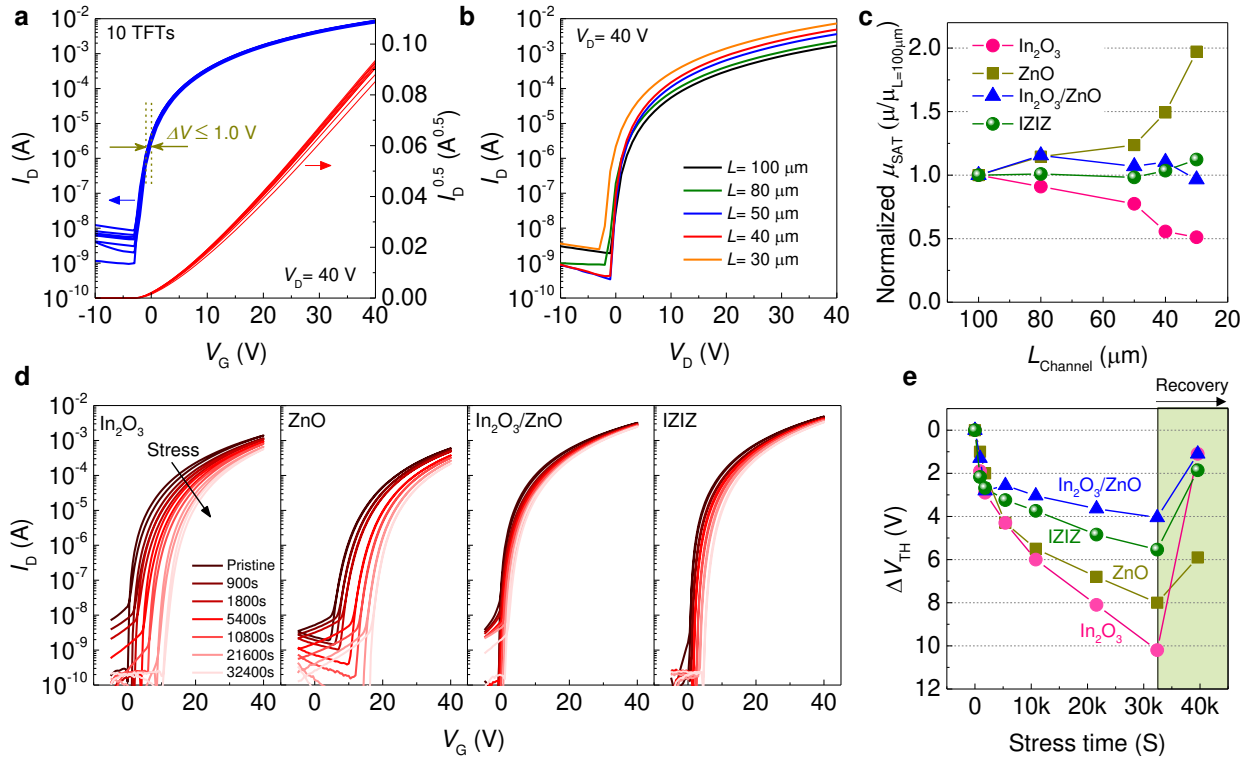


Figure 4. (a) Transfer characteristics of 10 different IZIZ TFTs fabricated simultaneously. (b) Transfer characteristics of IZIZ transistors with different channel lengths (L). (c) Channel length dependent μ_{SAT} of In_2O_3 (black), ZnO (red), $\text{In}_2\text{O}_3/\text{ZnO}$ (blue), and IZIZ (green) transistors. (d) Transfer characteristics of In_2O_3 , ZnO, $\text{In}_2\text{O}_3/\text{ZnO}$, and IZIZ transistors obtained before and during bias-stressing under constant $V_G = 40$ V and $V_D = 20$ V. (e) Time dependence of V_{Th} shift (ΔV_{Th}) under continuous bias stress and the corresponding recovery stage (shaded area).

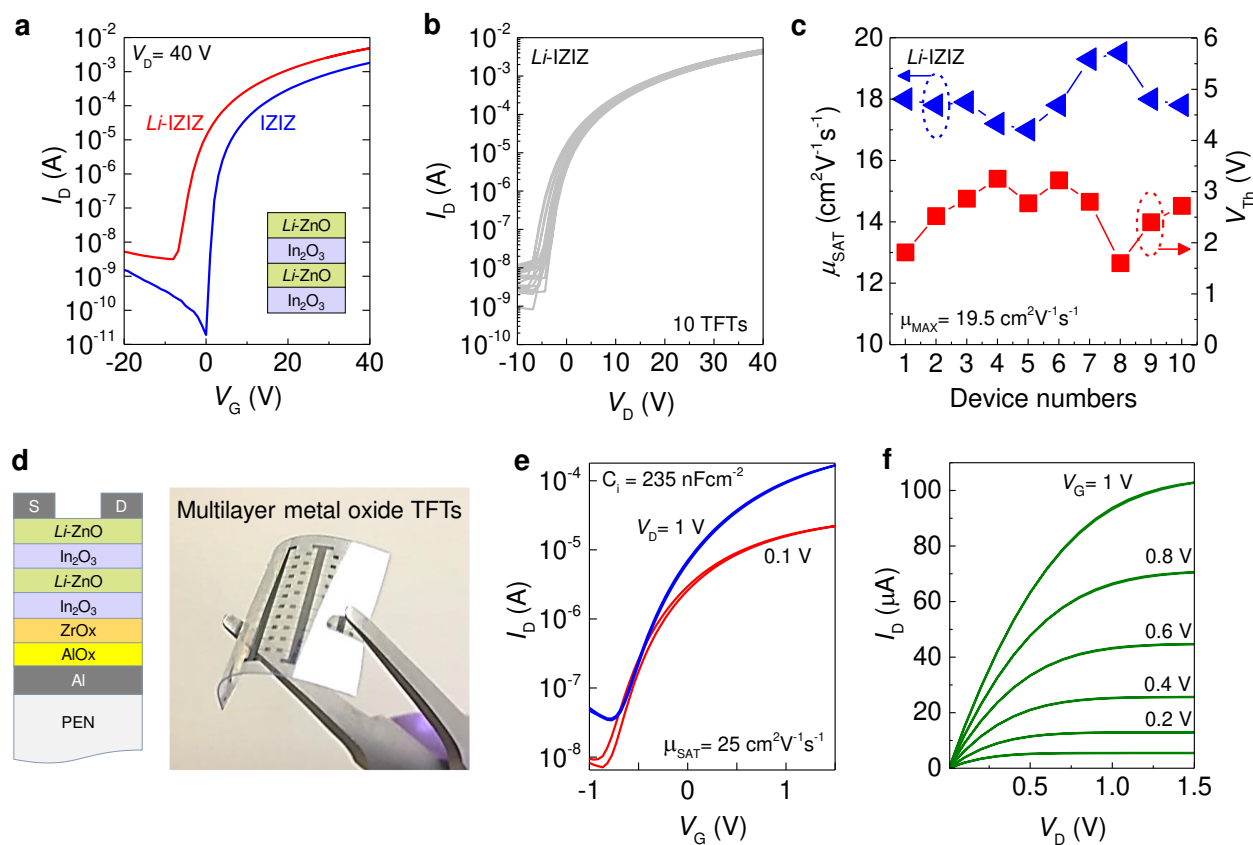


Figure 5. (a) Transfer characteristics of pristine and Li-doped IZIZ transistors. Inset: Schematics of Li-doped IZIZ superlattice employed as the channel system. (b) Transfer characteristics of 10 Li-IZIZ TFTs. (c) Variation of the electron mobility (μ_{SAT}) and threshold voltage (V_{Th}) of 10 Li-doped IZIZ transistors fabricated on the same substrate. (d) Schematic of the Li-IZIZ transistor architecture and a photograph of the actual transistor fabricated on a flexible PEN substrate. Representative sets of transfer (e) and output (f) characteristics of a low operating voltage Li-IZIZ transistor.

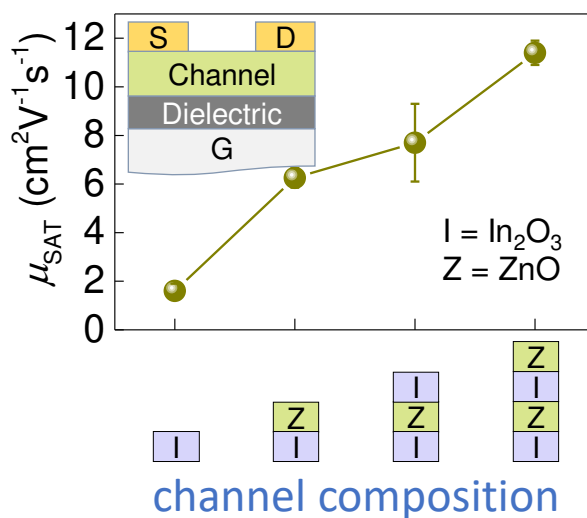
ToC Text

Solution-processed heterojunction and superlattice channel transistors composed of sequentially deposited In_2O_3 and ZnO layers show remarkably different operating characteristics depending on the stack configuration. The difference relates to the quality of the heterointerface and its dependence on the material deposition sequence. Optimised superlattice transistors fabricated on plastic substrates operate at ± 1.5 V with a maximum electron mobility of $25 \text{ cm}^2/\text{Vs}$.

Keyword: Metal oxide semiconductors; thin-film transistors; doping; heterojunction transistor; solution processing

Dongyoon Khim, Yen-Hung Lin, Thomas D. Anthopoulos**

Impact of Layer Configuration and Doping on Electron Transport and Bias Stability in Heterojunction and Superlattice Metal Oxide Transistors



Supporting Information

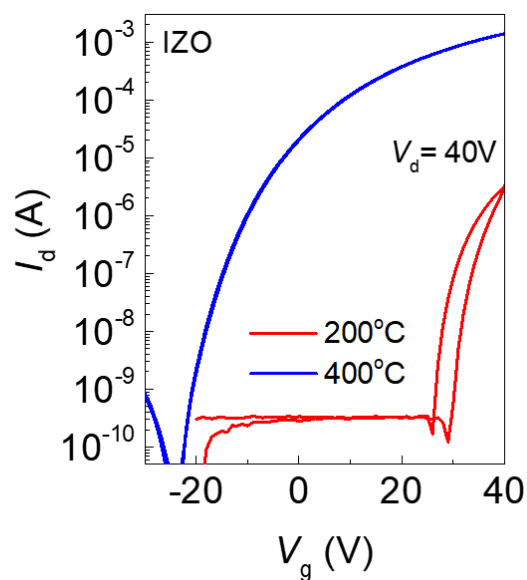
Impact of Layer Configuration and Doping on Electron Transport and Bias Stability in Heterojunction and Superlattice Metal Oxide Transistors*Dongyoon Khim*, Yen-Hung Lin, Thomas D. Anthopoulos**

Figure S1. Transfer characteristics of bottom-gate, top-contact IZO TFTs fabricated by spin-coating of a blend of precursor materials followed by thermal annealing at 200 °C (red) and 400 °C (blue) in ambient air.

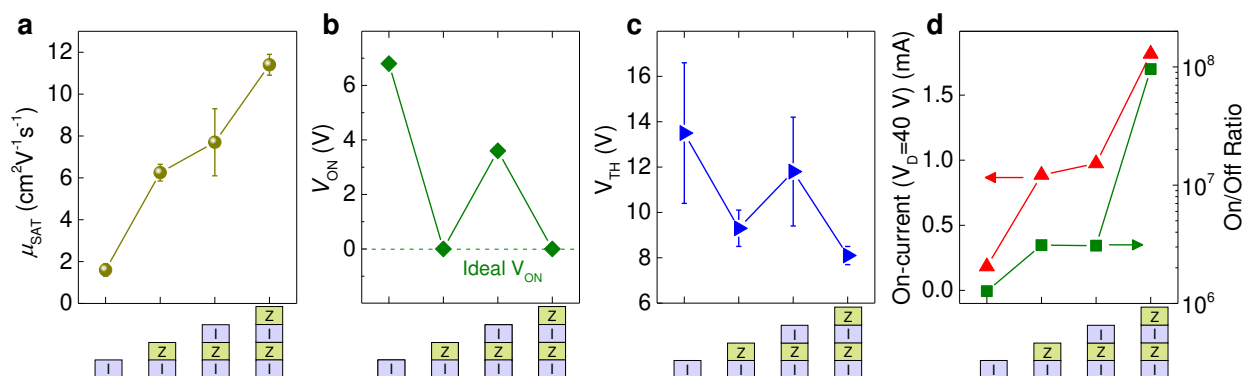


Figure S2. Evolution of; (a) saturation electron mobility (μ_{SAT}), (b) on-set voltages (V_{ON}), (c) threshold voltages (V_{TH}) and (d) on-current and on/off current ratio as a function of channel configuration for Type-I TFTs.

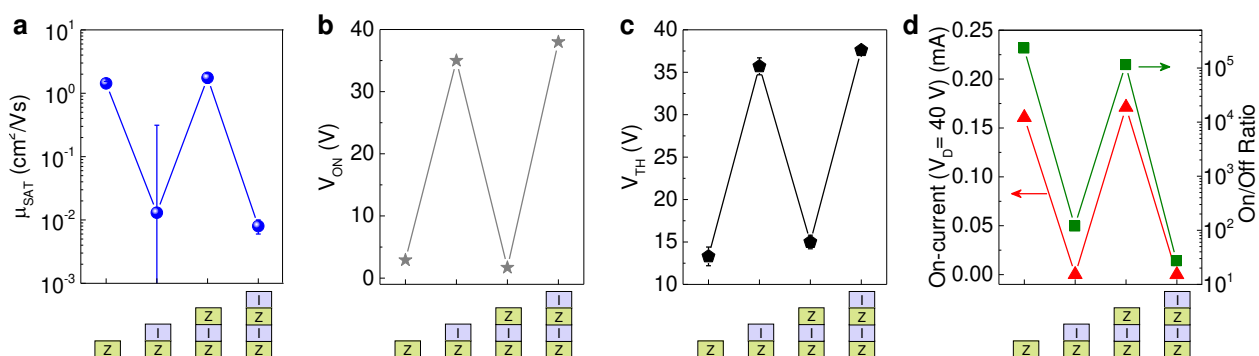


Figure S3. Evolution of, (a) saturation electron mobility (μ_{SAT}), (b) on-set voltages (V_{ON}), (c) threshold voltages (V_{TH}), and (d) on-current and on/off current ratio as a function of channel configuration for Type-II TFTs.

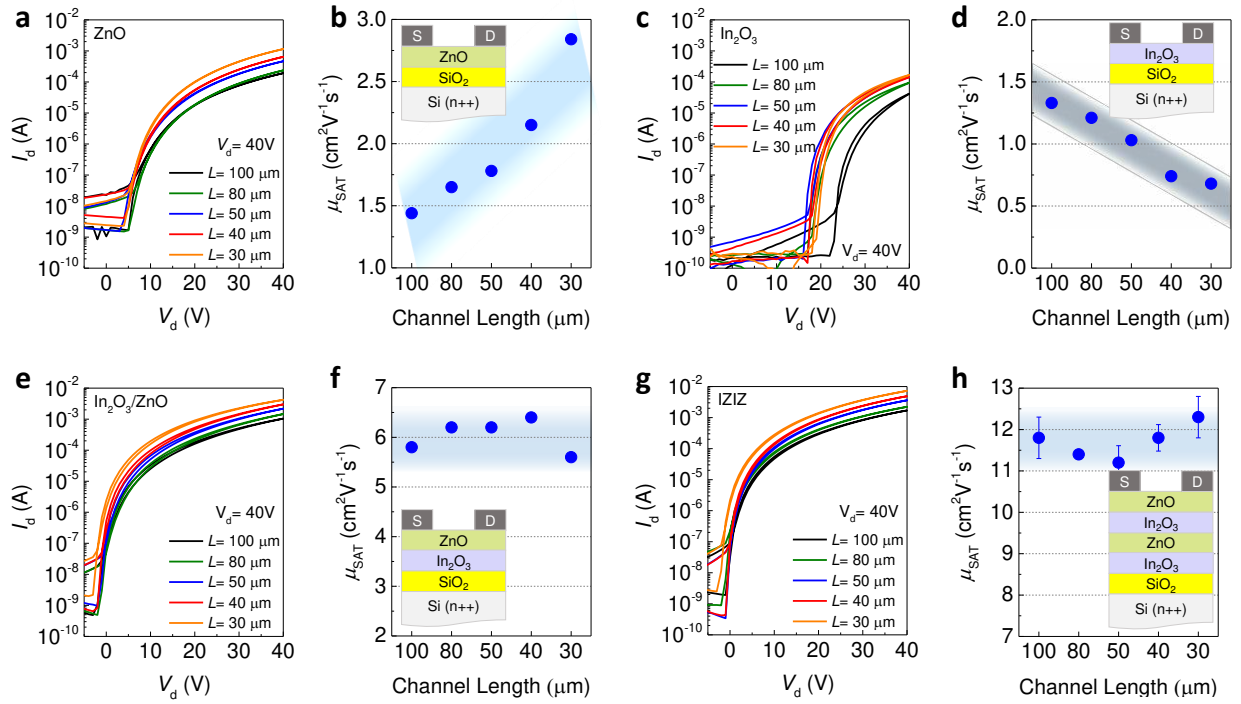


Figure S4. Transfer characteristics of TFTs with different channel lengths and the corresponding μ_{SAT} values for ZnO [(a) and (b)], In_2O_3 [(c) and (d)], $\text{In}_2\text{O}_3/\text{ZnO}$ [(e) and (f)], and IZIZ [(g) and (h)] devices.

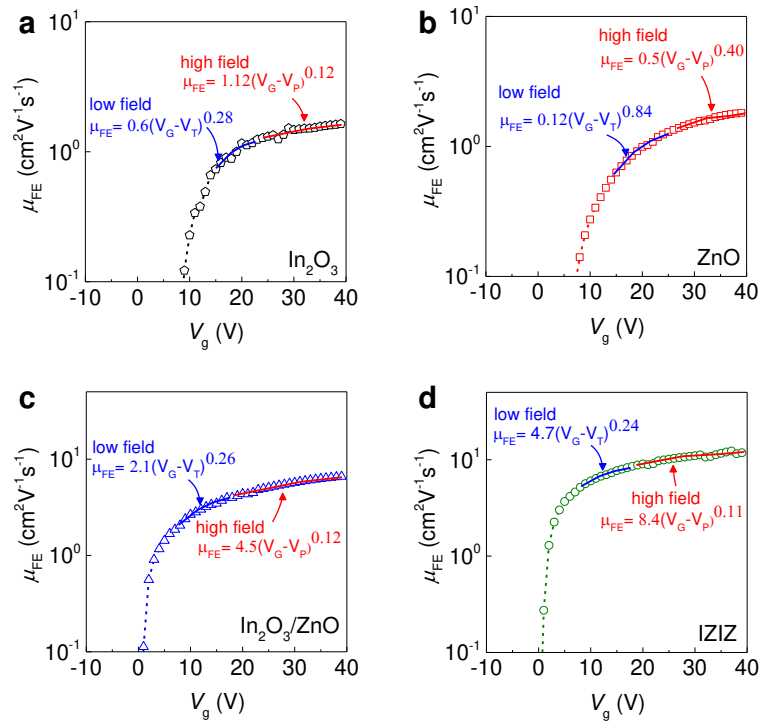


Figure S5. (a) Gate-voltage dependence of the electron mobilities of: (a) In_2O_3 , (b) ZnO, (c) $\text{In}_2\text{O}_3/\text{ZnO}$, and (d) IZIZ TFTs. Solid lines (solid blue line for low-field, and red line for high-field) are the fits to the power law equation.

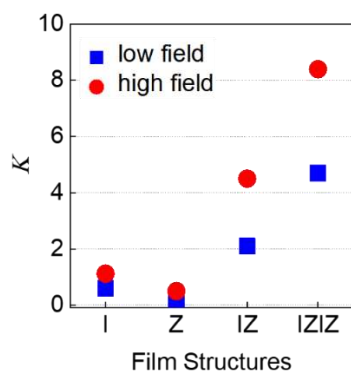


Figure S6. Prefactor K values according to the power law equation $\mu_{FE} = K(V_G - V_{T,P})^\gamma$ of In_2O_3 , ZnO , $\text{In}_2\text{O}_3/\text{ZnO}$, and IZIZ TFTs.

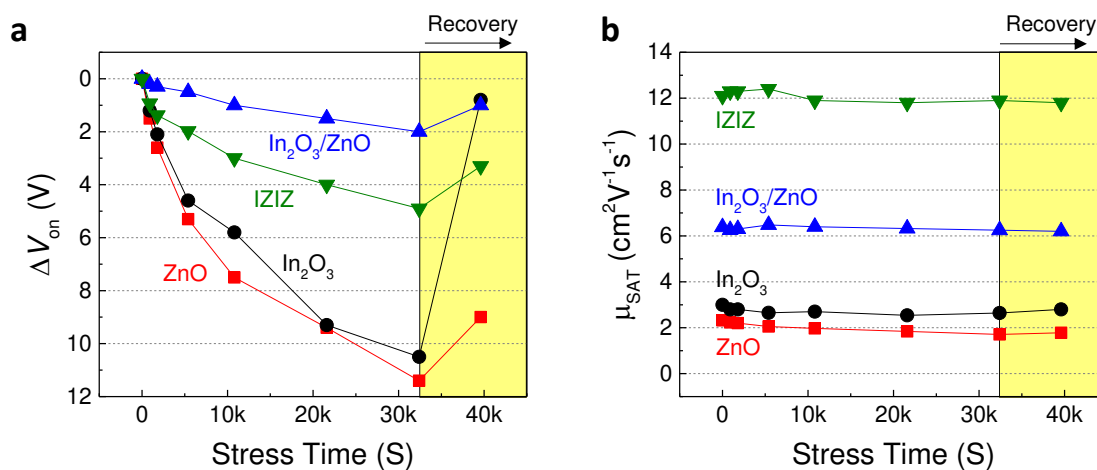


Figure S7. Time dependence of (a) V_{on} shift (ΔV_{on}) and (b) μ_{SAT} under bias stress and recovery states.

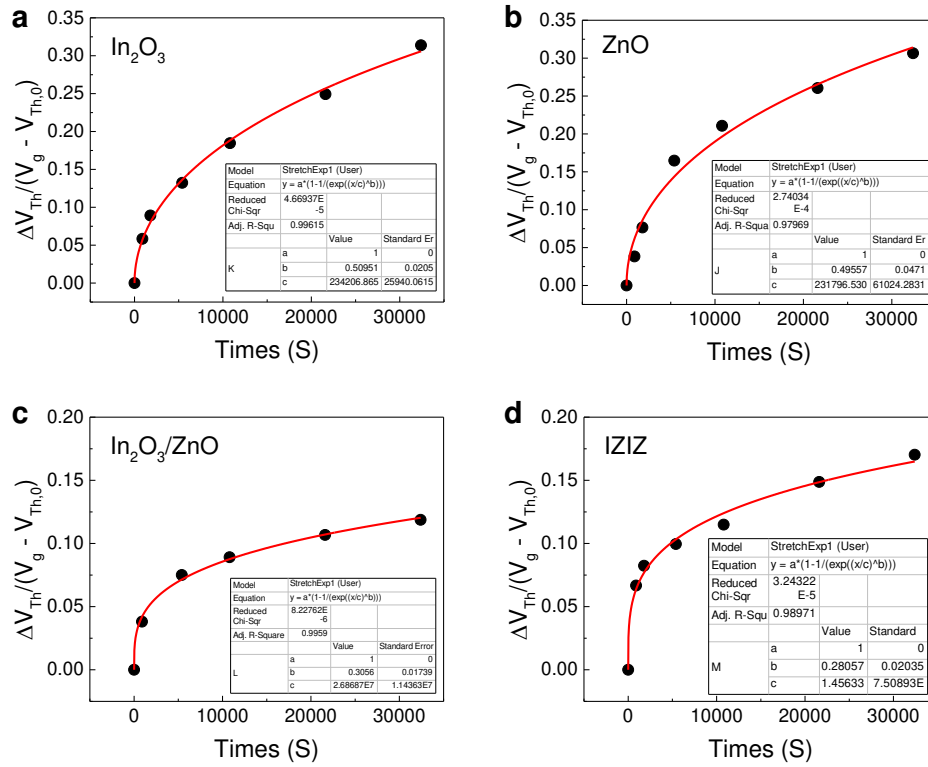


Figure S8. Time dependence of $\Delta V_{\text{Th}}/(V_g - V_{\text{Th},0})$ for gate bias stresses of (a) In_2O_3 , (b) ZnO , (c) $\text{In}_2\text{O}_3/\text{ZnO}$, and (d) IZIZ TFTs. The measured data are well fitted with a stretched-exponential equation with a characteristic trapping time τ and a stretched-exponential exponent β .

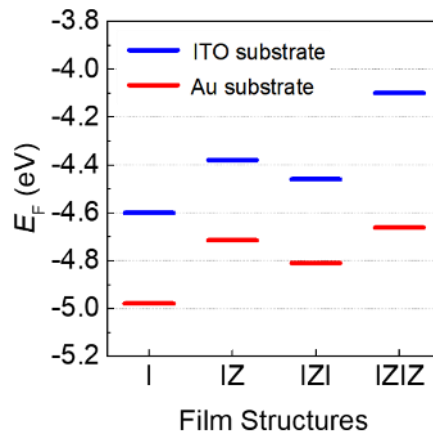


Figure S9. Fermi energy level in In_2O_3 , $\text{In}_2\text{O}_3/\text{ZnO}$ (IZ), IZI, and IZIZ layers deposited on ITO and Au substrates measured by Kelvin probe (KP).

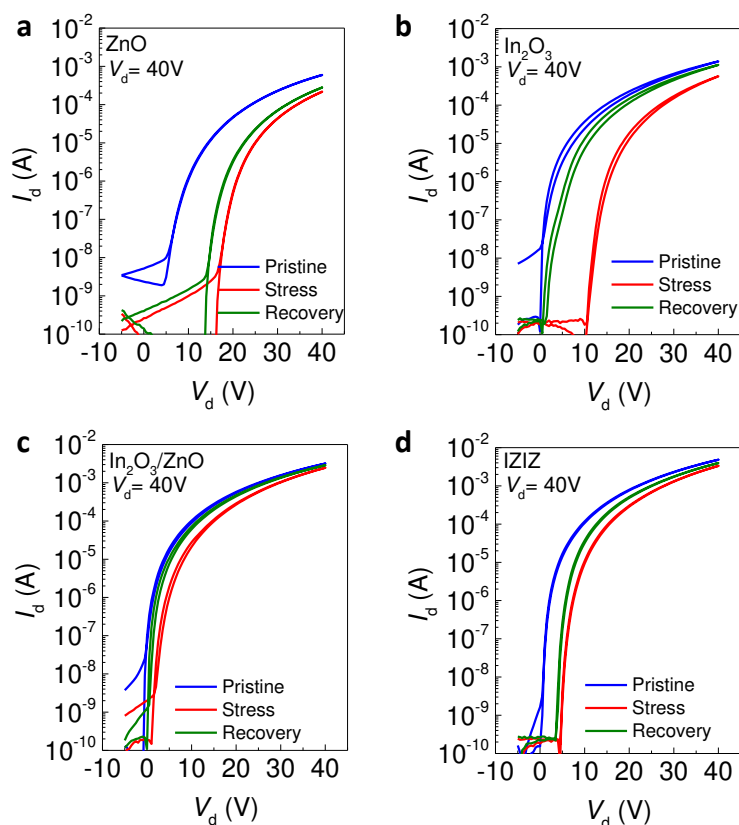


Figure S10. Transfer characteristics of before (blue) and after (red) bias stress and after recovery (green) of 15,000s of (a) ZnO, (b) In₂O₃, (c) In₂O₃/ZnO (IZ), and (d) IZIZ TFTs.

Table S1. Summary of the bias stress effect on μ_{SAT} , V_{Th} , and V_{on} depending on stress time and trapping time τ and a stretched-exponential exponent β of the various channel architectures investigated.

| Bias-stress condition | ZnO | | | In ₂ O ₃ | | | In ₂ O ₃ /ZnO | | | IZIZ | | |
|-----------------------|--|---------------------|---------------------|--|---------------------|---------------------|--|---------------------|---------------------|--|---------------------|---------------------|
| | μ_{SAT} (cm ² /Vs) | V_{Th} (V) | V_{on} (V) | μ_{SAT} (cm ² /Vs) | V_{Th} (V) | V_{on} (V) | μ_{SAT} (cm ² /Vs) | V_{Th} (V) | V_{on} (V) | μ_{SAT} (cm ² /Vs) | V_{Th} (V) | V_{on} (V) |
| Pristine (no-stress) | 2.32 | 13.9 | 4.6 | 3.0 | 7.5 | 0 | 6.38 | 5.90 | -1.0 | 12.1 | 7.46 | 0 |
| 900 s | 2.23 | 14.9 | 6.1 | 2.8 | 9.4 | 1.2 | 6.26 | 7.2 | -0.8 | 12.3 | 9.63 | 0.93 |
| 1,800 s | 2.20 | 15.9 | 7.2 | 2.8 | 10.4 | 2.1 | 6.30 | 8.71 | -0.7 | 12.3 | 10.14 | 1.38 |
| 5,400 s | 2.05 | 18.2 | 9.9 | 2.65 | 11.8 | 4.6 | 6.48 | 8.46 | -0.5 | 12.4 | 10.7 | 1.98 |
| 10,800 s | 1.97 | 19.4 | 12.1 | 2.70 | 13.5 | 5.8 | 6.40 | 8.94 | 0 | 11.9 | 11.2 | 3.0 |
| 21,600 s | 1.84 | 20.7 | 14.0 | 2.54 | 15.6 | 8.3 | 6.32 | 9.54 | 0.5 | 11.8 | 12.3 | 4.0 |
| 32,400 s | 1.71 | 21.9 | 16.0 | 2.64 | 17.7 | 10.5 | 6.25 | 9.95 | 1.0 | 11.9 | 13.0 | 4.9 |
| Recovery (2 h) | 1.78 | 19.8 | 13.6 | 2.8 | 8.6 | 0.8 | 6.20 | 7.0 | 0 | 11.8 | 9.32 | 3.3 |
| β | 0.49 | | | 0.50 | | | 0.31 | | | 0.28 | | |
| τ (s) | 2.31×10^6 | | | 2.34×10^6 | | | 2.69×10^7 | | | 1.46×10^7 | | |