Impact of Layout on 90nm CMOS Process Parameter Fluctuations

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Abstract
A test chip has been built to study the effects of layout on the delay and leakage of digital circuits in 90nm CMOS. The delay is characterized through the spread of ring oscillator frequencies and the transistor leakage is measured by using an on-chip ADC.

Introduction

Increased process parameter variation has been perceived as one of the major roadblocks to further technology scaling. The corner-based design approach treats all variations as random. As the corner spread is increasing with technology scaling, simultaneously satisfying performance, power and yield requirements becomes challenging. In order to better account for the variability in the design process, it is necessary to distinguish systematic shifts in parameter values from truly random ones. The variations are generally characterized as within-die (WID), die-to-die (D2D) [1]. While these relationships are generally known at the process level, they are hardly visible to the designer.

Test Chip

The test chip, implemented in a general-purpose 90nm technology is used to evaluate the distributions of WID and D2D variations in ring oscillator frequencies and transistor standby leakage currents. The purpose of the experiment is to evaluate the absolute magnitude of WID and D2D variations, its spatial correlation, and the impact of layout styles. The chip contains an array of 10x16 tiles, occupying 1mm × 1mm area. Each tile has twelve 13-stage ring oscillators (ROs) and 12 transistors in the off-state, each with a different layout (Fig.1). The ring oscillators contain inverters with a single poly finger, as well as a stack of three fingers. Poly density, poly orientation and metal coverage are varied in the layout. To automate a large number of measurements, the RO frequency is divided down and its value is scanned out of the chip [2]. The tiles at the perimeter of the die are ignored in the measurements to eliminate edge effects. A single-slope ADC implemented using a high-gain folded-cascade amplifier with 2.5V devices, a large on-chip metal fringe capacitor and comparators was implemented on chip to measure transistor off-currents between 1nA to 1µA (Fig.2).

Measurement Results

Measured data shows three dominant and distinctive trends (Fig.3). The WID frequency variation for the same layout is small, up to 1.2% of the std. deviation/median (σ/µ). The systematic median frequency spread over RO layouts with different poly densities and orientations is much larger, up to 11.5%. This spread is significantly larger than 1.1% predicted by simulation of the extracted layout. Finally, the D2D spread is large, from a typical to a fast simulation corner. The ROs with single isolated poly fingers exceed the fast corner and are excluded from the measurements.

Variations in stacked gates are less pronounced than those with single gates. Similarly, added poly stripes to maintain the uniform density reduce the variation effect as well. However the reduction in σ/µ of 0.3% is small, compared to a large reduction in average frequency of 11.5%.

Spatial correlation in variation is important to quantify, as it could be exploited in statistical timing analysis. A weak spatial correlation is observed in the measurements, stronger in the horizontal than in the vertical direction (Fig.4). One direction is along the slit of light and is subject to lens aberrations and curvature. The other is in the direction of scan, which is subject to the variation in scan speeds and light dosage. The layouts 6a/6b are rotated by 90°, and thus behave differently than the others in Fig 4, confirming this trend.

The variation in leakage currents exhibits the same trends as the RO frequency, but with larger relative values. WID maximum layout-to-layout shift in average $\log(I_{LEAK})$ is ~20% for single gates. Within-die within-layout σ/µ is 2-4%. Denser layout reduces leakage and tightens the spread. M1 coverage over poly reduces leakage current to half its value and reduces the σ/µ by 1%.

There is a strong positive correlation for $\log(I_{LEAK})$ vs frequency spread only for D2D variation (mean of centers of patch) and between configurations (Fig.6). For the same WID configuration, there is no visible correlation as given by a circular patch in the plot.

Parameter Extraction

Using the least squares method and the BSIM3 model, the variation in L and Tox can be de-embedded from the frequency (F) and leakage current ($I=\log(I_{Leak})$) measurements at varying Vdd (1.0, 1.4V), substrate bias (0V, -0.2V) and temperature (25°C and 60°C):

$$Y=\begin{bmatrix}F\\I\end{bmatrix} \quad , \quad X=\begin{bmatrix}L\\Tox\end{bmatrix} \quad , \quad M=\begin{bmatrix}\frac{\partial F}{\partial L} & \frac{\partial F}{\partial Tox}\\ \frac{\partial I}{\partial L} & \frac{\partial I}{\partial Tox}\end{bmatrix}$$

Fig.7 shows the de-embedded distribution of L and Tox yielding a conclusion that most of the variation can be attributed to changes in L.

Summary

Regular, layout reduces the systematic layout-dependent process variations, that are not captured by extraction. Since most of the variations are attributed to the channel length, using high and uniform poly density reduces the random variability, but at a large expense in average performance. Since the spatial correlation is weak, design with larger logic depths can reduce the overall variability. Adjusting the supply voltage and back bias can be used to effectively compensate for D2D variations.

Acknowledgements

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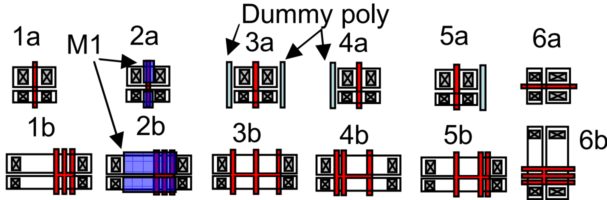
References

[1] J.W. Tschanz, et al, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," IEEE Journal of Solid-State Circuits, Nov. 2002.

[2] D.Boning et al, "Test Structures for Delay Variability" TAU 2002.

[3] M. Orshansky, *et al*. "Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits", IEEE Trans. CAD, May 2002



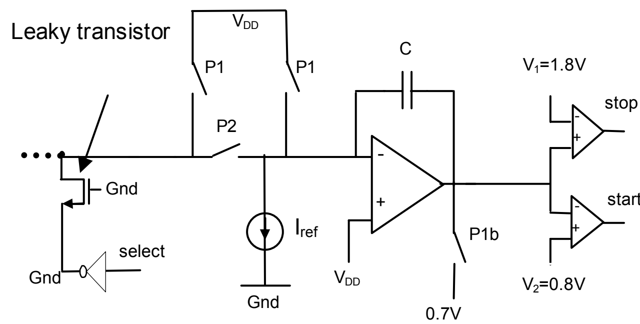


Fig.1 Layout configurations and die photo of the test-chip. Tile pitch is 62.5µm horizontal and 100µm vertical.

Fig.2 Single slope ADC for current measurement.

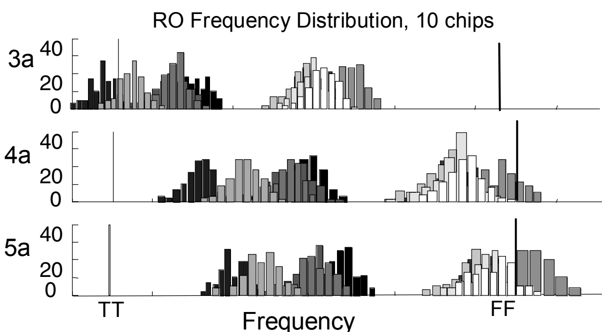


Fig.3 Frequency distribution for 'a' configurations. Vertical lines correspond to typical and fast corner simulation results.

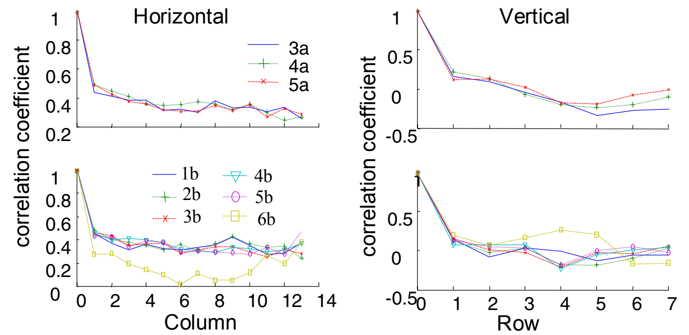


Fig.4 Plot of RO frequency spatial correlation coefficient between the 14 columns and between the 8 rows.

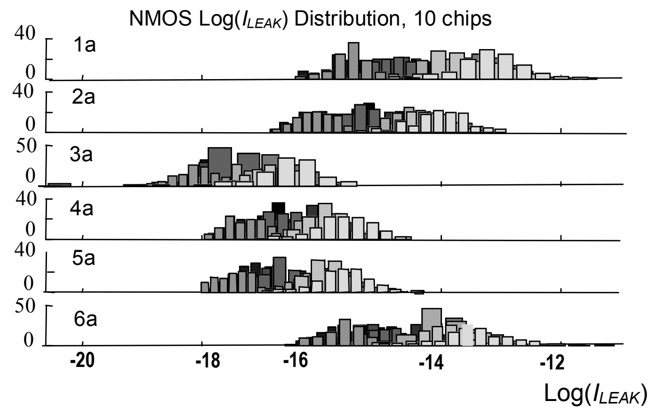


Fig.5 Plot of log(I_{leak}) distribution for 'a' configurations

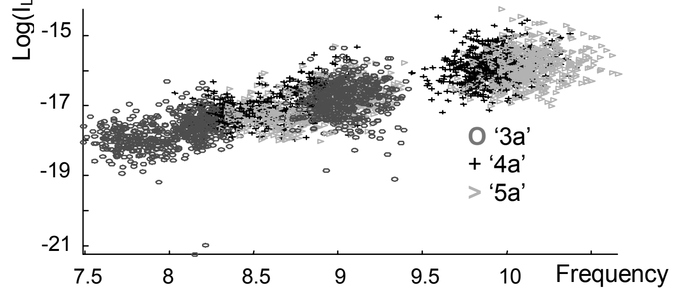


Fig.6 Scatter plot of log(I_{leak}) vs frequency.

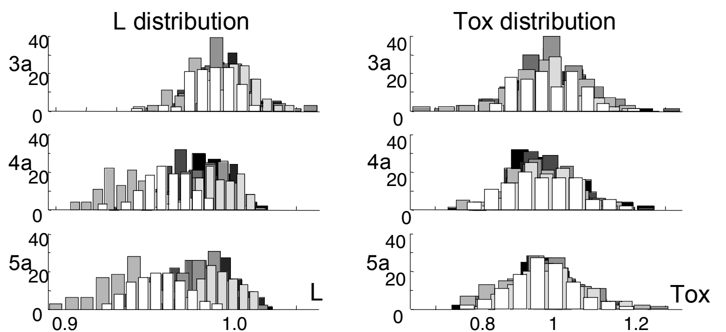


Fig.7 Distribution of normalized oxide thickness (Tox) and gate length (L) for 3 layouts and 8 chips.