Impact of Modern Electronic Equipment on the Assessment of Network Harmonic Impedance

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Abstract-- Network harmonic impedance forms the link between harmonic currents emitted by individual devices and the harmonic voltage levels in the grid. It is essential for the definition of current emission limits in order to ensure Electromagnetic Compatibility between all equipment connected to the grid. Among all electrical equipment in future smart grid electronic devices, like PV inverters, EV chargers or lamps with electronic ballast, will have a dominating share. This is expected to have a considerable impact on the network harmonic impedance characteristic.

The paper discusses the frequency-dependent input impedance of different types of modern electronic equipment and its potential impact on the network harmonic impedance. It is shown that the semiconductor switching results in a variation of the impedance within the fundamental cycle. This is not considered by the presently used assessment methods as they assume only passive network elements. Beside a method to measure these variations, several indices are introduced to quantify the level of its impact. The paper aims to provide some impulses for further discussions, particularly about the definition of network harmonic impedance in presence of electronic devices, the necessity to include these variations in realistic harmonic studies and if this has to be considered in the standardization.

Index Terms-- Electronic loads, Fast Fourier Transform, Frequency domain analysis, Harmonic impedance, Smart grid, Time domain analysis.

I. INTRODUCTION

THE network harmonic impedance is an important component for harmonic emission coordination (calculation of emission limits) in power systems. It is required to determine the level and spread of harmonic emission in the grid. Harmonic emission standards like [1] use the network harmonic impedance to calculate limits for current harmonics emitted by customer installations. Such assessment methods often simplify the network harmonic

impedance by extrapolating the short circuit impedance at the point of common coupling (PCC) [2]. Certainly this practice will neglect the influence of electronic devices, especially at higher frequencies and lead to conservative results. E.g. many electronic devices have grid side filter circuits which introduce additional capacitances and can significantly reduce the frequency of the first resonance [3].

"Network harmonic impedance" is a common notation, but suggests that the impedance is only considered at harmonic frequencies. In this paper a significantly higher frequency resolution is used and the notation "frequency-dependent network impedance" would be more precise term. For the reader's convenience this is shortly referred to as network impedance or impedance in the further text.

From theoretical point of view the network impedance is only defined if it consists exclusively of passive elements. However, many electronic devices consist of a rectifier circuit with a following DC link capacitor. During the recharging period this capacitor gets connected in parallel to the network, thus significantly influencing the network impedance as seen from the connection point. A simple diode bridge rectifier opens and closes one time every half cycle of the fundamental voltage, which is illustrated in Fig. 1. This changes the network impedance twice between two states and raises the question if the simplifying assumption of passive circuits is applicable anymore. The impact increases with increasing frequency as the impedance of the shunt capacitor decreases.
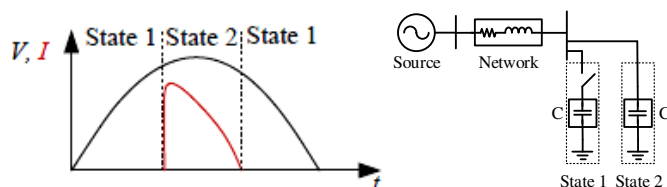

Fig. 1. Current waveform of a simple rectifier circuit and simplified equivalent circuit for both states

Duration and extent of the variation strongly depends on the circuit topology of the device, which can be generally classified into circuits without power factor correction (nPFC), with passive PFC (pPFC) or with active PFC (aPFC). The 'momentary' variation of network impedance can have negative impact e.g. on the proper functioning of Power Line Communication [4]. Sudden impedance changes can cause transients like zero-crossing oscillations [5].

Existing measurement methods for network impedance can be broadly divided into non-invasive methods and invasive methods [6]. *Non-invasive methods* use existing network

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elements to generate the excitation current, like switching of capacitor banks or transformers (e.g. [7]-[9]). This involves no additional setup thus keeping the total cost of the experiment low. However, this method is usually not preferred due to the limited injected frequency range, the very short duration, the highly unbalanced spectra with small magnitudes and an always existing, often varying background distortion. The *invasive methods* on the other hand provide a better accuracy and a controllable frequency range (e.g. [10]-[12]). They use an external setup to generate the excitation current and to carry out the measurements. Thus they provide better control of the generated disturbance magnitude and can be easily tailored for different system conditions and locations.

Virtually any measurement method determines the network impedance based on multiples of the fundamental voltage cycle. Therefore the change in impedance within a fundamental cycle due to semiconductor switching is not visible and questions arise, how these "averaged" measurement results have to be interpreted, how the variation of network impedance within a fundamental cycle can be determined and what impact it will have on EMC.

The study presented in this paper is focused on the measurement-based evaluation of the input impedance of nonlinear modern electronic devices as well as the simulation-based assessment of the impact of these nonlinear devices on the network harmonic impedance. Section II discusses the proposed analysis methods and suggests several indices to quantify the impact of electronic devices on network impedance. Section III provides a comprehensive, measurement-based overview about the input impedance characteristic of electronic devices with different circuit topologies. Finally in section IV the possible impact of multiple electronic devices connected to the network at a single point (e.g. house connection) is studied based on simulations. A summary of the important findings and future work items concludes the paper.

II. ANALYSIS METHODS

A. Primary algorithm (classical algorithm)

The diagonal elements of the impedance matrix (Z_{bus} matrix) of a power system network represent the equivalent impedance of the network as seen from a particular node or bus. These diagonal elements can be calculated for a particular frequency f by injecting a current i_f at the respective node and solving Ohm's law assuming Thevenin's equivalent for the remaining network.

The accuracy of this method is sensitive to existing background harmonics (cf. [8], [10]) and therefore most of the available measurement devices use the difference method as illustrated by Fig. 2. In the first step samples of voltage (v_{pre}) and current (i_{pre}) are taken before excitation (Fig. 2 (a) & (b)). As second step an excitation current (i_f) is injected and measurement of the resulting voltage (v_{post}) and current (i_{post}) are taken (Fig. 2 (c) & (d)). In the third step the difference of pre- and post-states are calculated for voltage and current in order to remove any constant background harmonics present
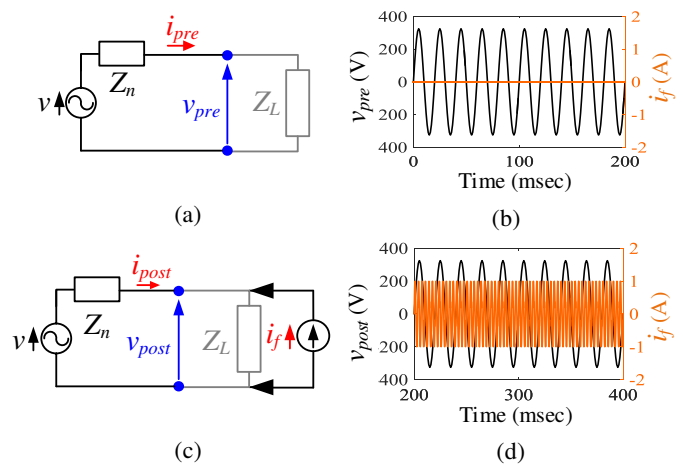

Fig. 2. Pre-excitation state: (a) network schema and (b) waveforms of injected current (i_f) and measured voltage (v_{pre}), Post-excitation state: (c) network schema and (d) waveforms of injected current (500 Hz) and measured voltage (v_{post})

in the system voltage and current. Finally the network impedance (Z_f) at frequency f can be calculated using (1).

$$Z_f = \frac{v_{post} - v_{pre}}{i_{post} - i_{pre}} = \frac{v_{diff}}{i_{diff}} \qquad (1)$$

In case of time-varying background harmonics the accuracy of the difference method can significantly reduce. Therefore it is common to inject current at frequencies that are normally not present in the grid (e.g. interharmonics). If the above steps are repeated over a range of frequencies, the network impedance curve is obtained. This is commonly known as frequency sweep analysis.

The described method can be applied either in time-domain or in frequency-domain. In *time-domain* the RMS values of v_{diff} and i_{diff} are used in (1) to get the impedance magnitude. The phase difference between v_{diff} and i_{diff} waveforms provides the impedance angle. However, this method is not applicable for real networks as RMS values of v_{diff} and i_{diff} waveforms will always include unwanted background harmonics. For *frequency-domain* analysis Fast Fourier Transform (FFT) is applied to v_{diff} and i_{diff} waveforms and the complex values for the required frequency component (f) are used in (1) to calculate magnitude and angle of the impedance. Frequency-domain provides more robust and accurate results, as the respective frequency component can be better identified even when signals contain multiple frequencies. This method is generally preferred for measurement based impedance calculation [6], [10]. Therefore only the frequency-domain analysis is applied for further analysis in this paper.

The classical algorithm, which is referred to as primary algorithm, calculates the network impedance based on the time period of the fundamental voltage cycle i.e. 20 milliseconds in 50 Hz networks. The result is a single "average" impedance value per cycle for each frequency. This method is further referred to as voltage cycle method (VC method). All commercially available measurement devices that are known to the authors use this method.

B. Secondary algorithm

The limitation of the VC method is that the change in network impedance due to semiconductor switching is not explicitly visible. So the influence of electronic devices on the measured impedance cannot be quantified.

To address this issue, a new analysis technique is proposed, termed as 'secondary algorithm' which uses the time period of the injected current cycle (i.e. T milliseconds if current of frequency $f = 1/T$ Hz is injected) to calculate the network impedance at $1/T$ Hz. This reveals a possible time variation of network impedance within a VC window, as illustrated by Fig. 3. The result of this algorithm is a "momentary" impedance characteristic within a single fundamental cycle. As this method is based on the cycle of the injected current, it is referred to as current cycle method (CC method). The number of impedance values per voltage cycle corresponds to the ratio of injected frequency and fundamental frequency. The higher the frequency of the injected signal, the higher is the resolution of the "momentary" impedance characteristic, thereby providing a smoother and more accurate representation of the impedance variation.
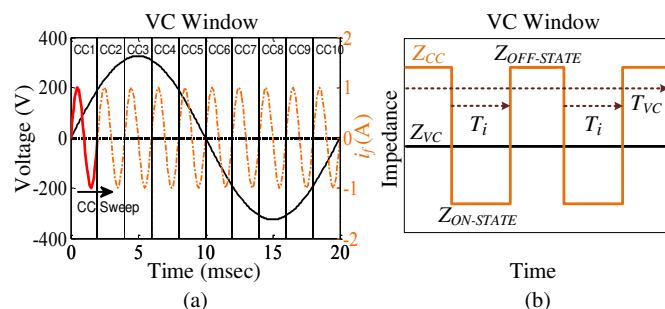

Fig. 3. (a) Injected current cycle (CC) swept through one fundamental voltage cycle (VC) (b) Time variation of impedance within one VC window

As an example, Fig. 3(a) presents a VC window with injected current of 500 Hz (10 current cycles within one fundamental voltage cycle). To obtain the 'momentary' impedance, each cycle of the injected current is used to calculate 10 individual impedance values within the VC window. Fig. 3(b) shows the 'momentary' impedance (Z_{CC}) exemplarily for a simple rectifier circuit without PFC. It can be seen that Z_{CC} changes its state four times. The network attains minimum impedance ($Z_{ON\text{-}STATE}$) during the ON-state of the rectifier bridge. When the bridge is closed (OFF-state), the impedance is given by $Z_{OFF\text{-}STATE}$. The "average" impedance calculated according to VC method (Z_{VC}) cannot identify this variation at all. The phase angle of the impedances from VC and CC methods are denoted by θ_{VC} and θ_{CC} respectively.

ON/OFF-state is used to explain and characterize the operation of an individual device. In case of multiple devices of different rating and circuit topology, a multitude of different ON/OFF states will overlay asynchronously. In these cases the minimum/maximum network impedance within a fundamental voltage cycle should be used for $Z_{ON\text{-}STATE}$/$Z_{OFF\text{-}STATE}$.

C. Assessment indices

To quantify the influence of electronic devices and to assess the impact of different circuit topologies on the measured impedance, the indices in Table I are proposed.

TABLE I
Indices for quantification of power electronic device influence on measured impedance

Indices	Expression	Remark
$k_1(f)$	$\dfrac{Z(f)_{ON\text{-}STATE}}{Z(f)_{VC}}$	Per unit ratio between ON-state impedance and "average" impedance
$k_2(f)$	$\dfrac{\sum_i T_i}{T_{VC}}$	Total duration of ON-state impedance within a VC window
$k_3(f)$	$\dfrac{Z(f)_{ON\text{-}STATE}}{Z(f)_{OFF\text{-}STATE}}$	Per unit ratio of impedance variation between ON-state and OFF-state

Index $k_1(f)$ presents the ratio of ON-state impedance resulting from CC method to the 'average' impedance obtained by VC method. This provides a per unit ratio between the two methods. A lower value of $k_1(f)$ indicates that $Z_{ON\text{-}STATE}$ is significantly different from Z_{VC} and the impact of electronic devices is more significant. Index $k_2(f)$ quantifies the total duration for which the ON-state impedance is present within the VC window. ΣT_i corresponds to the sum of the times T_i for $Z_{ON\text{-}STATE} \leq Z_{VC}$. Index $k_3(f)$ provides an idea about the level of impedance variation between ON- and OFF-state and is only useful if the impedance $Z_{OFF\text{-}STATE}$ is not infinite. The application of the indices is illustrated in the next sections. Further indices, e.g. to quantify the severity of the impedance variation are under development.

The value range of all indices is between zero and one. Index values close to one mean that the impedance behavior is close to that of networks containing only passive elements and the classical "average" method (primary algorithm) is sufficient for analysis. With decreasing index values the impact of active switching on the impedance increases and should not be neglected anymore.

As the value of "average" impedance Z_{VC} in relation to the ON-state impedance indirectly includes information about the "duty cycle" of the impedance variation, the index $k_1(f)$ is sufficient for the assessment of individual equipment. The index $k_3(f)$ does not provide meaningful results in absence of a network impedance, e.g. if the input impedance of a device is obtained (either by simulation or measurement) without any source impedance.

III. INPUT IMPEDANCE CHARACTERISTIC OF EQUIPMENT

A. Classification of circuit topologies

As modern electronic devices have a large diversity in their circuit topologies, a large variation of their "momentary" impedance characteristic within the fundamental voltage cycle is expected. For example, the input impedance of a simple rectifier circuit will be almost infinite if the rectifier bridge is closed (OFF-state). However, the presence of an alternative conducting path during the OFF-state e.g. by an input filter at the front end of rectifier can reduce the impedance variation significantly.

In order to select a representative sample of electronic devices for the measurements, a general classification of basic circuit topologies is used [13]:

TABLE II
Overview of measured devices, respective indices $k_1(f)$ and $k_2(f)$ and average impedance/phase angle

General topology	Input filter	Equipment	$k_1(f)$	$k_2(f)$ (informative)	$|Z_{VC}|$ (Ω)		θ_{VC} (degree)	
					1 kHz	2.3 kHz	1 kHz	2.3 kHz
nPFC	-	CFL 20W	0.30	0.32	160	80	-65	-50
nPFC	Capacitive	Dimmable LED 7.2W	0.44	0.57	400	380	-35	5
pPFC	Capacitive	PC SMPS 420W at 12% S_r	0.53	0.41	220	70	-80	-75
pPFC	-	LED 3W	0.55	0.55	750	260	-85	-83
aPFC	Capacitive	PC SMPS 400W at 7% S_r	0.65	0.60	100	40	-75	-60
aPFC	Capacitive	PC SMPS 400W at 45% S_r	0.75	0.88	70	28	-69	-51
aPFC	-	CFL 30W	0.84	0.82	500	240	-70	-80
aPFC	LCL	PV inverter 3kW at 100% S_r	1	1	5	4	-60	-88

- No power factor correction (nPFC)
- Passive power factor correction (pPFC)
  (either with series inductance or capacitance)
- Active power factor correction (aPFC)
  (including other self-commutating technologies)

Furthermore the existence of an additional input filter is distinguished.

The most severe level of impedance variation is expected for nPFC-circuits e.g. in low power compact fluorescent lamps (CFLs) and most light emitting diode lamps (LED). Circuits with pPFC as well as possibly existing input filters are commonly used in devices with higher power ratings e.g. switch mode power supplies (SMPS) for computers. It provides an improvement of impedance variation by reducing the difference between ON- and OFF-state values. Circuits with aPFC tend to produce relatively constant input impedance within the fundamental cycle as their switching frequencies are usually much higher than the frequency range considered in this paper. An aPFC circuit is used for devices with stricter emission requirements like higher power lighting equipment as well as for improvement of energy-efficiency, e.g. in computer power supplies.

Based on the qualitative considerations above, a set of electronic devices has been selected for the detailed measurement-based analysis of their input impedance characteristic (Table II).

B. Measurement framework

The measurement setup consists of a linear power amplifier with a maximum output current of 10 A and a bandwidth better than 5 kHz. A shunt 0.1 Ω has been used for current measurements. Voltage and current has been adapted to the input ranges of the Analog-Digital Converter by signal conditioner modules, which also include the Anti-Aliasing-Filters. Finally the signals are sampled at 100 kHz/s. No additional impedance has been introduced between the source and the device. An automatic frequency sweep in the low frequency range between 50 Hz and 2300 Hz in steps of 5 Hz has been carried out.

The typically used current injection is not possible in absence of network impedance, as in case of very high input impedances this might result in very high voltages. Consequently for these measurements a supply voltage containing the fundamental component and the swept component with variable frequency has been applied. In order to obtain an interpretable time characteristic of the "momentary" impedance, the lowest frequency for the

analysis is limited to 800 Hz. The upper limit of 2300 Hz is determined by the bandwidth of the power amplifier.

Finally for all devices "momentary" and "average" impedance has been determined.

C. Measurement results

Selected results for "momentary" impedance and "average" impedance are summarized in Table II. The indices $k_1(f)$ and $k_2(f)$ have been calculated for the considered frequency range. Index $k_2(f)$ is only informative as the assessment of $k_1(f)$ is sufficient for equipment characterization. As both indices remain almost constant over the frequency range, only a single value is provided in the table. The "average" impedance values have been calculated for 1 kHz and 2.3 kHz.

Spectrograms of magnitude and phase angle of "momentary" impedance as well as the respective current and voltage waveforms for sinusoidal supply voltage are shown in Fig. 4 for one device per topology class. While time and frequency are presented on x- and y-axis, magnitude/phase angle is quantified by a color map. It's scaling has intentionally been chosen different for the individual devices in order to utilize the range of colors as best as possible. "Average" impedance characteristic obtained by the VC method is presented for the same devices in Fig. 5.

The following subsections discuss the results for the different circuit topologies in more detail.

1) Equipment without power factor correction (nPFC)

A CFL 20W and a dimmable LED 7W have been analyzed. The "momentary" impedance characteristic of the CFL 20W shows a large variation of magnitude and phase angle between ON- and OFF-state (cf. to Fig. 4 left). The input impedance during the ON-state is mainly determined by the DC-link capacitor of the rectifier while during the OFF-state, when the current is zero, impedance can be assumed to be infinite. As a result the spectrogram of momentary impedance of CFL 20W contains only two narrow stripes with finite values of impedance magnitude and phase angle, which correspond to the interval of current flow. The low values for $k_1(f)$ confirm the significant impedance variations. As the LED 7W includes an additional filter circuit, $k_1(f)$ is slightly higher. The "average" impedance values show a distinctive capacitive behavior for the CFL 20W, but a behavior closer to ohmic for the LED 7W.

2) Equipment with passive power factor correction (pPFC)

A LED 3W and a PC SMPS 420W with 12% load have been analyzed. The additional circuit element for the
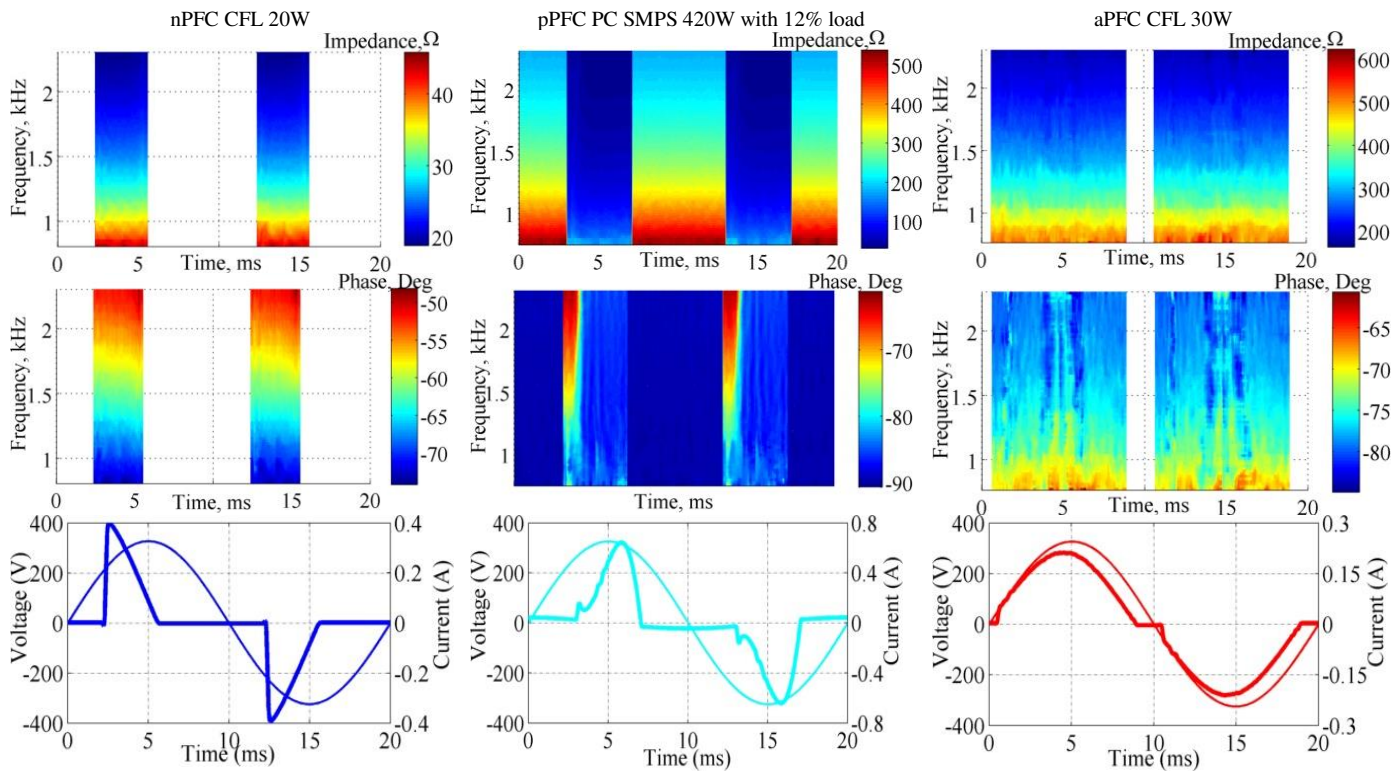
Fig. 4. Time-frequency spectrograms of momentary impedance and current waveforms for selected devices

realization of pPFC (e.g. an inductance or a capacitance) improves the impedance characteristics, which is also reflected by the higher values for $k_1(f)$ compared with those for the nPFC devices. The conduction time of the rectifier bridge is longer, which is also confirmed by the index $k_2(f)$. Due to the input filter the momentary impedance for PC SMPS 420W with 12% load (Fig. 4 middle) shows capacitive characteristic for both OFF-state and ON-state. The abrupt phase increase at the beginning of conducting interval (cf. Fig. 4 middle) is caused by the resonant pPFC filter. The "average" impedance characteristic shows for both devices a clearly capacitive behavior.

Fig. 5. Average impedance characteristics for considered equipment

3) Equipment with active power factor correction (aPFC)

A CFL 30W, a PC SMPS 400W at two load states and a 3 kW PV inverter are analyzed. As expected, these devices have values for $k_1(f)$ close to one which means almost constant impedance characteristic. It should be noted that this

conclusion only holds, if the analyzed frequency range is well below the switching frequency of the aPFC circuit. However, under partial loading impedance characteristics might deteriorate, as it can be easily seen from the difference in $k_1(f)$ for the PC SMPS 400W between 45% and 7% load at the DC-side. This consequently means that the input impedance can also depend on the operating state of a device. The "momentary" impedance characteristic of the CFL 30W (Fig. 4 right) has long conducting intervals of constant magnitude and phase angle. The short non-conducting intervals (infinite impedance) have also been observed for other equipment as this specific feature can further increase the energy efficiency of a device. The "average" impedances in Table II show also a clearly capacitive character for all measured aPFC devices.
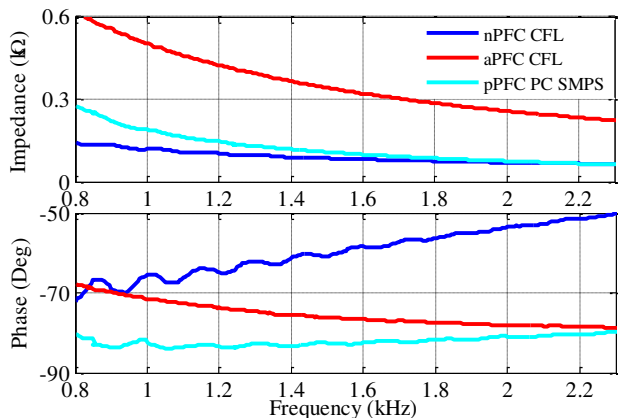
D. Summary

The assessment of input impedance characteristics of electronic equipment was done based on its level of nonlinearity, i.e. the type of PFC circuit used. The results show a reduction of impedance variation within fundamental cycle and an increase of the index $k_1(f)$ for increasing power factor performance of the circuit (nPFC → pPFC → aPFC). This is also directly linked to the level of current harmonic distortion THDi, which is the lowest for aPFC devices.

It has been shown that the index $k_1(f)$ is almost constant in the frequency range between 1 kHz and 2.3kHz and is suitable to distinguish between devices with different level of impact on the "momentary" impedance variation. Therefore, it could be a useful indicator to assess the dominating equipment topology in a LV network. Based on these initial measurements the following indicative value ranges are suggested:

- $k_1(f) < 0.5$:
  higher nonlinear characteristic (nPFC)
- $0.5 \leq k_1(f) < 0.75$:
  moderate nonlinear characteristic (pPFC)
- $k_1(f) > 0.75$:
  lower nonlinear characteristic (aPFC)

The phase angle of average impedance (θ_{VC}) in Table II shows that all considered devices feature predominantly capacitive behavior. This can have a considerable impact on network resonances, particularly in residential low voltage (LV) networks. E.g. in an urban LV network with 400 household customers a first resonance as low as 500 Hz has been identified by measurements [14].

IV. IMPACT ON NETWORK IMPEDANCE

The devices studied in the previous section are now analyzed by connecting multiple of them in parallel to a representative LV network in order to simulate their impact on the "momentary" impedance under a more realistic grid condition. Three cases with different sets of devices have been analyzed by simulation.

A. Simulation Environment

The basic schema of the simulation setup is shown in Fig. 6 and has been implemented in Simulink. It consists of four subsystems: source, reference network, load, harmonic injection and measurement.

The reference network is based on the impedance model proposed in the informative annex of IEC 61000-4-7 Ed.2. This model is designed to represent the impedance characteristic of a LV network in the frequency range of 2 kHz to 9 kHz. The reference network comprises of only linear, passive elements arranged as T-section. Load subsystem includes different models introduced in Section III. These models are designed based on electronic devices available in the market (e.g. [15-19]) and resulted in a comprehensive library of circuit-based device models for time-domain simulations ([13], [20]). Harmonic injection and measurement subsystem carries out pre-injection state measurements for 10 fundamental cycles, injects current i_f and carries out post-excitation state measurements for another 10 fundamental cycles. These measurements are processed according to the

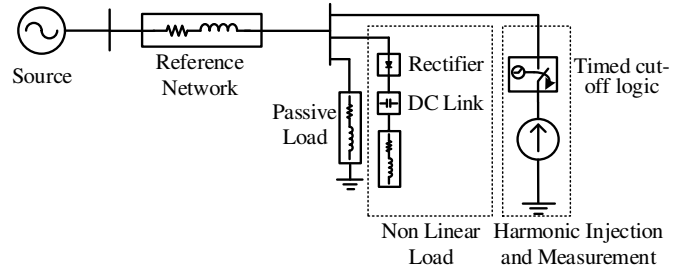algorithms presented in section II in order to calculate the network impedance Z_f.

Fig. 6 Schematic for simulation setup

B. Selection of excitation current (i_f) magnitude

Experiences by the authors have shown that the magnitude of injected current i_f as well as the location of the measurement can have significant impact on the measured impedance. The level of the impact depends to a certain extent on the circuit topology of the devices. This issue is still investigated, but a relatively high impact has been identified for the simple device without PFC, as discussed below.

A single nPFC CFL of 21W is used as load to investigate this issue by comparing measured impedances for different magnitudes of the injected current i_f (0.1 A and 1 A). These are later on referred to as low injection and high injection. The results for the "momentary" impedance according to the CC method are presented for low injection in Fig. 7 and high injection in Fig. 8. Each plot presents three frequencies. The time variation of network impedance increases with increasing frequency. The ON-state impedance is found to have significantly different characteristic for low and high injection. This difference can be explained with the help of Fig. 9. With low injection i_f overlaps the load current without any current chopping. In case of high injection the load current gets increasingly chopped off as i_f tries to change its direction, which consequently causes the bridge to close very shortly. A similar characteristic can be observed in the negative half cycle as well. This effect results in different values for the calculated voltage difference ($v_{post} - v_{pre}$) and the current difference ($i_{post} - i_{pre}$) and hence in the calculated impedance for the two injection levels.
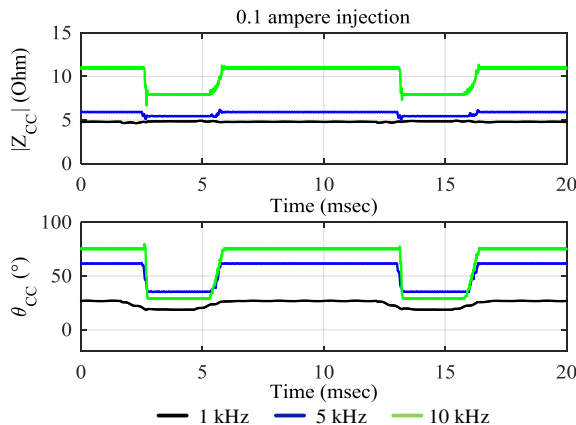

Fig. 7. Network harmonic impedance based on CC method with 1 nPFC CFL load and low injection current
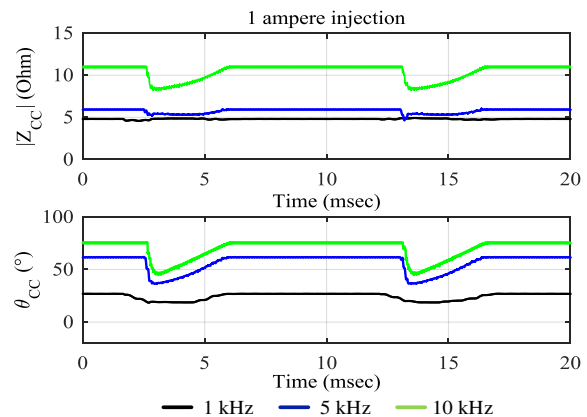

Fig. 8. Network harmonic impedance based on CC method with 1 nPFC CFL load and increased injection current
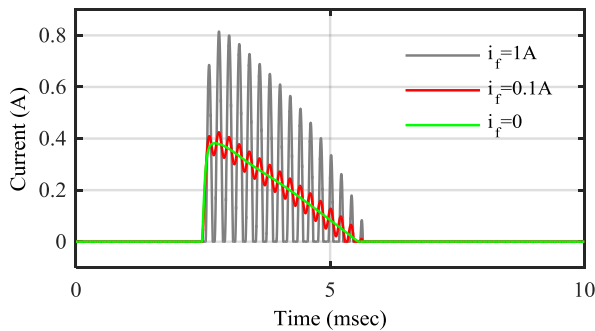
Fig. 9. Load current (no PFC CFL) with increase in magnitude of i_f

Fig. 11. Current waveform for three individual CFLs and its sum

From Fig. 8 and Fig. 9 it is evident that the injection current should be as low as possible. However, a very low magnitude of i_f can result in an increasing influence of background noise. In contrast, a high magnitude can lead to unwanted impact on the load current (e.g. chopping). In both cases the calculated impedance will be erroneous. Hence, it is essential to adapt the injection magnitude to the measurement location in order to obtain accurate and realistic impedance measurements.

As background noise is not an issue in the simulation, the low injection magnitude has been used for all case studies.

C. Case studies

The primary objective is to assess the impact of individual device topologies (e.g. nPFC, aPFC) as well as a combination of different device topologies on the network impedance. For each case the difference between VC method and CC method is discussed as well.

1) Three nPFC CFL devices

Two nPFC CFLs of 20 W and one nPFC CFL of 21 W are used for this case. Though these lamps have similar circuit topology and nearly similar rating, the nature of the current drawn by them is not exactly the same (Fig. 11).

This variability in current characteristics is also reflected in the measured impedance, shown in Fig. 10. The slight differences in firing angle result in a short impedance step. Comparison of Fig. 7 and Fig. 10 shows that increase in number of CFLs leads to greater difference between $Z_{ON\text{-}STATE}$ and $Z_{OFF\text{-}STATE}$. The phase angle is also found to shift towards a
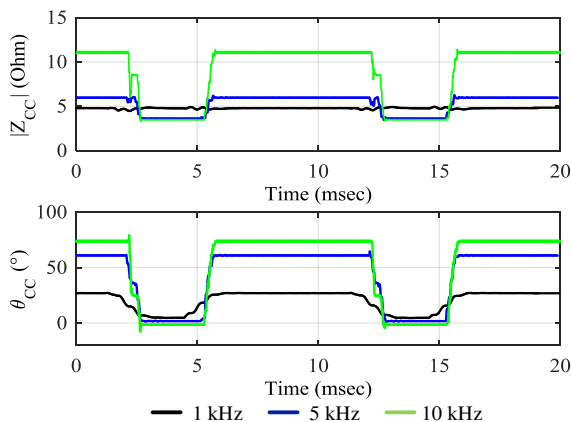
more capacitive behavior compared to a single CFL. Thus number and composition of nonlinear loads will have a considerable impact on the network impedance.

Table III presents the "average" impedance and the three indices derived from "momentary" impedance for three different frequencies. $k_1(f)$ and $k_3(f)$ values reduce significantly with increase in frequency while the duration of ON-state ($k_2(f)$) remains almost constant.

TABLE III
"Average" impedance and assessment indices for 3 nPFC CFL

Frequency (kHz)	0.1 amp injection				
	$|Z_{VC}|$ (Ohm)	θ_{VC} (degree)	$k_1(f)$	$k_2(f)$	$k_3(f)$
1	4.76	20.38	1.00	1.00	1.00
5	5.19	49.13	0.70	0.35	0.60
10	8.54	64.70	0.41	0.36	0.31

2) Two aPFC CFL devices

Two aPFC CFLs of 30W are used for this case. Due to its complexity the circuits for aPFC CFLs can considerably differ. However, due to the high switching frequencies the impact on the network impedance for frequencies below 10 kHz is very similar. The "momentary" impedance for the two CFLs is presented in Fig. 12. It shows virtually no variation and is similar to an impedance characteristic with passive elements, as the high frequency switching is still invisible at the considered frequencies. The impedances calculated by VC method and CC method are similar and all calculated indices will have values equaling to one. Therefore the table is not shown.

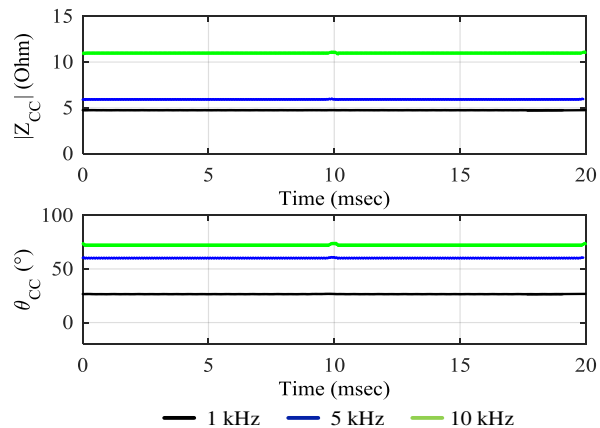Fig. 10. "Momentary" impedance with three nPFC CFLs

Fig. 12. "Momentary" impedance with two aPFC CFLs

Subsequently, the classical VC method is sufficient if a dominating share of aPFC devices is connected to a particular site. As devices with aPFC circuits are usually costlier than comparable nPFC or pPFC devices, their share in the network is expected to be low at present, but increasing in the future.

3) Mixed load

This case study considers a more realistic household by combining the following devices with different topologies: one passive load (100 Ω resistance with associated inductance), two aPFC CFL (2×30 W), three nPFC CLFs (2×20 W + 1×21 W), one dimmable LED (7.2 W) and one pPFC SMPS PC (420 W). Fig. 13 presents the "momentary" impedance of individual devices at 10 kHz while Fig. 14 presents the "momentary" impedance of the aggregate. Impedance plots for passive load and aPFC CFL are not included in Fig. 13 as both exhibits constant impedance over voltage cycle.
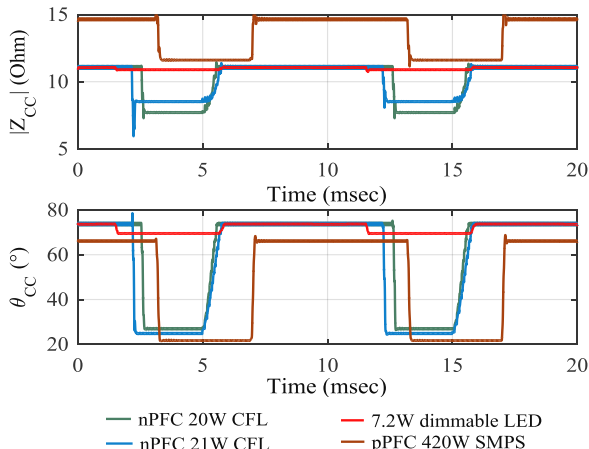

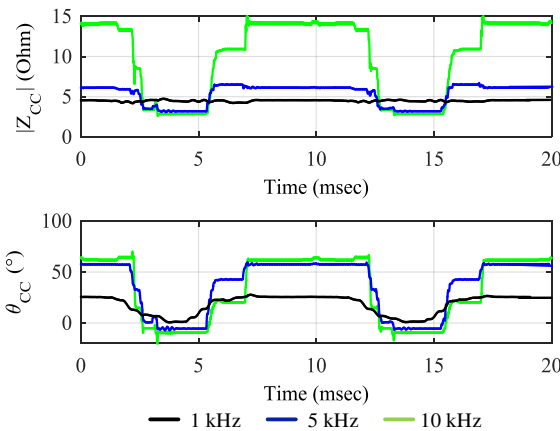Fig.13. "Momentary" impedance for different devices at 10 kHz

Fig. 14. "Momentary" impedance for aggregate of different devices

As shown in Fig. 13, the firing angle of the rectifier valves and the duration of ON-state depends on the circuit topology (nPFC, aPFC and pPFC). The 'momentary' behavior of network impedance is therefore expected to be irregular, as confirmed by Fig. 14. Among the different categories of loads analyzed in this paper, nPFC CFL and pPFC SMPS are found to have dominant effect on the variation of magnitude and phase angle of the network impedance. The calculated indices

and the "average" impedance values for the aggregate of different devices are given in Table IV.

TABLE IV
"Average" impedance and assessment indices for device aggregate

Frequency (kHz)	0.1 amp injection				
	$|Z_{VC}|$ (Ohm)	θ_{VC} (degree)	$k_1(f)$	$k_2(f)$	$k_3(f)$
1	4.63	18.53	1.00	1.00	1.00
5	5.05	43.63	0.63	0.36	0.52
10	9.58	48.88	0.30	0.56	0.20

Comparing the index values with Table III it can be concluded that the difference between $Z_{ON\text{-}STATE}$ and $Z_{OFF\text{-}STATE}$ increases as the number of nonlinear devices increase. The high impact of the nPFC and pPFC devices is still dominating even in the typical situation of mixed equipment. The impedance at 1 kHz is almost constant due to the interaction with the reference impedance. For equipment with similar topology the ON-state duration, represented by $k_2(f)$, is similar for 5 kHz and 10 kHz while it varies significantly for the device aggregate.

V. Conclusion

This paper provides a methodology for visualization of impedance variation within the fundamental voltage cycle due to semiconductor switching. Three indices are proposed for the quantification of this variation. Measurements of input impedance for seven devices have shown that the circuit topology has significant impact on the character of the input impedance variation. Especially, for the simple equipment without power factor correction the impact is high. An index is used to quantify and classify the impedance variation and indicative value ranges provided for the major circuit topologies. As most of the devices have capacitive behavior, LV grids must not be considered per se as resonance-free anymore. The simulation of the influence of multiple electronic devices on the network impedance has shown that at 10 kHz even in case of a mix of different circuit topologies the impedance around the voltage maximum/minimum can be up to three times lower than around the voltage zero-crossing.

A major aim of the paper is to intensify the discussion about the definition of frequency-dependent network impedance in presence of electronic devices, particularly for micro grids in islanded mode. The time characteristic of the "momentary" impedance can also be a useful tool for troubleshooting and based on the proposed indices the general character of the equipment mix in a network can be obtained.

Future work includes the development of a mobile measurement device, further measurements of electronic devices as well as the improvement and extension of the index set. Systematic measurements in real LV networks are used to validate the simulation results and to improve the algorithms in terms of robustness and accuracy. Based on comprehensive knowledge about the individual equipment input impedance characteristic this work can contribute to the modelling of network impedance in the presence of bulk electronic devices.

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