Impact of Process Induced Stresses and Chip-Packaging Interaction on Reliability of Air-gap Interconnects

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Abstract

The mechanical stability of air-gap interconnect structures during thermal processing and under chip packaging interaction (CPI) were investigated using 3D multilevel finite element analysis (FEA) models. Low k cap delamination from the Cu barrier during thermal processing, channel cracking of the bridging cap and dielectric overlayers, and interface delamination under packaging were identified as the main concerns of mechanical stability and reliability for air-gap implementation. Simulation results revealed that the delamination driving force depends very much on the gap width to cap thickness ratio, the channel cracking issue in the dielectric overlayers can be managed in the presence of constraints from adjacent Cu wires, and the introduction of air-gaps significantly increases the interfacial delamination probability under the outermost solder bumps.

Introduction

Implementation of air-gaps in the trench dielectric levels has been demonstrated as a potential effective solution for further reduction of the capacitance coupling in the Cu/low k interconnects [1-4]. But how to fabricate air-gap interconnect structures with satisfactory reliability for an acceptable cost remains a challenging problem so far. Among the reliability issues, mechanical stability of the air-gap interconnects has always been a serious concern. Collapse of bridging low k cap (or hard mask) over wide gaps has been observed during thermal decomposition of gap forming materials [2,4]. It was also pointed out that keyhole shaped gaps [5] in etchback and non-conformal refill schemes may cause potential crack initiation. And as packaging assembly exerts additional stresses to the fragile low k structures, chip-packaging interaction (CPI) in air-gap structure is a potential serious reliability problem but has yet to be investigated.

In this paper, we analyze the structural stability of air-gap interconnect structures during thermal processing and subsequent packaging assembly using 3D multilevel finite element analysis (FEA) models. Our investigation focuses first on the effect of process induced stresses on the collapse of the low k cap during sacrificial material removal and channel cracking of the bridging ILD overlayer. Then the study is extended to the effect of chip-packaging interaction on air-gap interconnect structures.

Structural Stability of Air-Gap Interconnects

Effect of Process Induced Stress

The structural stability was first investigated by examining the effect of air-gap implementation on process induced stresses. Finite element models were developed to simulate process induced stresses in an air-gap interconnect containing five metal levels with a M1 half pitch of 65nm as shown in Fig. 1. FSG were used as interlevel dielectrics (ILD) in the first two levels and level 5. Air-gaps with SICOH low k caps were implemented in levels 3 and 4. A total of 32 process steps were used to simulate the process flow of Cu damascene structures, including depositions of ILD dielectrics and SiCN cap layers at 400°C and Ta/TaN barriers, electroplating of Cu at 25°C followed by annealing. Table I lists the material properties used in the simulations.

Table I. Thermomechanical properties

	Elastic Modulus (GPa)	Poisson's Ratio	CTE (ppm/C)
Si	130.2	0.28	2.3
Cu	104.2	0.35	17.0
Ta	185	0.34	6.5
SiCN	440	0.17	4.5
FSG	51	0.25	3
SiCOH	9.5	0.3	20
TEOS	72	0.2	1.4

The results in Fig. 2 show that the stress in the Cu lines of the M3 and M4 levels is slightly relaxed due to the implementation of the air gaps. Changing the elastic modulus of the low k cap from 8.0 GPa to 12.0 GPa has a negligible effect on the stress in the Cu line. To study the scaling effect, the half-pitch was reduced from 65 nm to 32 nm and 22 nm with 80% air gaps at the M3 and M4 levels. The stress in the Cu lines was found to only vary slightly. These results on Cu stress indicate no intrinsic impact on the Cu reliability by the introduction of airgaps in the interconnect structures.

To assess the effect of process induced stresses on structural stability, we calculated the crack driving force for delamination of the low k cap from the barrier, which is known to be prone to fracture. [4] For this study, a simplified 3D air gap structure (Fig. 3a) was used and process induced stresses were calculated following the process flow used for the five-level interconnect model. An interfacial crack was introduced between the low k cap and one of the Cu Ta/TaN barrier layers, and the virtual crack closure technique (VCCT) [6] was employed to calculate the energy release rate (ERR) for crack growth. Figure 3b shows the ERR obtained as a function of the crack length. Using two different low k ILDs gives indistinguishable ERRs, suggesting that the ILD material plays an insignificant role in controlling the delamination of the low k cap. On the other hand, the ERR increases dramatically as the width of the air gap increases. As shown in Fig. 4, the ERR increases by an order of magnitude as the air gap width increases from 0.2 μm to 2 μm. This can result in debonding at the cap/barrier interface and collapse of the low k cap over wide air gaps. Fig.4 also shows that the ERRs increase as the elastic modulus of the low k material increases. This is to be expected as the ERR roughly

scales with the elastic modulus under the condition of a constant thermal strain. Overall, these results indicate that the implementation of air-gaps has a negligible effect on the process induced stresses, but with a sizable increase in the air-gap width, the ERR can significantly increase to impact the structural stability. These results agree well with Ref. [4].

Effect of external load

Here we included a uniformly distrubuted load pulling the low k cap toward the airgap, representing a possible force due to the removal of the sacrificial layer for fabrication of the airgap. Fig. 5 shows that the ERR increases as the intensity of the distributed load increases but the rate of increase depends on the air gap width. For a gap width of 1.5 to 2 μm, the ERR can increase 2 to 3 times thus significantly increasing the reliability concern.

Cracking of low k overlayer

The structural stability of air-gap structure was further investigated by considering the effect due to a subsequent step when a low k overlayer is deposited on top of the air gap structure (Fig.6). This layer may fail by channel cracking which can occur due to the lack of elastic constraint after airgap formation underneath. The VCCT method was again employed to calculate the ERR of a crack introduced in the low k overlayer. Fig.7a shows that the ERR for crack growth in the overlayer increases with an increase in the air gap width. This is consistent with what is expected to happen due to reduced constraints from the underlying layers [6].

However, increasing airgap volume percentage (from 50% to 80%), reducing the modulus of the via level dielectric (from FSG to SICOH) and varying the thickness of the SiCN passivation layer (5/10/20 nm), did not result in much difference in the calculated ERR results (Fig. 7a and 7b), and the ERR values are still manageable compared with typical cohesive strength of ULK's (G_c>5GPa). This can be attributed to the constraints from the adjacent Cu wires.

Together with the delamination results, we conclude that the air gap width is the most critical design parameter for reliability considerations, both in terms of low k cap delamination and overlayer cracking for the air gap structures.

Impact of Chip-Packaging Interaction

Finally, the mechanical reliability of the air-gap structure was investigated by examining the impact of chip-packaging interaction (CPI). After completing the fabrication of the air-gap interconnects, the silicon die is incorporated into a plastic flip-chip package where the interconnect structure as a whole is subjected to additional stresses coming from packaging processes. The process with the highest thermal load is the die attach step before underfilling the package. The CPI effect of the die attach step for air-gap structures was investigated for Pb-free solders with a reflow temperature of 250^{o}C. The substrate in the package was organic and with a die size of 8x8 mm^2. A 3D finite element model was used based on the multilevel sub-modeling technique for the CPI study and the VCCT method was used to calculate the crack driving force ERR at relevant interfaces under the outermost solder ball [7,8]. For this study, we used a 4-level 3D interconnect structure which provided a realistic wiring structure to analyze the effect due to implementation of the air-gap structure. To simulate the hierarchical structure, the pitch and line dimensions in the first two metal layers (M1 and M2) are set corresponding to a line width of 100nm, which is doubled in the third layer (M3), and doubled again in the fourth layer (M4). ERRs were calculated for horizontal cracks placed at each metal level at the interface between the etch stop/passivation (ESL) and the low k dielectric or the air-gap, which is known to be most prone to delamination. Each crack has a width of 0.1 μm and a length of 2 μm extending in the multiple wiring directions as shown in Fig.8a.

As a base line for comparison, results of the ERRs of the interfacial cracks in a model with full low k ILD in M1, M2 and M3 and SiO_2 in M4 are summarized in Fig.8b. The ERR is highest for the M3 interface as a result of the elastic mismatch between SiO_2 and the low k layer. The effect of air-gap implementation was first examined for an across level full air-gap structure as shown in Fig.9 where air-gaps are used to replace all the intermetal dielectrics (IMD) in the M3 level. This led to a significant increase of about 5x in the ERR for crack 3 in the M3 level as shown in Fig.10a. It should be noted that the value of ERR depends on the size of the crack used in the calculation. Since only one crack size was used, the result from this calculation can provide only a qualitative guideline to evaluate the mechanical stability of the air-gap structures. Nevertheless, such a large increase in the ERR should be considered to be a serious concern. For this reason, we compared those ERR values with the ERRs for a partial air-gap structure where only the dielectrics between dense metal lines were replaced by air-gaps, thus avoiding any long air gap structure butting the M3 line on top of the via (see Fig.9). This resulted in a significantly reduction of the ERRs as shown in Fig.10b. Thus the results again indicate that the air gap dimension is a critical parameter in controlling the mechanical stability of the air-gap structures subject to chip-packaging interaction. Airgap-specific design is essential to implement a robust airgap interconnect structure, especially for schemes using across-level gap-forming IMD material.

Conclusion

The impact of process induced stresses and chip-packaging interaction on mechanical stability of air-gap interconnect structures have been investigated using multilevel finite element analysis (FEA) models. The ERR was calculated as crack driving force and the results identified low k cap delamination from the Cu barrier and channel cracking of the bridging cap and dielectric overlayers to be serious reliability concerns. The gap width to cap thickness ratio is a critical parameter in controlling the magnitude of the ERR for delamination in the air-gap structure. This result is consistent with that from the CPI study, indicating that a proper design of the air-gap structure is important to ensure its structural reliability during thermal process and packaging assembly.

References

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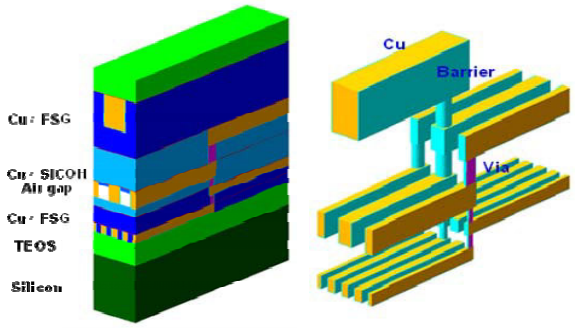

Fig. 1 A five-level model of airgap interconnect

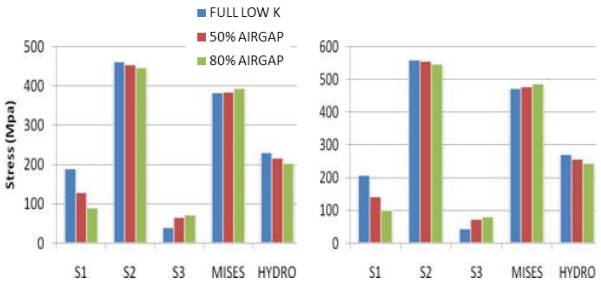

Fig. 2 Comparison of process-induced stresses in Cu lines (M3 and M4) with airgaps.

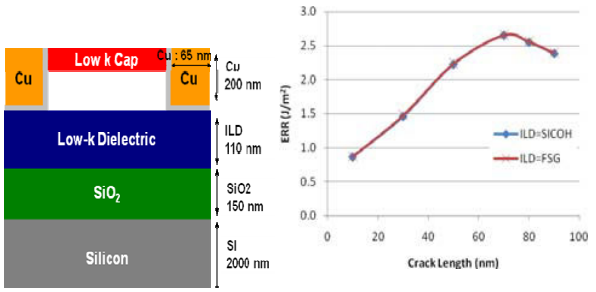

Fig. 3 ERRs for debonding of low k cap from the barrier with different ILD materials for 50% air gap.

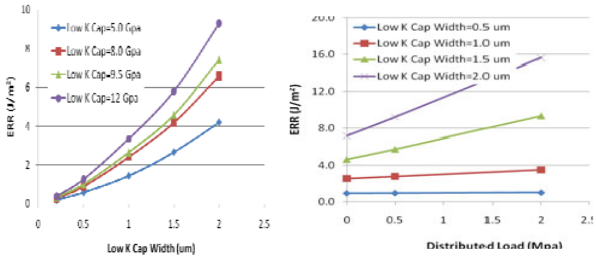

Fig. 4 ERRs for debonding with different low k cap moduli for 50% airgap.

Fig. 5 ERRs with different low K cap width for 50% airgap under external loading

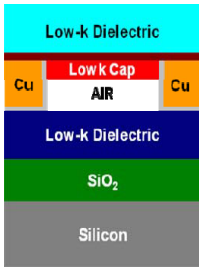

Fig. 6 A simplified airgap structure with a low k overlayer.

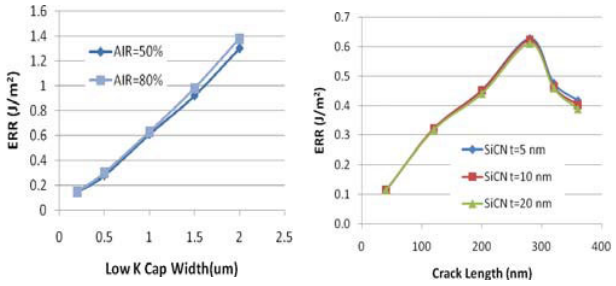

Fig. 7 (a) ERRs for overlay cracking with different low k cap width (b) ERRs with different passivation thickness.

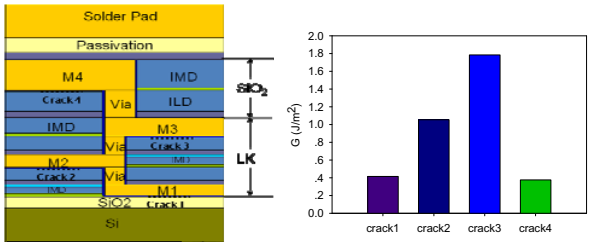

Fig. 8 ERR for 4 level interconnect with Full Low-K

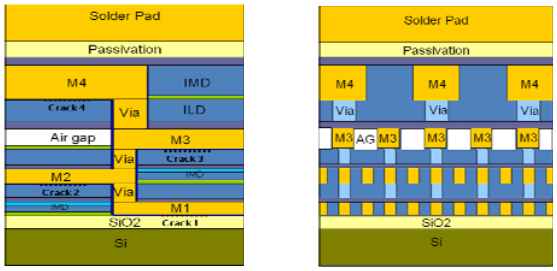

Fig. 9 3D 4-level interconnect model with full air gap structure

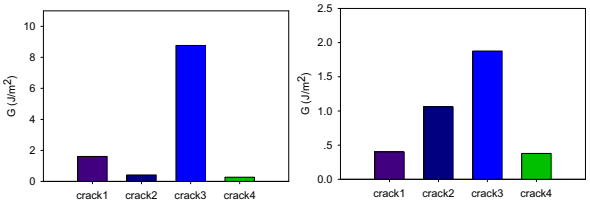

Fig. 10 ERR for 4 level interconnect with a. full air gap and b. partial air-gap