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Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2019.2942364

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Du, H., Reigosa, P. D., Ceccarelli, L., & Iannuzzo, F. (2020). Impact of Repetitive Short-Circuit Tests on the Normal Operation of SiC MOSFETs Considering Case Temperature Influence. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *8*(1), 195-205. [8844745]. https://doi.org/10.1109/JESTPE.2019.2942364

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Impact of Repetitive Short-Circuit Tests on the Normal Operation of SiC MOSFETs Considering Case Temperature Influence

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***Abstract*—This paper presents the impact of repetitive short-circuit tests on the normal operation of a commercial Silicon Carbide (SiC) MOSFET and the influence of different case temperatures on the short-circuit degradation process. To ensure repeatable short-circuit test conditions, the maximum short-circuit withstanding time is studied at three different case temperatures, and the critical energy is identified. In order to investigate the effect of short-circuit stress on the normal operation, the static and dynamic characteristics are periodically measured along with repetitive short-circuit activity. The turn-on switching loss increases gradually with the increasing number of repetitive short-circuit tests. This is associated with the increase of the gate leakage current during the short circuit tests, which shows a reduction of the on-state gate voltage because of the gate oxide degradation. Then, since the case temperature of the device is subject to the operating condition in the application, the degradation process of repetitive short-circuit tests with respect to different case temperatures are investigated, and the relationship between the number of repetitions to failure and the initial case temperature is established. Finally, the case temperature influence is explained by a 1-D transient thermal model based on the short-circuit condition.**

***Index Terms*—Temperature, degradation, power MOSFET, short circuit, Silicon Carbide, switching characteristics.**

I. Introduction

SILICON Carbide (SiC) power semiconductor devices are becoming more and more attractive in power electronics applications, e.g., electric vehicles, railway traction, and power grids, thanks to their superior physical properties over silicon-based devices [1] [2]. The higher breakdown electric field strength, thermal conductivity and carrier velocity provide the capability for SiC devices in faster switching, higher voltage and higher temperature operations [3] [4]. Therefore, the reliability of SiC MOSFETs becomes critical in order to meet the long-term application requirement, especially the reliability under abnormal operating conditions, such as overcurrent, overvoltage, Unclamped Inductive Switching (UIS) [5] and Short Circuit (SC) [6]. Among these, the SC conditions receive extensive attention since the device withstands both high voltage and high current at the same time.

Due to the smaller chip size and thinner gate oxide, the robustness of SiC MOSFETs regarding the SC condition is lower than their Si counterparts [7] [8]. So far, two chip-related failure mechanisms under SC conditions have been found [9]. Thermal instability is one of them; during a single SC event, a high-energy pulse is dissipated in a relatively short time, and the internal temperature increases well above the rated limits. The drain leakage current, caused by the drift of thermally generated carriers, could trigger positive temperature feedback when it achieves a considerable value and eventually leads to the thermal runaway [10] [11]. The other main observed failure mechanism is the gate oxide damage. The gate oxide thickness needs to be thinner due to the larger bandgap of the SiC material, and therefore the gate structure is fragile [12]. The leakage current from gate to source, generated by the creation of conductive paths, is increased by the high electric field and high temperature [7] [13]. In [14], four possible different conductive paths have been identified.

On the other hand, the failure mechanism is dependent on the amount of dissipated SC energy [10]. The influence of the gate-source voltage, DC-link voltage, gate resistance, and pulse time duration on the SC energy have been investigated in [15]. Since an undesirable SC fault may occur in a variety of ways during the lifetime of the devices and at least 2 μs is needed for the commercial drivers to react, the repetitive SC tests could reflect the impact of a single SC event and also provide more insights about the degradation process [16] [17]. With the aid of repetitive SC tests, aging indicators can be explored comprehensively. The shift of the gate threshold voltage, the reduction of the gate-drain capacitance and the increase of the gate leakage current, drain leakage current and on-state resistance [7] [18]–[21] have been proposed as the indicators to evaluate the degradation after repetitive SC events. However, the effect of SC events on the normal operation of SiC MOSFETs, especially on switching performance, needs to be taken into account.

At the same time, the case temperature of the device, which is subject to the operating conditions or real application scenarios, needs to be considered. In [10] and [22], the temperature-dependent SC capability and robustness are

Manuscript received May 29, 2019; revised August 31, 2019; accepted September 7, 2019.

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analyzed, which is limited by the heat-generated leakage current and related to thermal runaway [23]. The gate-oxide damage is also observed by the failure analysis after SC test at 150 ºC [24]. However, the impact of different case temperatures on the SC degrading process still needs to be investigated.

In this context, the aim of this paper is to analyze the effect of repetitive SC tests on the electrical performances of 1000 V/ 22 A discrete SiC MOSFETs at different case temperatures with 3rd-generation planar technology. This work mainly focuses on the variation of static and dynamic characteristics and the influence of case temperature on the number of SC repetitions until failure. The paper is organized as follows:

After an introduction, in Section II, the SC test setup for SiC MOSFETs is presented and the maximum SC withstanding time with respect to different initial case temperatures are presented. In Section III, the repetitive SC tests are performed at room temperature combined with static and dynamic characterizations. Several aging indicators, including gate leakage current and on-state resistance, have been analyzed in detail. The relationship between the on-state gate-source voltage during SC tests and the gate leakage current measured is verified. The switching waveforms and losses are obtained by the standard Double Pulse Tests (DPT). Section IV presents the repetitive SC tests at different initial case temperatures. The gate-source voltage, which is related to the gate leakage current, is used as an aging indicator. A relationship between the number of SC repetitions (N_{SC}) and the case temperature is presented in the same section as well. Finally, in order to understand the impact of case temperature on the gate degradation, the chip temperature evolution during SC tests are simulated. Section IV draws the conclusions.

II. Short-Circuit Aging Test

A. Configuration of Experimental Setup

A Non-Destructive Tester (NDT) has been built for the SC tests with DC-bus voltage and current limits of 2.4 kV and 10 kA [25]. The basic schematic of the NDT and its appearance are shown in Fig. 1 and Fig. 2, respectively. The needed energy for SC tests is provided by a high voltage power supply (V_{DC}) and a high-power capacitor bank (C_{DC}). The series protection consists of four paralleled IGBT power modules to ensure high current capability and at the same time interrupt the SC current immediately after the pulse in order to avoid the device destruction and allow for post-failure analysis. The busbar is custom-designed for even current distribution and the stray inductance is about 10 nH. The control signals to the gate drivers for both series protection and the Device Under Test (DUT) are provided by a 100 MHz Field-Programmable Gate Array (FPGA) board. A commercial SiC MOSFET isolated gate driver by CREE is used and the gate-source voltage is set to +15 V/ –4 V. During the SC tests, drain-source voltage, drain current and gate-source voltage waveforms are measured by means of the HDO6054-MS oscilloscope with the high voltage probe (LeCroy PPE 2 kV), Rogowski coil current probe (PEM CWT6), and the passive voltage probe (LeCroy PP018), respectively.

The DUT is a 1000 V/ 22A discrete SiC MOSFET with 3rd generation planar technology (CREE C3M0120100K) [26] and it has separate Kelvin source pin (TO-247-4) to ensure low

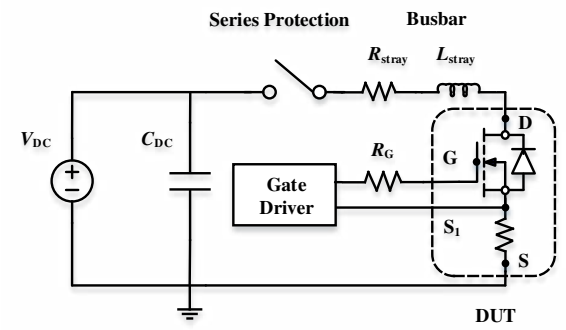

Fig. 1. Principle schematic of the Non-Destructive Tester (NDT).

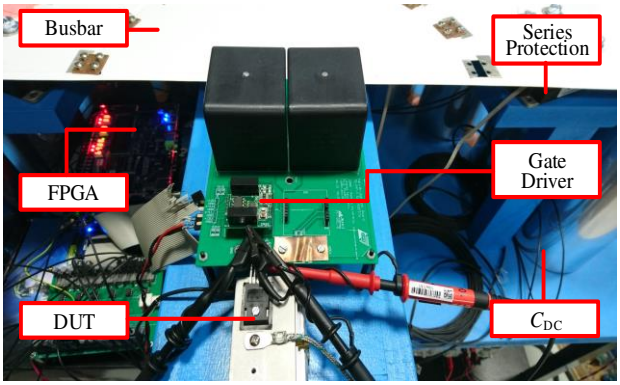

Fig. 2. Appearance of NDT with DUT and PCB adaptor.

common-source inductance package. Initially, the matched fresh devices, which have similar initial static characteristics, especially threshold voltage (V_{th}) and output characteristics (I_D-V_{DS}), are selected to ensure the similar SC energies under the same SC conditions. Then, they are used as the DUTs and numbered from S_1 to S_9. Besides, a temperature controller and electrical heater are used to investigate the impact of different initial case temperatures and an isolated Thermal Interface Material (TIM) is used between the DUT and heating plate during the SC tests. Since the drain-source voltage (V_{DS}) is clamped to the DC-bus voltage during the SC test, the impact of output capacitance (C_{OSS}), which is always charged, could be negligible.

B. Temperature-Dependent Maximum SC Withstanding Time

The maximum SC withstanding time is experimentally investigated at different initial case temperatures for the three fresh devices, which have similar static characteristics (S_1, S_2, and S_3). The results help to identify the critical energy and make sure that the selected testing conditions for the repetitive aging SC tests are below critical SC energy.

The SC waveforms under a bias voltage of 600 V with increasing pulse time duration at three case temperatures (i.e. T_C = 25 ºC, 100 ºC, and 150 ºC) are shown in Fig. 3. At 25 ºC case temperature, the reduction of the gate-source voltage appears when the pulse time duration increases to 4 µs, indicating a gate oxide damage. On the other hand, it can be observed in the blue dotted boxes that a tail current appears at turn-off for the SC pulse durations larger than 2.5 µs at each case temperature. This phenomenon is in agreement with previous work [9], and its mechanism is also confirmed in [11] and [20]. The high temperature within the depletion region

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leads to a thermal generation current flowing across the device junction. If the leakage current is high enough, a thermal runaway mechanism might be triggered [22]. As can be seen in the red dotted boxes in Fig. 3 (b) and (c), the devices fail after turning off, which confirms the thermal runaway mechanism.

The SC withstanding time duration decreases from 4 µs to 3 µs and then 2.7 µs when the initial case temperature increases from 25 ºC to 100 ºC and 150 ºC. The SC energy is calculated when the failure is observed, being 0.15 J, 0.13 J to 0.12 J with increasing case temperature. The summary of the SC tests with increasing time duration at different case temperatures is listed in Table I.

TABLE I
SUMMARY OF SC TESTS WITH INCREASING TIME DURATION AT DIFFERENT CASE TEMPERATURES

No.	Case temperature (ºC)	SC withstanding time (µs)	Critical energy (J)	Failure mode
S_1	25	4	0.15	Gate oxide damage
S_2	100	3	0.13	Thermal runaway
S_3	150	2.7	0.12	Thermal runaway

III. STATIC AND DYNAMIC CHARACTERISTICS VARIATIONS

A. *Static Characteristics Variations*

In order to evaluate the impact of repetitive SC tests on the static characteristics in the normal operation, another fresh DUT (S_4) is firstly investigated with the static characterization between repetitive SC tests by means of the Power Device Analyzer (Keysight B1506A).

With the aim of performing the repetitive SC tests below the maximum SC critical energy, the testing conditions are set to V_{DC} = 600 V, t_{SC} = 2.2 µs and T_C = 25 ºC. The output voltage of the gate driver is fixed to +15 V/ –4 V during the repetitive SC tests, and the gate resistance is equal to 20 Ω, which dampens the oscillation when the device turns off. Initially, the static characteristics, including threshold voltage (V_{th}), gate leakage current (I_{GSS}), drain leakage current (I_{DSS}) and on-state resistance ($R_{DS,on}$) are measured on the fresh device. Then, the repetitive SC tests are performed, and the drain-source voltage (V_{DS}), gate-source voltage (V_{GS}) and drain current (I_D) waveforms are recorded during SC tests. Every 10 SC repetitions, the static characterizations are performed again. The drain current and gate-source voltage waveforms from the 20th to 140th repetition are shown in Fig. 4. A reduction of the on-state gate-source voltage and on-state drain current are observed with the increasing number of repetitions. This phenomenon could be explained by the gate oxide degradation mechanism; the conductive paths, which are formed through the

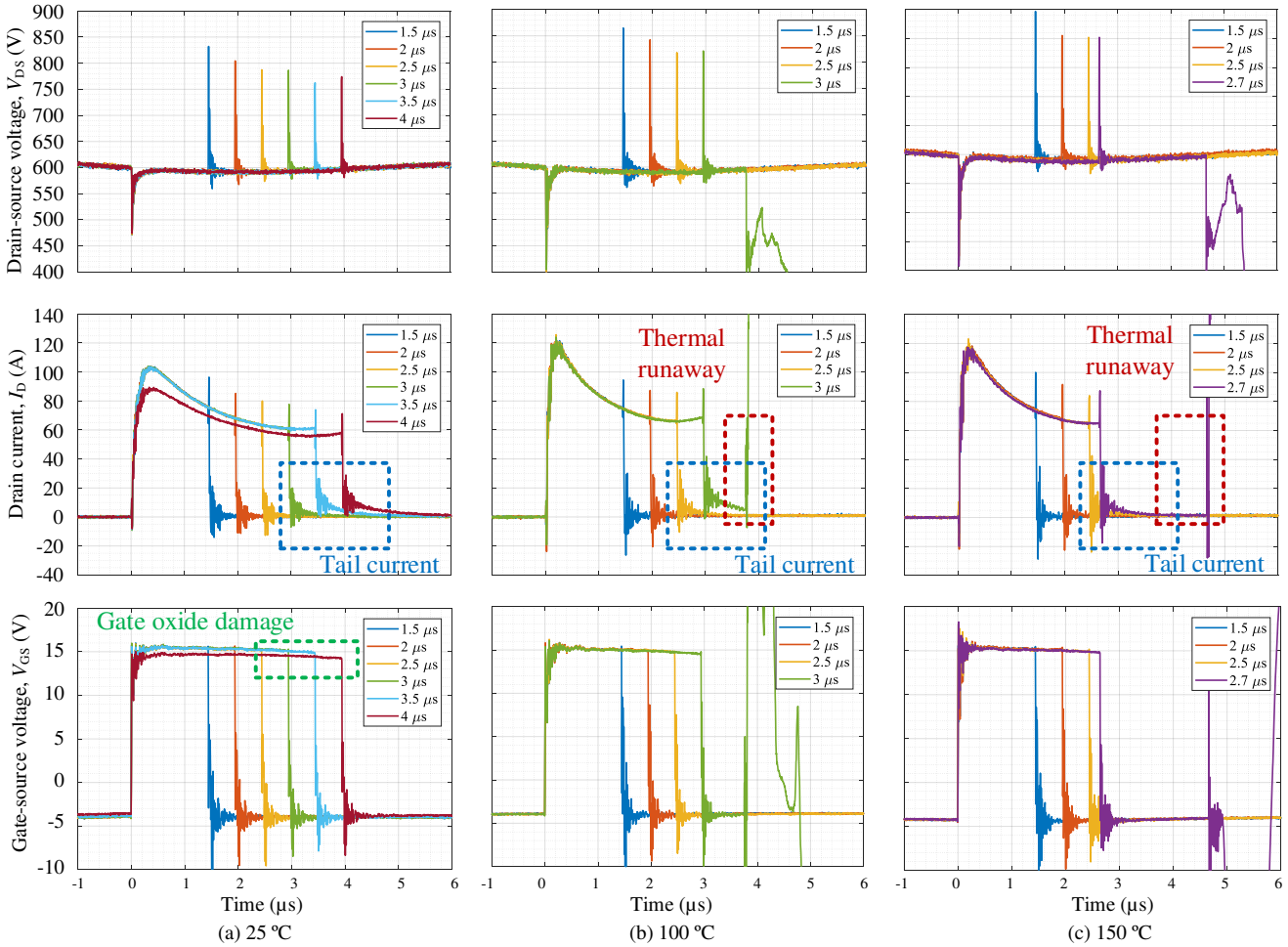

Fig. 3. Drain-source voltage, drain current and gate-source voltage waveform of SC tests with increasing time duration at different case temperatures. In the blue dotted boxes, tail currents are highlighted. The gate oxide damage and thermal runway are marked in the green and red dotted boxes, respectively.

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gate oxide during the SC tests lead to a gradually increasing gate leakage current (I_{GSS}) and eventually cause a permanent gate oxide damage. At the same time, the considerable I_{GSS} forms a voltage drop across the gate resistance, which decreases the effective gate voltage on the device during on-state operation. It is shown as the reduction of on-state V_{GS} during the SC tests and leads to the SC drain current I_D decrease. Therefore, the effective gate voltage (V_{GS}) can be expressed by the output voltage of the gate driver (V_{driver}), external gate resistance (R_G) and gate leakage current (I_{GSS}) as (1).

$$V_{GS} = V_{driver} - R_G \times I_{GSS} \quad (1)$$

The variation of on-state V_{GS} and I_D during SC test is also in agreement with the results in [27], which is related to the degradation of the gate structure.

The results of the gate leakage current measured with the power device analyzer in Fig. 5 confirm the gate degradation. After 30 SC repetitions, the gate leakage current jumps from 4.87 pA (after 20 SC repetitions) to 6.33 mA when the V_{GS} is equal to 15 V. The I_{GSS} increases significantly after 40 SC repetitions and decreases again after 50 SC repetitions, which might be affected by the electrons de-trapping mechanism [28] [29]. Thereafter, it increases gradually from the 50th repetition, and the SC tests stopped after 140 repetitions when the maximum gate leakage current reaches 100 mA.

The threshold voltage (V_{th}) is measured with the power device analyzer (Keysight B1506A), and the connection diagram is shown in Fig. 6. Since the gate and drain terminals are connected together internally while measuring V_{th}, the effect of the gate leakage current needs to be considered.

Fig. 7 shows the variation of I_D-V_{GS} curves every 10 repetitions, and it can be divided into three stages. From the initial state to the 20th repetition, the threshold voltage shifts positively. This phenomenon can be explained by the electrons trapping. When a positive bias is applied to the gate, the electric field stress across the oxide is very high because of the small gate oxide thickness. The electrons at the strongly inverted surface tunnel into or through the gate oxide (i.e. the SiO_2 layer between substrate and polysilicon). This mechanism is named Fowler-Nordheim tunnelling, and it is explored in detail in [7] [30]. Therefore, an increase in the net negative charge (i.e. electron trapping) could result in a positive shift of the threshold voltage and the threshold voltage can be expressed as [31]:

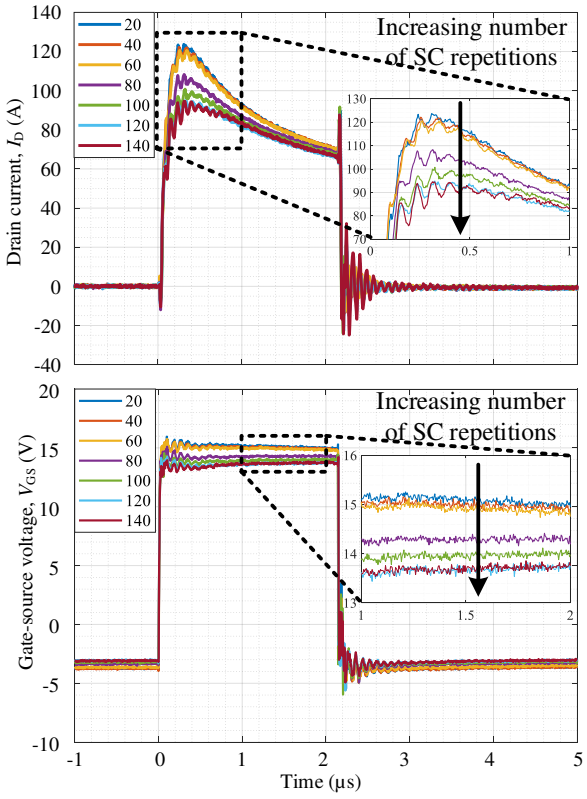

Fig. 4. Drain current and gate voltage waveforms of repetitive SC tests from 20th to 140th repetition at room temperature.

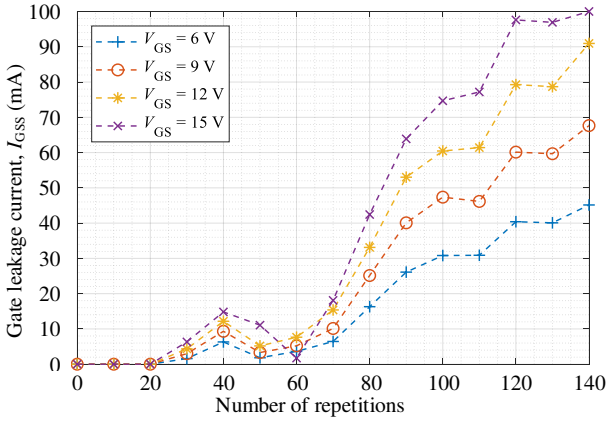

Fig. 5. Gate leakage current increases after repetitive SC tests.

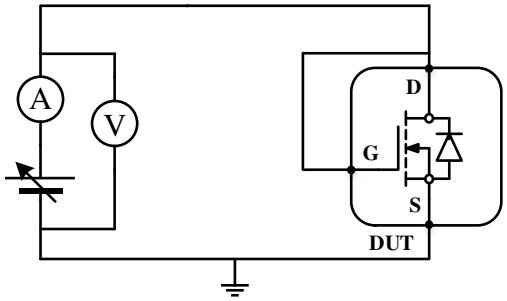

Fig. 6. The connection diagram of V_{th} measurement by Keysight B1506A.

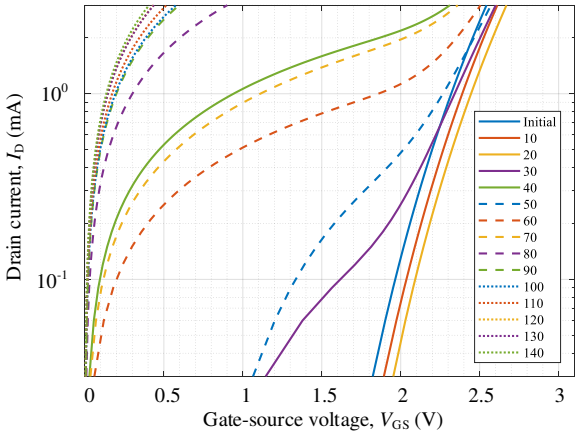

Fig. 7. I_D-V_{GS} curves variation after repetitive SC tests.

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$$\begin{cases} Q_{ox} = Q_T + Q_m + Q_I + Q_F \\ V_{th} = V_{thi} - \frac{Q_{ox}}{C_{ox}} \end{cases} \quad (2)$$

Where V_{thi} is the initial threshold voltage, Q_{ox} is the charges in gate oxide, and C_{ox} is the specific capacitance of the gate oxide layer. The oxide contains four types of positive charges: trapped oxide charge (Q_T), mobile charge (Q_m), fixed oxide charge (Q_F) and interface state charge (Q_I).

In the second stage of Fig. 7, the drain current increases gradually with the increasing V_{GS} after 30 repetitions. Since the gate and drain terminals are connected together, this phenomenon shows that a conductive path inside the gate oxide has been formed. In this case, a small current going through the gate oxide contributes to the I_D and the threshold voltage cannot be obtained accurately in this way. The last stage starts from the 80th repetition to the 140th repetition and the curves indicate that the gate oxide conductivity increases gradually.

The on-state resistance is calculated by the output characteristics (I_D-V_{DS}) when the $V_{GS,set}$ is set to 15 V and I_D is equal to 15 A. In Fig. 8, the $R_{DS,on}$ increases with the increasing number of repetitions and this could be explained by the positive threshold voltage shift and the effective gate-source voltage reduction as mentioned above. From the initial state to the 20th repetition, the effective V_{GS} remains as 15 V and $R_{DS,on}$ increases owing to the positive V_{th} shift. Thereafter, the effective V_{GS} applied on the device becomes lower than its settings value (i.e. $V_{GS} < V_{GS,set}$ = 15 V), which could lead to further increase in $R_{DS,on}$. Besides, the reduced mobility from increased oxide charge scattering might be another factor, and it needs to be further investigated.

An obvious correlation between the on-state gate-source voltage during SC tests and the gate leakage current is obtained. Fig. 9 shows the reduction of the on-state gate-source voltage at 2 µs and the increase of the gate leakage current, measured by means of static characterization, with the number of SC repetitions increasing. The SC tests are stopped at 140th repetition when the maximum gate leakage current increases up to 100 mA, and in this case, the minimum gate-source voltage at 2 µs is equal to 13.6 V, which is decreased by 9.3 % if compared to 15 V. Since the gate oxide degradation has also been observed on the other types of commercial SiC MOSFETs [7] [15], the reduction of V_{GS} could be considered as an aging indicator and the reduced value needs to be further confirmed for the other devices.

Furthermore, another fresh DUT (S_5) is used to monitor the I_G variation during repetitive SC tests in order to confirm the increasing gate leakage current during repetitive SC tests and ensure the gate oxide degradation at the same time. In this case, another voltage probe is placed before the external R_G (20 Ω) and the voltage drop on the R_G can be measured during SC tests. Then the gate current I_G during SC tests can be calculated with the R_G and the measured voltage drop across the R_G. Fig. 10 shows the relationship between the average I_{GSS} (from t = 1 µs to 2 µs) and the on-state V_{GS} at 2 µs. When the V_{GS} at 2 µs decreases to 13.6 V, the repetitive SC tests are stopped after 124 SC repetitions, and the I_{GSS} is equal to 73.34 mA. Thereafter, the I_{GSS} is also measured with the power device analyzer, and it reaches 100 mA when the V_{GS} is 12.3 V. Therefore, the on-state gate voltage at 2 µs during SC tests (nearly at the end of the pulse time duration) is selected as the aging indicator in order to evaluate the degradation process in the following tests.

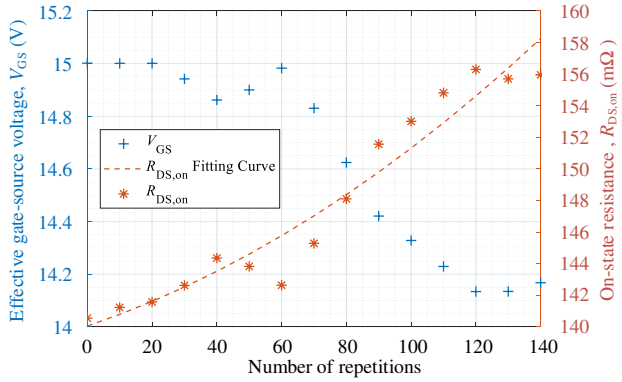

Fig. 8. On-state resistance increases after repetitive SC tests ($V_{GS,set}$ = 15 V and I_D = 15 A) and the effective gate-source voltage (V_{GS}) decreases, measured at the same time by static characterization.

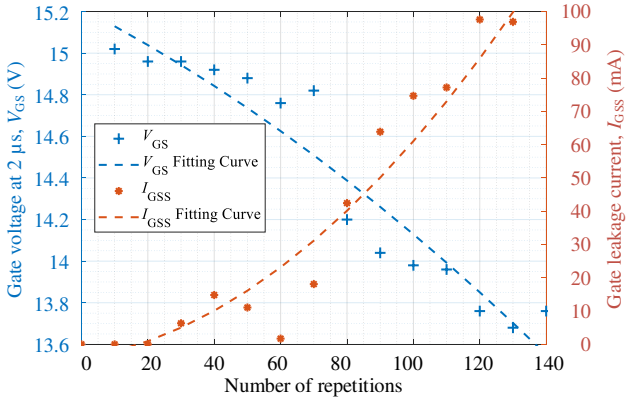

Fig. 9. Correlation between the on-state gate voltage (t = 2 µs) during SC tests and the gate leakage current, measured by static characterization ($V_{GS,set}$ = 15 V) (S_4).

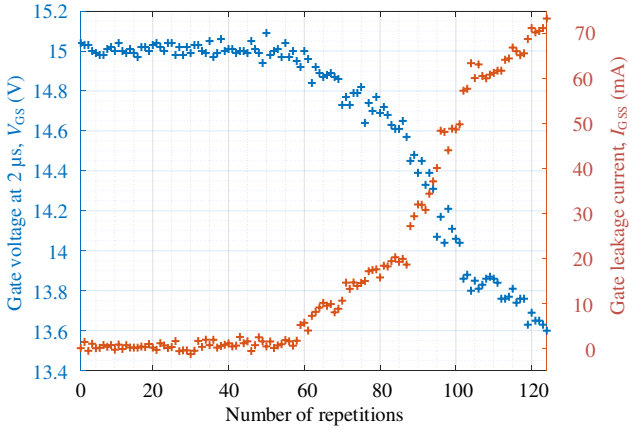

Fig. 10. Correlation between the on-state gate voltage (t = 2 µs) and the average gate leakage current during SC tests (S_5).

B. *Dynamic Characteristics Variations*

The SC robustness of power semiconductor devices is typically assessed on fresh components; however, a SC event could occur several times along the life of the component

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during normal operation and its effect on the normal operation of the device can be quite different, depending on the level of degradation. Therefore, in this section, Double-Pulse Tests (DPT) are combined together with repetitive SC tests for the fresh DUT (S_6) in order to investigate the degradation of the normal operation of the SiC MOSFET after repetitive SC tests.

The schematic of the standard DPT is shown in Fig. 11 [32]. A 1.2 kV / 20 A SiC Schottky diode (D_1) is used as the freewheeling diode and the inductance of load is equal to 620 µH. The DUT is driven by a +15 V/ –4 V gate voltage, and the used gate resistance and capacitance are equal to 20 Ω and 4.7 nF in order to slow down the switching and mitigate the parasitic inductance in the gate loop, which might cause the oscillation during switching transient. Fig. 12 shows the V_{DS}, I_D, and V_{GS} waveforms during DPT and the first pulse time (t_1= 18 µs) is used to increase the current to its rated value. Then, there is a delay of 6 µs (t_2) between the first and second pulse for the device to settle out. The second narrow pulse time (t_3) is set to 6 µs and the SC aging test condition is set the same as before (V_{DC} = 600 V, t_{SC} = 2.2 µs and T_C = 25 ºC).

Initially, the standard DPT is performed on a fresh device (S_6) and the drain-source voltage, gate-source voltage and drain current waveforms are measured. Then the repetitive SC tests are performed and after each 20 SC repetitions, the DPT is carried out again to analyze the impact of SC aging stress on the dynamic characteristics. The SC tests stop at 110th SC repetition when the on-state V_{GS} at 2 µs during SC test, i.e. the aging indicator, decreases to 13.6 V. Thereafter, the last DPT is performed on the degraded device after 110 repetitions.

The V_{DS}, V_{GS}, and I_D waveforms during turn-on and turn-off transitions before and after 110 repetitions of SC tests (i.e. the initial and the last one) are shown in Fig. 13 and Fig. 14, separately. After repetitive SC aging tests, the device turns on slower and turns off faster than before. This phenomenon could be explained by the reduction of the effective gate-source voltage V_{GS}.

During turn-on transient, no I_D flows through the device until V_{GS} exceeds V_{th}. Due to the reduction of the effective V_{GS} after SC tests, it takes longer time to reach V_{th}, which leads to the increased delay of I_D. When V_{GS} is larger than V_{th}, I_D is given by (3) [33].

$$I_D(t) = g_m[V_G(t) - V_{th}] = \frac{\mu_{ni} C_{ox} Z}{2L_{CH}}[V_G(t) - V_{th}]^2 \quad (3)$$

Where g_m is the transconductance of the device, μ_{ni} is the inversion layer mobility, C_{OX} is the specific capacitance of the gate oxide, L_{CH} is the channel length, and Z is the equivalent channel width. At the same time t, the lower effective V_{GS} results in the lower I_D, which is in agreement with the waveform in Fig. 13. On the other hand, the reduction of mobility and the increased scattering from trapped charges might cause the reduction in transconductance. Further investigations are needed on this point. Similarly, during the turn-off transient, the effective V_{GS} after SC tests needs less time than before to decrease to V_{th}, and thus the I_D starts to decrease earlier in Fig. 14.

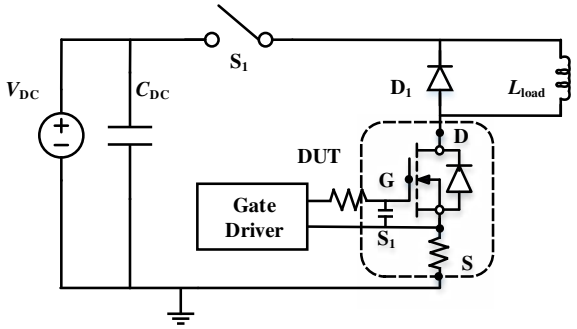

Fig. 11. Principle schematic of the standard Double Pulse Test (DPT).

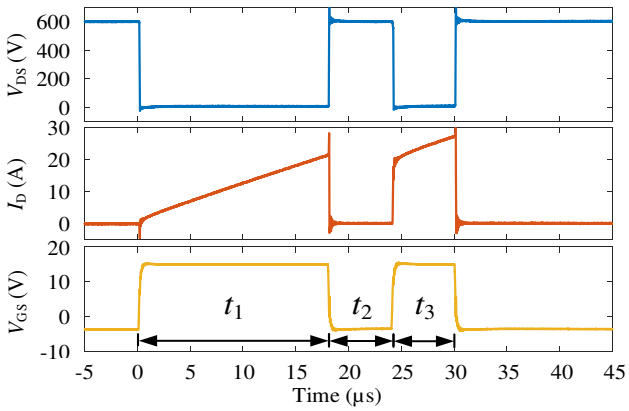

Fig. 12. Drain-source voltage, drain current and gate-source voltage waveform of Double Pulse Test.

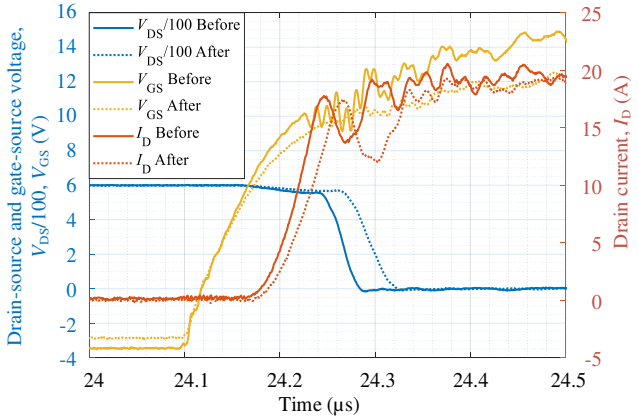

Fig. 13. Drain-source voltage and drain current waveforms during turn-on time before and after 110 repetitions of SC tests.

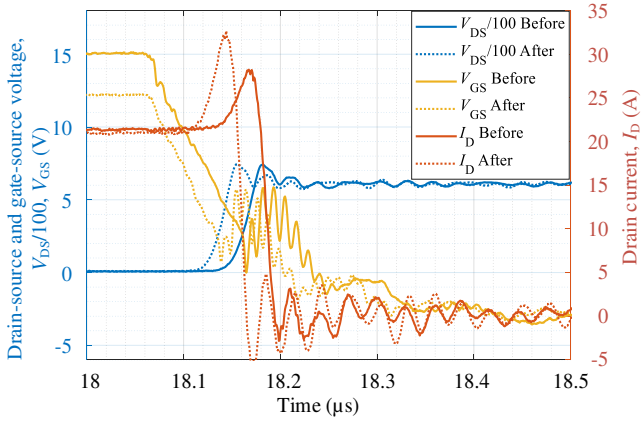

Fig. 14. Drain-source voltage and drain current waveforms during turn-off time before and after 110 repetitions of SC tests.

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Fig. 15 shows the reduction of on-state gate-source voltage and the variation of switching loss with increasing number of SC repetitions. The turn-on loss increases after 80 SC repetitions because of the delay of turn-on V_{DS}, which is similar to [34], and it is in agreement with the reduction of the aging indicator (V_{GS} at 2 µs). Meanwhile, the turn-off loss variation induced by the SC stress is not obvious and it only increases slightly at the end of repetitions due to the higher current spike during turn-off transition.

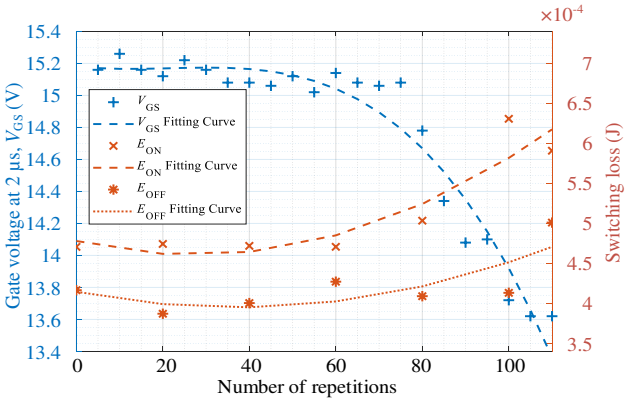

Fig. 15. The reduction of gate-source voltage and the variation of switching loss with the increasing number of repetitions.

IV. Impact of Case Temperature on Short-Circuit Aging

A. *Repetitive SC Tests at Different Temperatures*

The repetitive SC tests are performed with 600 V bias voltage and 2.2 µs pulse time duration at 25 ºC, 100 ºC, and 150 ºC for the three fresh DUTs (S_7, S_8, and S_9), which have matched static characteristics, in order to investigate the impact of different case temperatures. The gate resistance used on the driver board is equal to 6.67 Ω, and the output voltage of the gate driver is fixed as +15 V/ –4 V.

Fig. 16 presents the drain-source voltage, drain current, and gate-source voltage waveforms at different temperatures, and the gate oxide degradation similar to Fig. 4 is observed in each case; the on-state gate voltage and drain current decreases with the number of SC repetitions increasing, which indicates the increase of gate leakage current.

The experimental results obtained in Fig. 9 shows that when the on-stage gate-source voltage decreases from 15 V to 13.6 V, the device could be considered as a failed device; therefore, this criterion is considered for the following repetitive SC tests. The V_{GS} variation (at 2 µs) with increasing repetitions at 25 ºC, 100 ºC, and 150 ºC are shown in Fig. 17. The number of repetitive SC tests until failure (N_{SC}) increases from 194 repetitions (25 ºC) to 224 repetitions (100 ºC), and then to 422 repetitions (150 ºC) with the case temperature increase. The relationship between the number of repetitions to failure and the initial case temperature is presented in Fig. 18, and it could be fitted as (4).

$$N_{SC} = f(T_c) = 130.9 \times \exp(0.007457 \times T_c) \quad (4)$$

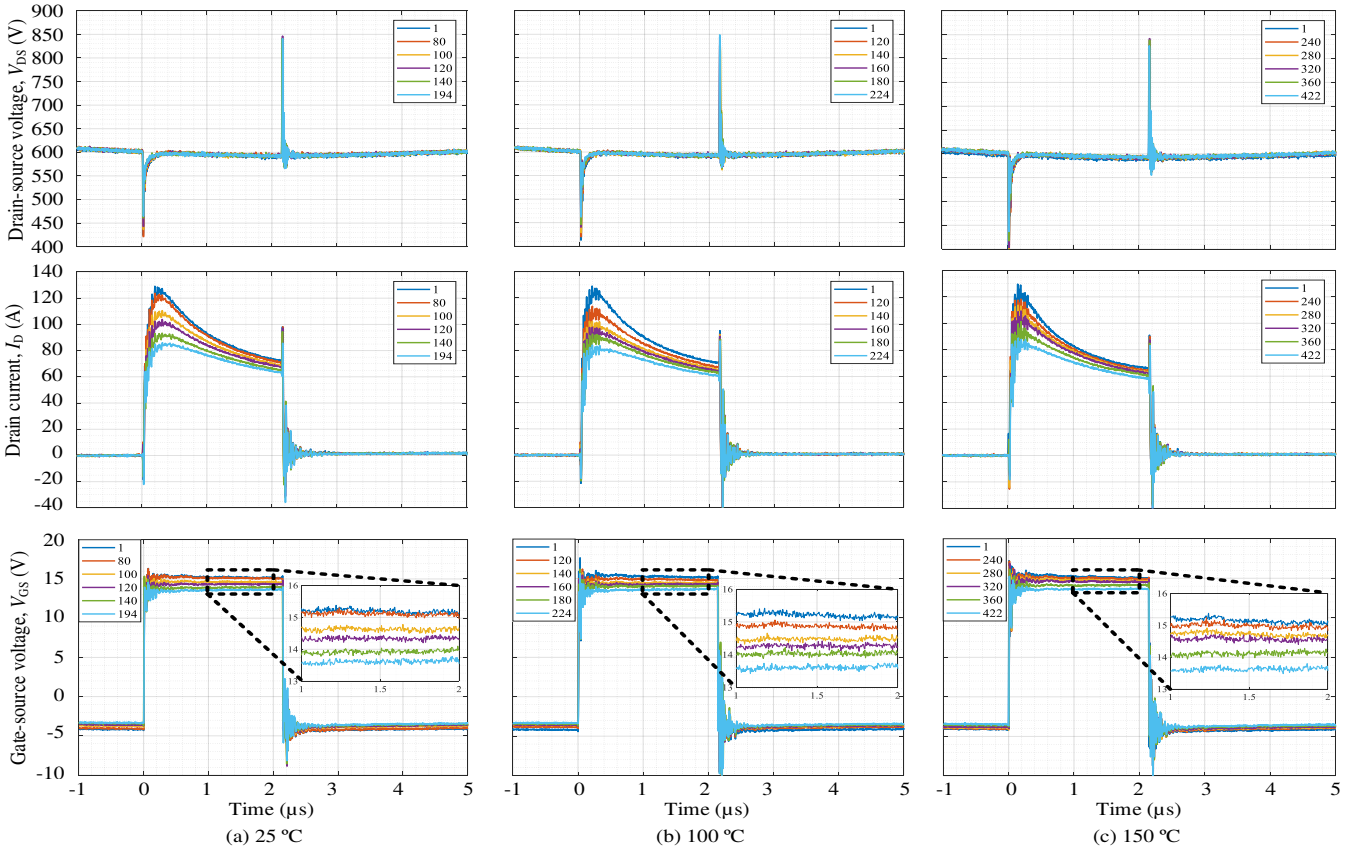

Fig. 16. Drain-source voltage, drain current and gate-source voltage waveform of repetitive SC tests with fixed pulse time duration (t = 2.2 µs) at different case temperatures.

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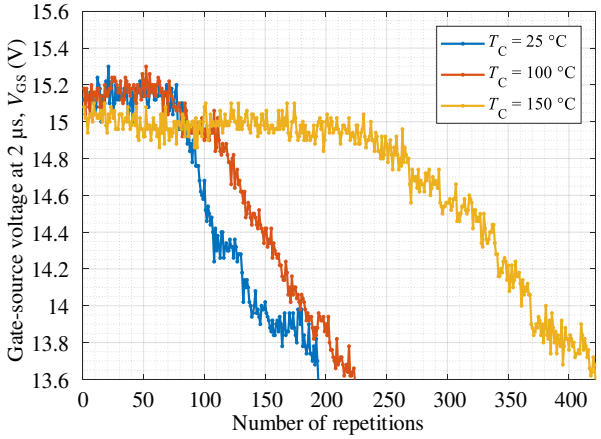

Fig. 17. Gate voltage at 2 µs (V_{GS}) variation with increasing SC repetitions at different case tempeatures.

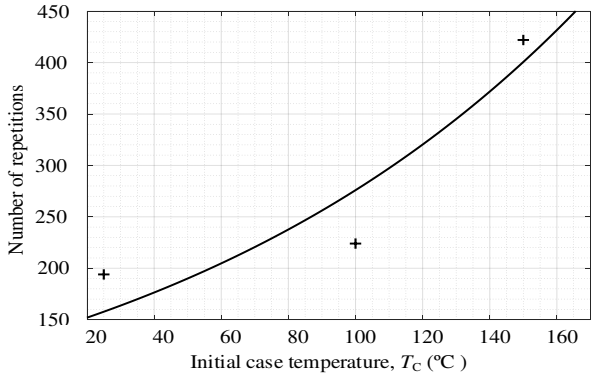

Fig. 18. Relationship between the number of repetitions to failure and the case temperature.

One may think that the increasing case temperature could lead to earlier failures; however, this is not the case for SiC MOSFETs, since the drain current decreases with temperature due to its negative temperature coefficient, leading to lower SC energies.

As can be seen in Fig. 19, the gate-source voltage during the first SC test at different case temperature keeps the same value. The drain current during the first SC test at 150 ºC case temperature is the lowest one, and the drain current at 25 ºC is higher than 100 ºC. The SC energy from t = 0 µs to 2.2 µs is also calculated for each repetition of SC tests with respect to different case temperatures, as shown in Fig. 20. In the first stage (SC tests within 100 repetitions), the SC energy at 25 ºC case temperatures is higher than 100 ºC and 150 ºC, and all the calculated values are below 0.12 J, which is the critical energy at 150 ºC. Thereafter, when more than 100 repetitions are performed, the SC energy reduction is mainly determined by the reduced drain current caused by gate degradation.

B. Thermal Behavior Simulation of SC Tests

In order to investigate how the higher SC energy results in the less number of SC repetitions to failure, the thermal behavior during SC test is considered. Since the very fast temperature transient during SC operation (i.e. t = 2.2 µs) cannot be easily approached in measurement, a thermal simulation is performed to estimate the transient temperature. Therefore, a 1-D heat propagation model is used to analyze the

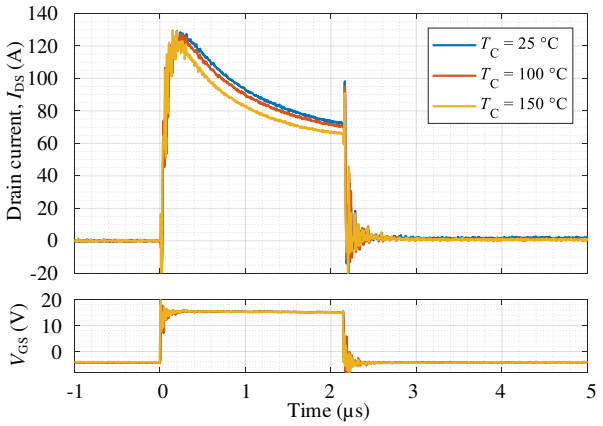

Fig. 19. Drain current and gate-source waveforms during the 1st repetition SC test at different case temperatures.

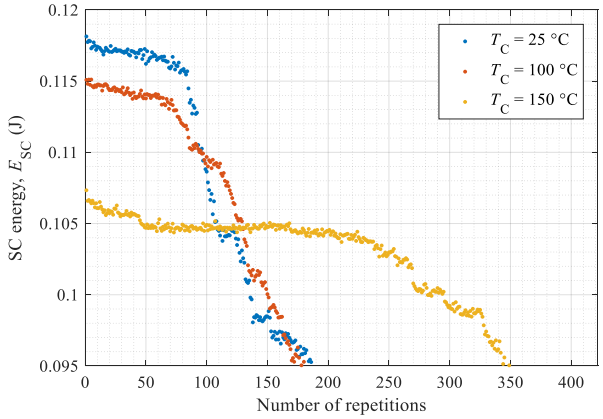

Fig. 20. Short-circuit energy (E_{SC}) variation with increasing number of SC repetitions at different case temperatures (25 ºC, 100 ºC and 150 ºC).

thermal behavior during SC test at different initial case temperatures as shown in Fig. 21.

The estimated doping concentration in the N- drift layer is 1 × 10^{16} cm^{-3} and the junction depth is 0.6 µm (x_j = 105.6 µm). The depletion width in the P-well layer (x_p) is omitted in the model due to the negligible thickness. The width in the N- drift layer (x_n) can be calculated by (5) where ε_s is the dielectric constant of SiC, N_d is the doping concentration in the N-drift region, V_{ds} is the applied voltage during SC test and q is the electron charge [35].

$$x_n \approx \sqrt{\frac{2\varepsilon_s}{qN_d} V_{ds}} \tag{5}$$

The distribution of the electric field density in this region ($x_j \le x \le x_n$) is calculated by (6).

$$E(x) = \frac{qN_d}{\varepsilon_s}\left(x_n + x_j - x\right) \tag{6}$$

During SC tests, the V_{DS} bias is applied, and the on-state drain current goes through the device at the same time. The SC current density $J(t)$ is obtained by the active chip area A and the time-dependent SC current $I_{SC}(t)$, which is derived from the actual SC waveform. Since the V_{DS} changes slightly during the

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SC test, the heat generation rate $Q(x,t)$ can be calculated by (7).

$$Q(x,t) = E(x) \cdot \frac{I_{SC}(t)}{A} \quad (7)$$

Therefore, the classical heat equation in (8) can be solved in the model to simulate the temperature distribution in terms of time.

$$\frac{\partial}{\partial x}\left(\lambda(T) \cdot \frac{\partial T}{\partial x}\right) + Q(x,t) = \rho \cdot c(T) \cdot \frac{\partial T}{\partial t} \quad (8)$$

λ, ρ and c are the thermal conductivity, physical density and specific heat of each material, respectively. Their settings in SiC material are listed as below (9)-(11) [36] and the parameters in other materials (i.e. resin, Al and solder layer) are included in Table II.

$$\lambda(T)_{\mathrm{SiC}} = (0.0003 + 1.05 \times 10^{-5} T)^{-1} \ \ (\mathrm{W/m \cdot K}) \quad (9)$$

$$\rho_{\mathrm{SiC}} = 3.211 \ \ (\mathrm{g/cm^3}) \quad (10)$$

$$c(T)_{\mathrm{SiC}} = 925.65 + 0.3772T - 7.929 \times 10^{-5} T^2 - 3.1946 \times 10^{7}/T^2 (\mathrm{J/kg \cdot K}) \quad (11)$$

During the simulation, the time (t) increases from 0 µs to 2.2 µs in step of 4 ns and V_{DS} is set to 600 V, which are the same as the actual test in part A. The active chip area A is estimated by the measured chip size. The experimental drain current waveform during the first repetitive SC test at different case temperatures in Fig. 19 are used as $I_{SC}(t)$ in the model, in order to obtain an accurate heat generation rate. The temperature boundaries of both top (x = 0 µm) and bottom sides (x = 300 µm) in the 1-D model are set the same as the corresponding initial case temperatures due to the extreme short SC time duration.

Fig. 22 shows the simulation results of the temperature variation ($\Delta T = T - T_{\mathrm{case}}$) at different initial case temperatures (T_{case} = 25 ºC, 100 ºC, and 150 ºC). The maximum junction temperature rise (ΔT_{j}) decreases from 554.1 ºC to 534.8 ºC and then to 506.7 ºC when the case temperature increases from 25 ºC to 100 ºC and to 150 ºC.

This result is coherent with the fact that at higher initial temperatures, the drain current is lower, yielding a reduced SC energy and it indicates that the gate degradation under repetitive aging SC test is mainly related to the temperature variation rather than the maximum junction temperature. Due to the different Coefficient of Thermal Expansion (CTE) between the Aluminum and SiO_2 layer, there would be a mismatch on the interface between the materials, which is shown as the red dotted line in Fig. 21. With the number of short-circuit repetitions increasing, the cracks might appear through the SiO_2 layer. This hypothesis is in agreement with the crack measured by Magnified Focused-Ion-Beam (FIB) after short-circuit stress in [37].

Besides, the Coffin-Manson law is usually used for the temperature cycling condition in order to investigate the bond wire and solder pad degradation. The expected number of cycles to failure N_{f} at a given temperature swing ΔT_{j} and an average temperature T_{m} can be estimated with the equation

$$N_{\mathrm{f}} = A \cdot \Delta T_{\mathrm{j}}^{\alpha} \cdot \exp\left(\frac{E_{\mathrm{a}}}{K_{\mathrm{B}} \cdot T_{\mathrm{m}}}\right) \quad (7)$$

Where K_{B} is the Boltzmann constant, E_{a} is the activation energy, and α and A are the parameters. If the Coffin-Manson law is used for the Al/SiO_2 interface with typical values of power semiconductor packaging (i.e. α = –4, ΔT_{j} = 20 K and N_{f} = 1×10^6), the expected number of SC repetitions to failure is

TABLE II
THERMAL BEHAVIOR SIMULATION SPECIFICATIONS

Parameter	Value	Unit
ε_s	$9.66 \times 8.85 \times 10^{-12}$	F/m
A	3.478	cm^2
λ_{Resin}	0.2	W/(m·K)
ρ_{Resin}	1.8	g/cm^3
c_{Resin}	1000	J/(kg·K)
λ_{Al}	167	W/(m·K)
ρ_{Al}	2.7	g/cm^3
c_{Al}	900	J/(kg·K)
$\lambda_{\mathrm{Solder}}$	50	W/(m·K)
ρ_{Solder}	7.4	g/cm^3
c_{Solder}	190	J/(kg·K)

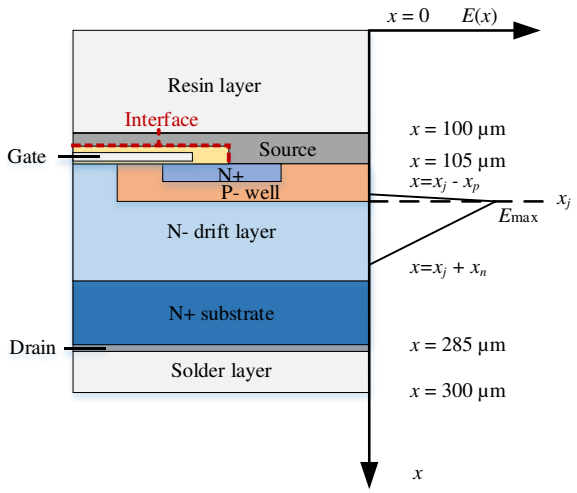

Fig. 21. Heat propagation model (1-D) of the SiC MOSFETs.

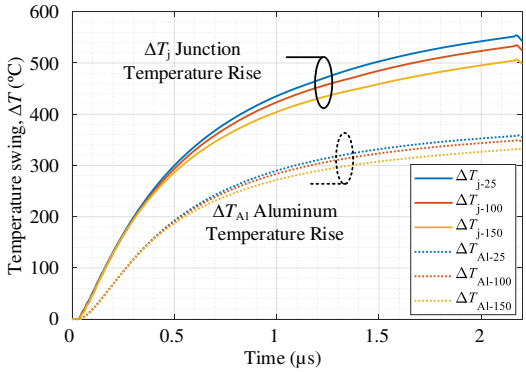

Fig. 22. Simulated junction temprature rise and alumuinum temperature rise at three different case temperatures (25 ºC, 100 ºC and 150 ºC).

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equal to few units since the temperature swing is very high (ΔT_j = 500 K). Therefore, during a SC transient, the higher drain current in terms of lower initial case temperature would lead to a larger temperature gradient and thus less number of repetitions to failure.

V. Conclusions

In this paper, the impact of repetitive SC tests on the normal operation of 1000-V/ 22-A SiC MOSFETs are investigated, and the influence of case temperature on the SC degradation process is presented. The test conditions for repetitive SC tests are selected below the critical energy, which is also temperature-dependent and verified by increasing the SC pulse time duration step by step, and a gate oxide failure is observed with the increasing number of repetitions.

Both dynamic and static characteristics are combined together with repetitive SC aging tests, respectively, in order to investigate the impact on normal operation. The dynamic turn-on and turn-off performance are affected, showing a delay and advance after repetitive SC tests. This phenomenon is caused by the reduction of the effective gate-source voltage on the device. Since the turn-on drain-source voltage delays gradually with the increase of SC repetitions, the turn-on loss increases correspondingly. With respect to static characteristics, the increase of the gate leakage current and on-state resistance are analyzed with increasing SC repetitions. A correlation between the on-state gate-source voltage during SC tests and the gate leakage current is confirmed, and in this case, a 9.3 % reduction of the on-state gate-source voltage is considered as the aging indicator for failure.

The impact of the case temperature on the repetitive SC is also taken into account. The results show that the number of repetitions until failure increases with increasing initial case temperature, which indicates the opposite trend compared to the SC robustness and the relationship between the case temperature and the number of repetitions is presented. This phenomenon can be explained by the lower SC energy due to the drain current reduction at higher case temperature. Thereafter, a 1-D heat propagation model together with experimental SC current waveforms is used to calculate the chip temperature evolution during the first repetitive SC test. The junction temperature rise decreases with the initial case temperature increase, which is in agreement with the fact that the SC energy is reduced at higher case temperature.

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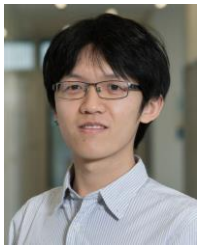

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