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Impact of Self-Heating Effect on Transistor Characterization and Reliability Issues in Sub-10 nm Technology Nodes

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ABSTRACT FinFET and fully depleted silicon-on-insulator (FDSOI) structures could further improve transistor's performance and, however, also introduce some new problems, especially the increasingly severer self-heating effect (SHE). In this paper, by utilizing the ultra-fast sub-1 ns measurement technique, I–V characteristics of FinFETs and FDSOI devices at different switch speeds are obtained. Furthermore, dynamic SHE phenomena as well as the time-resolved channel temperature change during transistor's switch on and off are able to be experimentally observed. And, more accurate device parameters like ballistic transport efficiency are extracted by the ultra-fast measurements. Moreover, it is experimentally confirmed that several nanoseconds are required to heat up the channel of transistors by the direct electrical characterization and, therefore, in sub-10 nm devices, SHE might be alleviated under high frequency/speed operations.

INDEX TERMS Self-heating effect, FinFETs, hot carrier injection, ballistic transport.

I. INTRODUCTION

As the basic unit of integrated circuits, the silicon (Si) metal-oxide-semiconductor field effect transistor (MOSFET) has been shrinking in size for chip's better performance, lower power, smaller area and lower cost. To maintain the pace of device scaling and overcome the short-channel effect, novel device structures, such as fully depleted silicon-on-insulator (FDSOI) and multi-gate FinFETs, have being developed. And more complex gate-all-around nanowire (GAA-NW) architectures and high-mobility Germanium (Ge) or SiGe channels are also being considered for more advanced technology nodes [1].

The thermal management issue began to be noted since Si MOSFETs entered the nanometer-scale era [2] because of the self-heating effect (SHE). The origin of SHE is the accumulated Joule heat generated by the current flow through the channel during transistor's operations. What raises our concern is the elevated local temperature resulted from the worse heat-dissipation ability of MOSFETs [3]–[6]. Joule heat also exists in planar bulk Si devices but has an easy access to spreading to the Si substrate, as shown in Fig. 1(a). For FDSOI devices (Fig. 1(b)), the insulating buried oxide forms a thermal barrier on account of the low thermal conductivity of SiO_2 and impedes the heat transfer from the channel to the Si substrate underneath [3], [4]. On the other hand, the low thermal conductivity of ultra-thin top Si layers is another concern in FDSOI devices [5]. For FinFETs with vertically oriented fins (served as the channel) wrapped by the gate, as shown in Fig. 1(c), not only the complex 3D structures but also the physical confinements of Si fins play roles in the severer SHE. As shown in Fig. 2(a), since the fin becomes narrower and taller from 22 nm to 7 nm technology node [6]–[8], less self-heating in the channel could dissipate through the width direction and can only propagate into the substrate. In the real applications, multi-fins are paralleled for one transistor to obtain large drive current, which leads to the heat affecting each other from each fin, resulting in an extra temperature rise.

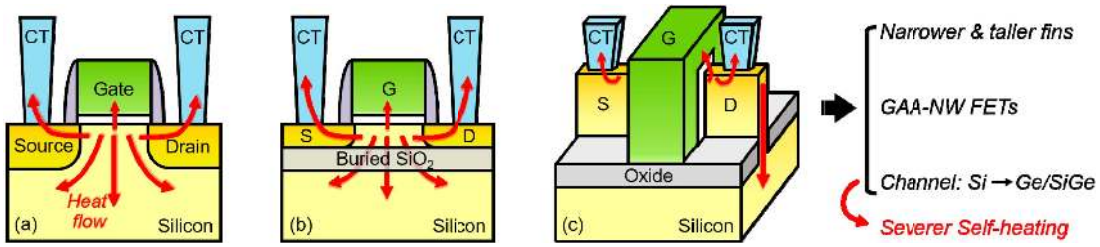

FIGURE 1. Evolution of transistors structures driven by aggressive scaling: (a) planar devices with bulk silicon substrates have outstanding heat dissipation ability congenitally. (b) MOSFETs on SOI substrates exhibit SHE due to the low thermal conductivity of the thin Si body and buried SiO_2 below. (c) three-dimensional FinFETs also suffer from SHE due to complicated constructions. Fin improvement, more complex architectures, and high mobility channel materials are proposed as candidates for continuous shrinking, yet all of these solutions seem to be still puzzled by SHE.

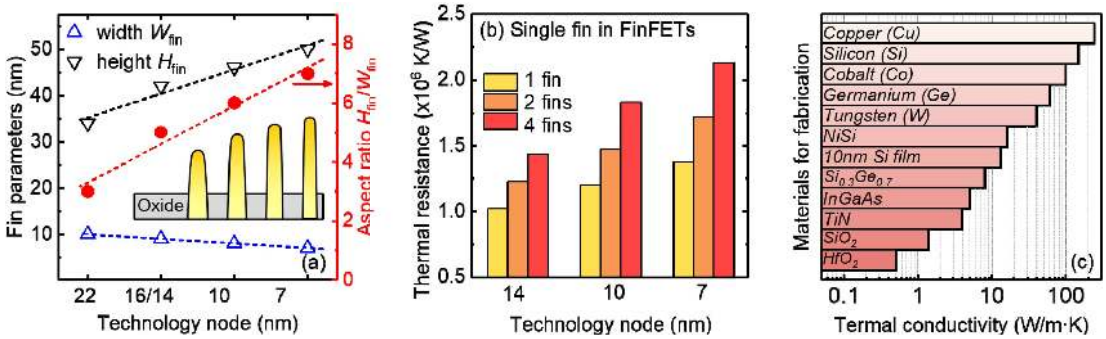

FIGURE 2. Trend of SHE related factors in further advanced nodes. (a) To suppress short channel effects and obtain better performance, the fin profile in FinFETs has been scaled to taller and narrower with higher aspect ratio, which results more physical confinements to spread the generated heat towards the source/drain region. (b) Larger thermal resistance per fin is expected with increasing number of fins from 14 nm to 7 nm nodes. (c) Thermal conductivities (at 300 K) of normal and emerging materials used in the fabrication of advanced nodes. Most of them have worse heat dissipation capability than bulk silicon.

On the other hand, as shown in Fig. 2(b) [9], the thermal resistance in the channel monotonically increases with the fin number and the improvement of node in FinFET technology.

As the promising candidate for aggressive sub-10 nm technology node, the GAA-NW device may have even severer SHE due to its ultra-small nanowire channel and strong phonon confinement [10], [11]. As for the potential alternative channel material with high mobility, Ge or SiGe also has a much lower thermal conductivity than Si, which may aggravate the SHE compared with the case of Si channel. Fig. 2(c) summaries the thermal conductivities of several materials adopted by the fabrication of advanced CMOS technologies [12]–[15]. From Fig. 2(c), it could be seen that the thermal conductivities of most materials are smaller than that of bulk silicon, even the recently proposed new interconnect metal material, Cobalt [6].

This undesirable SHE could first affect the electrostatic performance in terms of mobility, threshold voltage, saturation velocity and other physical parameters that are temperature dependent [16]. As a result, the drive current could be significantly influenced by the channel-temperature change due to SHE. Upon considering the device reliability, the local SHE is of potential concern for both interconnect reliability such as metal line's electron migration (EM) and transistor aging such as hot carrier injection (HCI) and bias temperature instability (BTI) [17]. Therefore, it is important to quantitatively characterize SHE and its impact of device reliability behaviors. Various techniques have been developed to evaluate the SHE, including quasi-DC, small-signal radio frequency (RF), heat sensor in layout, optical methods [3], [4], [18]–[20]. However, the experimental study of the real impact of SHE in the circuit operation case is still very limited. Recent literatures [21]–[23] have reported that self-heating may be mitigated under high-frequency operation in realistic uses. However, further study is still strongly needed to understand the impact of SHE in advanced technology nodes with new device structures and channel materials.

It has been reported that both the self-heat generation and dissipation are extremely fast, which are at the nanosecond scale [14]. It is necessary to develop speed-compatible electrical methodology to capture the fleeting SHE phenomena and understand the impact of SHE on the performance and reliability of device and circuits in real operation cases.

Recently, a novel ultra-fast measurement system has been proposed and demonstrated to experimentally characterize the SHE in aggressively scaled transistors with new device structures, using the electrical technique [24]. However, the quantitative impact of SHE on the parameter extraction and reliability degradations have not been comprehensively characterized, in spite of their importance to accurate modeling and reliability lifetime prediction. To address the above-mentioned issues, this paper aims to discuss if SHE will

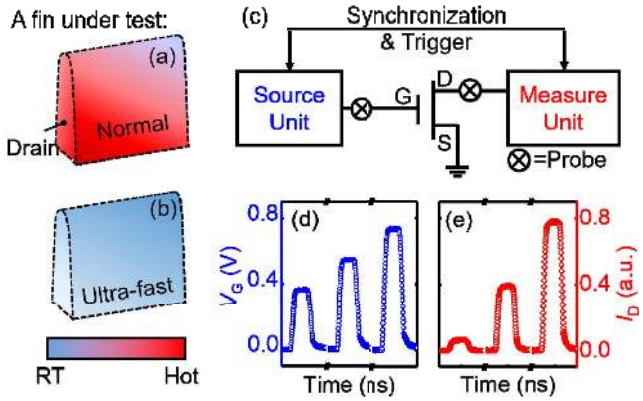

FIGURE 3. Contrast of fin thermal profiles under (a) normal and (b) ultra-fast characterization at the room temperature (RT). Slow speed makes the device under SHE while measurement. (c) Setup for the ultra-fast sub-1 ns electrical characterization. (d) and (e) Separately show V_G and I_D sequences picked from the I_D-V_G test.

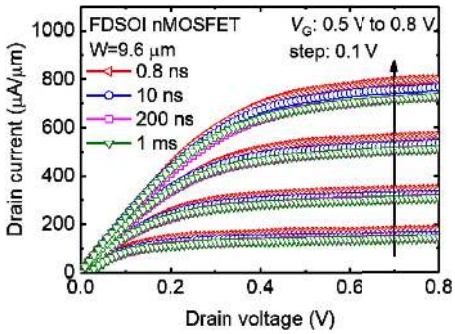

FIGURE 4. I_D-V_D characteristics of Si FDSOI MOSFET (L_G = 30 nm) measured at V_G ranging from 0.5 V to 0.8 V, using ultra-fast measurement system with four different speeds. With faster speed the transistors were less heated-up, which resulted in higher on-state current I_{on} due to the less phonon scattering.

be a serious problem in the aggressively scaled technology nodes with new device structures. The paper is organized as follows. Section II will introduce the developed sub-ns electrical characterization technique and compare the results under different measurement speeds regarding SHE. In Section III, extensive experimental results about accurate ballistic parameters extraction and dynamic transient SHE capturing with the ultra-fast measurements will be discussed. Moreover, the impact of SHE on the HCI reliability under real circuit speeds will be discussed as well.

II. EXPERIMENT SETUP

A. SUB-1 NS ELECTRICAL CHARACTERIZATION FOR TRANSISTORS

For transistors suffering from SHE, the most intuitive phenomenon during electrical characterizations is the drain current degradation after the devices switch from the off state to the on state. As summarized and reported in [17], the thermal time constant of FinFETs is on the order of nanoseconds. Thus, normal measurement tools such as traditional DC and commercial fast measurement units could not catch the self-heat process due to their limited measurement speeds. What's worse, the device might have been totally heated up and even already reached a thermal equilibrium state when the normal measurements are going on. Fig. 3(a) depicts an example of a single fin from a FinFET under normal measurement, which is suffering from SHE and its corresponding results are data with heating. To minimize and even avoid SHE generated exactly during the measurement itself, ultra-fast electrical characterization should be realized at the speed of sub-nanosecond. Thus, it will be possible to obtain accurate and intrinsic electrical parameters before the device performance is influenced by SHE, as the thermal profile depicted in Fig. 3(b).

Fig. 3(c) shows the schematic structure of setup for sub-1 ns electrical characterization based on the ultra-fast measurement system in [24], [25]. Here, the device under test (DUT) is designed for RF-level high-speed measurements. The gate voltage V_G and drain voltage V_D are supplied by the source unit, which can generate signals with a sufficiently short edge time of 20 ps. The measurement unit is able to sense the current change with a time-resolution of 1 ps. Signal synchronizations and triggers between the units have been realized by the communication protocol through the control bus in the system. Here, the applied V_G sequence and captured drain current I_D result during an I_D-V_G characterization are given as an example in Fig. 3(d) and (e), respectively.

B. SELF-HEATING IN TRANSISTORS WITH DIFFERENT STRUCTURES

Fig. 4 shows the electrical properties of short-channel n-type FDSOI device under four measurement speeds using the above system setup. FDSOI devices in this study were fabricated with the commercial CMOS technology. The thickness of Si layer in the adopted ultra-thin SOI wafer is within 10 nm and the buried oxide thickness is ~12 nm. Source/Drain were formed after implant and activation followed by epitaxially growth of raised S/D structure for a lower S/D resistance. Under the speed of 0.8 ns, the DUT is almost SHE free. And under 10 ns as well as 200 ns measurement speed, the DUT will suffer from the self-heating. And for the speed of 1 ms similar to the quasi-DC measurement, the DUT has already came to the thermal equilibrium. It could be observed from the Fig. 4 that the saturated on-current I_{on} increases with the increase of measurement speed, which could help alleviating SHE. The measurement process itself, especially that at a slow speed, has a direct impact on characterization results. It is experimentally confirmed that at a speed of sub-nanosecond, the measurement time is short enough for suppressing most of SHE.

The same speed-variant I_D-V_D characterizations were performed on 28nm bulk Si planar MOSFETs, bulk FinFETs and SOI FinFETs, respectively. The gate length L_G of planar devices is 30 nm, and the L_G of both bulk and SOI FinFETs is 20 nm. In order to compare the impact of SHE on device

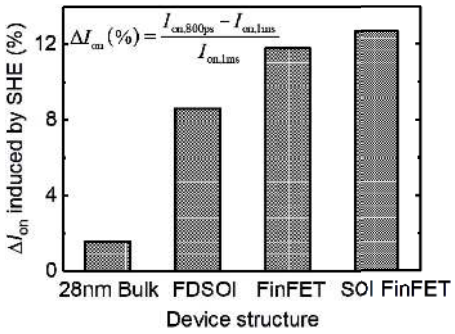

FIGURE 5. Contrast of ΔI_{on} induced by SHE in four different types of device structures. ΔI_{on} was calculated by comparing $I_{on,500\ ps}$ measured with a 800 ps speed and $I_{on,DC}$ measured with normal DC test. Planar bulk MOSFETs owing the best heat dissipation capability suffers the least SHE whereas SOI FinFETs being puzzled by the most SHE.

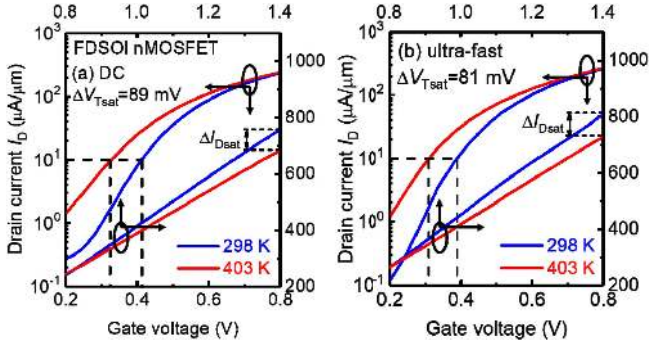

FIGURE 6. I_D-V_G characteristics of a FDSOI FET measured at 298 K and 403 K, using (a) normal DC system (b) ultra-fast measurement setup, respectively. The data from ultra-fast characterization exhibit very weak SHE thanks to the fast measurement speed. In (a), the measured $\Delta V_{Tsat} = 89$ mV, $\Delta I_{Dsat}/I_{Dsat} = 0.107$, while in (b), the measured $\Delta V_{Tsat} = 81$ mV, $\Delta I_{Dsat}/I_{Dsat} = 0.0875$.

performance, the criterion here is defined as the differences of I_{on} between data at 0.8 ns and 1 ms speed over the I_{on} at 1ms. As compared in Fig. 5, SOI FinFETs suffer from the most severe SHE while bulk Si planar MOSFETs suffer from the much less SHE, which is consistent with the expectation.

III. RESULT AND DISSCUSION

A. ACCURATE TRANSPORT PARAMETER EXTRACTION FOR TRANSISTORS

As mentioned above, I_D-V_G characteristic could also be influenced by the increased channel temperature caused by SHE, and exhibiting the difference between DC and ultra-fast characteristics. Then the extracted parameters such as the threshold voltage V_T and saturated drive current I_{Dsat} will be different, as the examples shown in Fig. 6. These inaccurate parameters will lead to an incorrect model and finally impact the circuit design.

For sub-100 nm MOSFETs, the drive current I_{Dsat} is proportional to the carrier injection velocity υ_{inj} and ballistic efficiency B_{sat}, or to be specific, $I_{Dsat} = W\upsilon_{inj}B_{sat}C_{ox}(V_G - V_T)$, where W is channel width, C_{ox} is the oxide capacitance, and V_T is the threshold voltage of the transistor [25]. Using the temperature dependent backscattering model, B_{sat} can be obtained from ratio of the near-equilibrium mean-free path λ_0 over the critical distance l_0 over which the potential drops by k_BT from the peak of the conduction band barrier, as illustrated in the Fig. 7(a). The ratio λ_0/l_0 can be extracted from the values of η and α using

$$\frac{\lambda_0}{l_0} = 4\left[\frac{1}{2} - \left(\alpha(T) + \frac{\eta(T)}{V_{GS} - V_T(T)}\right)\right]^{-1} - 2, \quad (1)$$

$$\alpha = \frac{\Delta I_{Dsat}(T)}{I_{Dsat}(T)\Delta T}, \quad (2)$$

$$\eta = \frac{\Delta V_{Tsat}(T)}{\Delta T}, \quad (3)$$

where η and α are defined to be the slopes of V_T shift ΔV_T and $\Delta I_{Dsat}/I_{Dsat}$ with respective to temperature T, respectively. It is related to B_{sat} as

$$B_{sat} = \frac{1}{1 + 2(l_0/\lambda_0)}, \quad (4)$$

For a MOSFET with fully ballistic transport, i.e., $B_{sat} = 1$, the carriers injected from the source end would not experience any scattering in the transistor channel.

Traditionally, the ballistic transport characterization was carried out by taking DC measurements at various temperatures to extract the temperature-dependent parameters α and η. However, due to the severe SHE, the dependency of ΔV_T and $\Delta I_{Dsat}/I_{Dsat}$ on the characterization temperature T would be greatly affected by the very long measurement time (millisecond scale). The channel temperature $T_{channel}$ may be much higher than the characterization temperature, leading to inaccurate α and η. In that case, λ_0 would be smaller due to higher phonon scattering in the heated channel, therefore, the value of λ_0/l_0 and B_{sat} would be smaller for a FinFET or FDSOI devices with SHE. To extract the accurate ballistic transport parameter for device modeling and circuit simulation, SHE or the measurement speed should be carefully taken into consideration.

Fig. 6(a) and (b) compare the I_D-V_G properties measured with normal DC and ultra-fast setup at 298 K and 423 K for a FDSOI device with $L_G = 50$ nm, respectively. Here, V_T is taken by constant current method and I_{Dsat} is taken at $V_G = V_T + 1.0$ V. It is obvious that the ΔV_T and ΔI_{Dsat} are not the same for the device measured at the two different characterization speeds. Consequently, the slope of ΔV_T and $\Delta I_{Dsat}/I_{Dsat}$ as a function of characterization T, which represent the values of α and η, would be different for the two cases. To analyze the impact of SHE on the characteristics of carrier ballistic transport, the DUTs was measured with various L_G ranging from 20 nm to 150 nm. For each device, the backscattering coefficients η and α were extracted using both characterization methods, respectively.

It should be noted that the effect of the T-variant series resistance R_{SD} was neglected in the above-mentioned

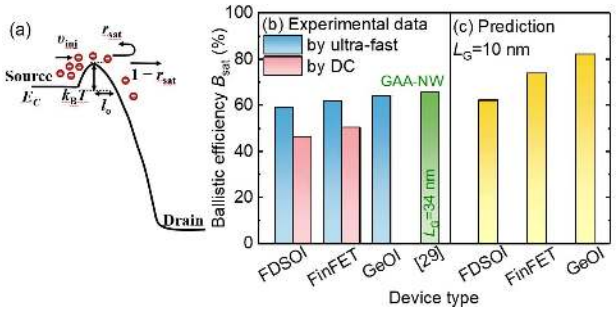

FIGURE 7. (a) A simplified schematic illustrates the ballistic transport model in the short-channel devices. (b) Comparison of R_{SD}-corrected ballistic efficiency B_{sat} of various devices in the advanced technology nodes, extracted by ultra-fast measurements (blue columns) and normal DC test (red columns). (c) Prediction of B_{sat} at $L_G = 10$ nm by numerical modeling fitted with the experimental data.

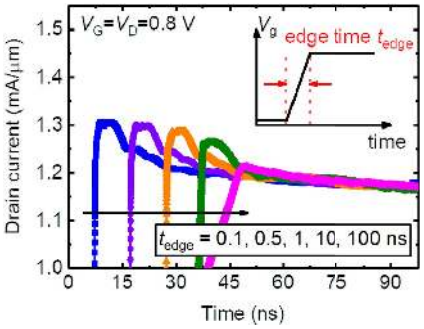

FIGURE 8. The gate voltage signals with different edge time t_{edge} ranging from 0.1 ns to 1 ms were applied on the 14 nm FinFETs, as shown in the schematic of inset. Corresponding transient I_D changes during the FinFETs operation were monitored with a time-resolution of 1 ps. The peak value is decreased as t_{edge} increases owing to the SHE during t_{edge}.

backscattering model. However, in the case of FinFET measurement, it cannot be ignored especially for devices with ultra-narrow fins connected directly to the S/D region with large volume. This is on account of the fact that the quantum contact resistance, which originates from the interface between the 3-D S/D regions and the low-dimensional quantum wire of S/D-extension regions, is sensitive to temperature [28]. Therefore, to be more accurate, the temperature dependent model was revised and provided in [28] in which a temperature dependence coefficient $\beta = \Delta R_{SD}/\Delta T$ is included to take account of the R_{SD} effect. For instance, β of FinFETs in this study is reported as 0.591 Ω/K from [29]. Based on the corrected backscattering model, the R_{SD}-corrected B_{sat} was found to be obviously higher than the un-corrected one.

To investigate the trend of ballisticity for devices in the future technology nodes, three kinds of devices with various L_G ranging from 20 nm to 150 nm were compared in this study. The 20 nm FinFET in [29], 30 nm FDSOI devices in [30], and 50 nm GeOI devices in [31] were used for comparison. The scalability model of B_{sat} was established based on the following derivation. It is known that B_{sat} is proportional to λ_0/l_0 and

$$l_o = \frac{k_B T}{q\varepsilon(0^+)}, \tag{5}$$

where $\varepsilon(0^+)$ is the electric field profile near the source end, and therefore is proportional to $1/L_G$. As a result, B_{sat} could be correlated to L_G as $B_{sat}^{-1} \propto L_G$. Fig. 7(b) shows the experimentally extracted B_{sat}, for all three kinds of devices. The GAA-NW device with $L_G = 34$ nm has a higher B_{sat} of 0.65 due to its outstanding electrostatic properties [28]. The B_{sat} of the three kinds of device with different gate lengths ranging from 20 nm to 200 nm was extracted using the parameters extracted by the ultra-fast measurement. Based on the above numerical model, it could be anticipated that the B_{sat} with less SHE would reach 0.73 for Si FinFETs and 0.86 for GeOI MOSFETs at $L_G = 10$ nm node when using the ultra-fast measurement. According to Lundstrom's theory, for an unchanged gate bias, a higher B_{sat} indicates a higher I_{Dsat}. Therefore, higher B_{sat} is important for reducing power consumption in IC circuits, and accurate B_{sat} characterization is quite essential for accurate circuit modeling and design.

B. SHE-INDUCED TRANSIENT TEMPERATURE CHANGE IN CHANNEL

In this part, we will show the captured process of SHE generation and dissipation in short-channel FinFETs and explain how to extract the dynamic heat generation time and dissipation time. Furthermore, the transient temperature change in the channel will be discussed in both FinFETs and bulk planar devices.

Si FinFETs with multiple fins fabricated in a commercial foundry fab were used in the characterization and simulation. In order to ensure no SHE-induced temperature rise during switching from the off state to on, the V_G pulse with different edge time t_{edge} from 0.1 ns to 100 ns was used, as shown in the inset of Fig. 8. All of the five I_D responses have the apparent rush right after turning on and then gradually decrease, which could be attributed to the carrier transport degradation caused by the SHE. Another point needs to be clarified is the difference of the rushes in I_D, for both amplitude and shape. It could be observed from Fig. 8 that the peak value of I_D pulses with $t_{edge} = 0.1$ ns and 0.5 ns are the same and both are slightly larger than that with $t_{edge} = 1.0$ ns. This indicates that $t_{edge} = 1$ ns is not fast enough and a tiny amount of SHE has been generated during the edge of 1 ns. It also implies that 0.5 ns of a faster measurement speed is suitable for obtaining the almost SHE-free I-V characteristics. This measurement speed is much faster than the limit of conventional semiconductor parameter analyzers.

When considering the process of heat dissipation, the off state time of the V_G pulse was changed to control the amount of dissipated thermal. The t_{edge} of each V_G pulse keeps at 20 ps and the on state time holds sufficiently long to make the FinFETs being heated up totally and reach to the state of thermal equilibrium. For the case of pulses with the long

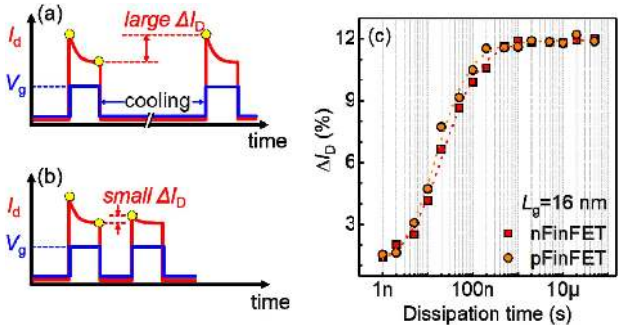

FIGURE 9. Schematic waveforms of V_G-t and the corresponding response of I_D-t under (a) long cooling time (off state) and (b) short cooling time. (c) Experimental data of the ΔI_D increases for longer cooling time in n- and pFinFETs. Long Enough cooling time gives the device more opportunities to cool down and the peak I_D will be larger when next pulse coming.

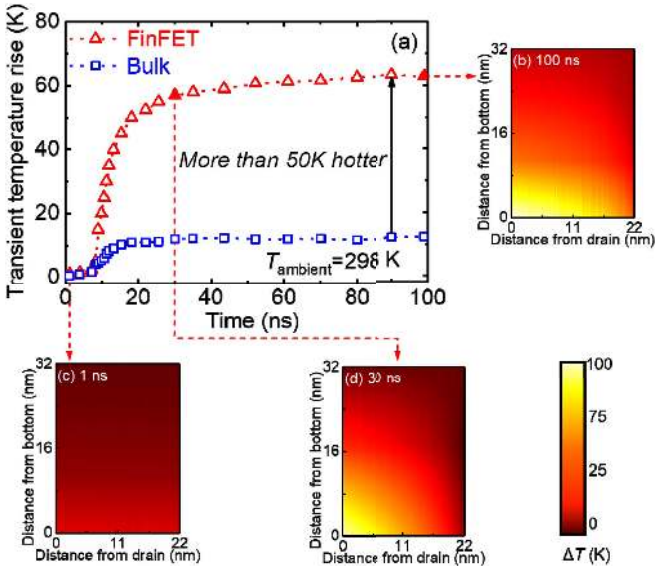

FIGURE 10. (a) Extracted experiment data of transient channel temperature after the device switching on. For FinFET devices, around 60 K will be elevated and about only 10 K rising for planar bulk devices to reach the SHE stable status. (b) Transient temperature profiles of a fin after switching on for 100 ns. (c) Extremely weak SHE makes negligible temperature rise after 500 ps. (d) SHE has already obviously strong and severe just after 30 ns.

cooling time, as shown in the Fig. 9(a), the whole SHE generated in the on state has been dissipated and the device was fully cooled down to the ambient temperature. When next pulse comes, the I_D goes to the peak value without any SHE, resulting in a large ΔI_D. However, for the pulses with the short cooling time, I_D cannot go to the peak value, as shown in the Fig. 9(b) because the self-heating dissipation during the off-state is insufficient. Different dissipation time was designed from nanosecond to microsecond, as shown in Fig. 9(c). It could be found that it takes around 1 μs to thoroughly dissipate the heat from SHE, for both p- and n-FinFETs. Another key point is that most part of heat was dissipated during the first 100 ns in the off state.

For device and circuit simulations, the real-time or transient channel temperature $T_{channel}$ is very critical to establish a precise transient model. With DC measurements, it is impossible to itself could introduce heating, as confirmed above. In this work, by measuring I_D with a V_G pulse of t_{edge} = 20 ps at various chunk temperature, the unique relationship between I_D and $T_{channel}$ was correlated. It is supposed that $T_{channel}$ should be the same as the chunk temperature until the current reaches the peak. With this I_D-$T_{channel}$ relation, the time evolution of $T_{channel}$ after the DUTs turning on could be clearly depicted, as shown in Fig. 10. For bulk FinFETs, the temperature increase is around 60 K and for bulk planar Si MOSFETs (L_g = 30 nm) it is only around 10 K. And the thermal time constant of the SHE can be in the range of 10-20 ns.

Sentaurus simulation [32] also confirms the above results, as shown in Fig. 10. The temperature profile of a single fin was simulated at four moments after switching from the off state to on state. It could be clearly observed that the FinFET device has already suffered from the SHE after 30 ns. And the temperature in the channel, especially at the drain side of the transistor begins to increase after 1 ns, which should be attributed to more phonon scattering occurs at the near side of drain.

Since, in real circuits, transistors switch on and off at a higher frequency than 1 GHz. If the operation frequency is high enough and the time of on state is shorter than the heat generation time and the time of off state is longer than the heat dissipation time, the device might suffer from few SHE. There are also several published results obtained from the thermal image showing no significant self-heating [19], [20] in a multi-GHz running IP block, also supporting this conclusion.

C. IMPACT OF SHE ON TRANSISTOR AGING RELIABILITY

BTI and HCI are two main degradation mechanisms in transistors and play their roles in the different situations of circuit operations. For modern MOSFETs working in the digital circuits, considerable BTI mostly deteriorates transistors when only V_G (no V_D) is applied at the off state. However, the devices experience the most severe HCI during the transitions of V_G and V_D signals, usually at the maximum I_D. And the channel is exactly heated up during this switching event when the current flows. HCI degradation has been attracting much more attention due to the emerging severe SHE in advanced technology nodes. Since HCI has a strong temperature dependence, SHE has significant impact on HCI in short-channel devices. As elaborated in part B, the heat generation process is quite fast, whereas the heat dissipation is relatively slow. Therefore, the HCI stress voltage waveforms, especially the period and duty cycle will have a strong impact on the HCI-induced device degradation.

In this study, different waveform patterns of V_G/V_D were applied to the short-channel FinFETs in the stress phases to explore the impact of SHE on HCI. As shown in Fig. 11, two traditional stress patterns, DC and AC stress with 5 GHz

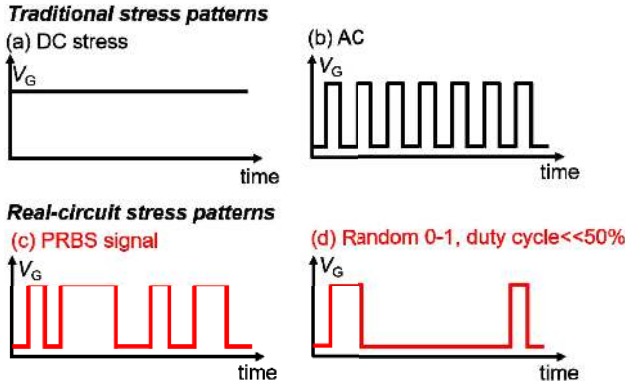

FIGURE 11. Four gate stress patterns (DC, AC, PRBS and random 0-1 stress) were used to accelerate the HCI acceleration. Different stress patterns introduce various amount of SHE and then assess the impact of SHE on HCI degradation.

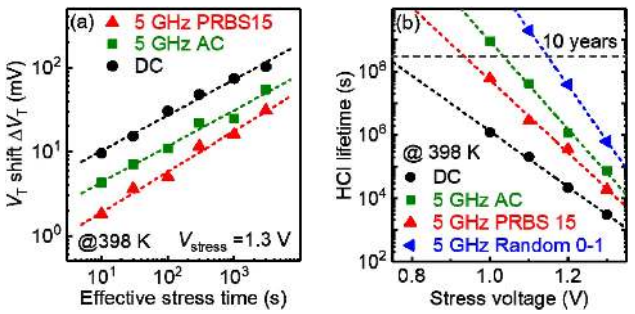

FIGURE 12. (a) Comparison of ΔV_T changing as a function of effective stress time with various DC, AC, PRBS stress, using ultra-fast measurement. The stress voltage is V_{stress} = 1.3 V and measured at 398 K. (b) HCI lifetime is also predicted as a function of stress voltage for the four different stress patterns. The random 0-1 signal with 10% duty cycle and same 5 GHz frequency as others has the fewest SHE and longest HCI lifetime.

frequency were applied on the gate, respectively. Here, to investigate HCI-induced device degradation at the real circuit operation case, 5 GHz 2^{15}-1 bits pseudo-random binary sequence (PRBS) signals and 5 GHz random 0-1 signal with 10% duty cycle were adopted to mimic the random circuit operation. Each bit of the stress waveform patterns is 200 ps. The stress voltage was $V_G = V_D = 1.1$ V and V_T was monitored after each stress phase. The accelerated results are shown in Fig. 12(a). It could be observed that much more HCI degradation was generated by the DC stress after the same effective stress time, compared with that by 5 GHz AC and PRBS stress. In addition, PRBS stress could induce more degradation than AC stress even at the same frequency. This is presumably attributed to the possibility of more continuous "1" bits in the PRBS stress, which have stronger SHE. Fig. 12(b) compares the prediction of HCI lifetime under four kinds of stress patterns. For the 5 GHz random 0-1 stress with only 10% duty cycle, which is similar as the situation in some part of the real circuits. The HCI stress lifetime is much larger than the 5 GHz PRBS and AC stress with 50% duty cycle. It indicates that although there exists severe SHE in FinFETs, and the impact of SHE on HCI reliability in real circuits is strongly depend on the real voltage waveforms applied to the device.

IV. CONCLUSION

SHE phenomenon and its impacts in advanced technology nodes have been quantitatively investigated with the sub-1 ns characterization technique. The SHE-induced transient I_D shift and channel temperature change have been successfully extracted. And the HCI-induced device degradation at the circuit speed has also been characterized to explore the influence of SHE on reliability behaviors. It could be expected that the SHE and its impact on device's performance and reliability may be alleviated under the GHz circuit operation in further advanced technology nodes.

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