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Impact of Solder Degradation on V_{CE} of IGBT Module: Experiments and Modeling

Yingjie Jia, Yongle Huang, Fei Xiao, Hongfei Deng, Yaoqiang Duan, *Student Member*, *IEEE*, and Francesco Iannuzzo, *Senior Member*, *IEEE*

***Abstract*—Solder degradation is one of the main packaging failure modes in insulated gate bipolar transistor (IGBT) modules, which is usually evaluated through the change of thermal resistance. However, due to the strong electro-thermal coupling in IGBT module, solder degradation also affects electrical characteristics, such as on-state voltage V_{CE}. The impact mechanism of solder degradation on V_{CE} is analyzed in this paper firstly. For the study of the solder degradation independently, a press-packing setup is designed for the accelerated aging test, which can remove the influence of bond wires degradation and significantly improve the experimental efficiency. Then, the IGBT equivalent resistance is defined, which conforms to Ohm's law in calculation and can respond to the dynamic current in real time. So, it could be conveniently used in the finite element method-based simulation. Meanwhile, a realistic 3D degradation model of solder layer is constructed by image processing method. Furthermore, an electro-thermal coupling model based on finite element is constructed to study the impact of solder degradation on the electrical and thermal characteristics of IGBT. Finally, the proposed degradation mechanism is verified by simulation and experimental results.**

***Index Terms*—Insulated gate bipolar transistor (IGBT), solder degradation, failure modes decoupling, electro-thermal model**

I. Introduction

INSULATED gate bipolar transistor modules (IGBTs) are the most widely used fully controlled power electronic device in the power electronic system. With the rapid development of equipment technology, the reliability requirements for IGBTs in various applications are getting more and more strict [1, 2]. The failure of IGBT modules is usually associated with packaging failure modes, such as bond wires fatigue and solder layers degradation [3]. Due to the complicated working environment of IGBTs, various fatigue failure modes of IGBT packages are usually co-existing and coupling [4]. So it is very difficult to study one specific failure mode independently with the influence of other failure modes isolated. Nowadays, simulation and experiment are the main methods to study the failure of the IGBT module. Therefore, it is crucial to the evaluation of reliability for IGBT modules to study specific failure modes with the help of realistic simulation models and reasonable experiments.

The reliability of IGBTs is closely associated with the thermo-mechanical fatigue of solder layers (die-attach solder and substrate solder). Since IGBTs are vertical devices, the solders are supposed to provide efficient thermal conduction path and the die-attach solder also provide electrical conduction path additional [3]. The degradation of solder layers causes an increase in junction-to-case thermal resistance R_{th_jc}, reduce the heat dissipation performance of the IGBT module, and raise the junction temperature T_j only to result in thermal runaway of IGBT chips finally [5]. So the fatigue phenomena occurring in the solder layers cannot be neglected. Many scholars have studied the failure of solder layers. Ref. [6-9] studied the solder degradation through finite element method (FEM), but the simulation method for degradation is so ideal that cannot meet the reality very well. In the accelerated aging experiments [10-12], failure modes other than solder layers are not easily excluded, which makes the experimental results difficult to be interpreted accurately. A method for evaluating the health of solder layers from the transient cooling curves at a specific time window is proposed in [13], but it requires accurate T_j measurement (ms level). In addition, in terms of packaging failure evaluation, thermal parameters, such as R_{th_jc}, are usually used to characterize solder layers degradation [14], while electrical parameters, such as on-state voltage V_{CE}, are used to evaluate bond wires [15, 16]. IGBTs are temperature sensitive devices so that there is a strong coupling between electrical and thermal characteristics. Thus, the degradation of solder layers will also affect electrical characteristics [3, 14]. However, the mechanism of its impact has not been clearly explained.

For simulation technology, FEM is a numerical method based on structure and material, which can overcome the limitations of experimental conditions and has become a widely used method in simulation modeling, structural design optimization and reliability analysis for IGBT modules [17]. However, the solution to electric field in FEM simulation software conforms to Ohm's law. IGBT, as a semiconductor device, is essentially different from the linear conductor, which brings inconvenience to FEM-based simulation. In [18, 19], the power losses of IGBT is expressed as a function of current, voltage, temperature and frequency, which acts as the heat

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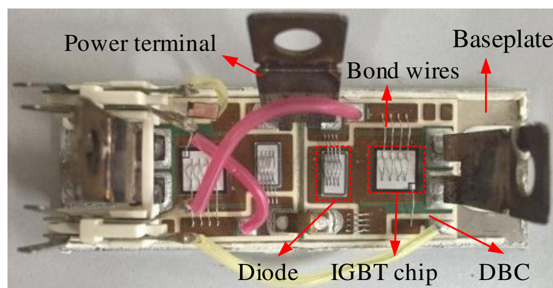

Fig. 1. Geometry of the studied IGBT module.

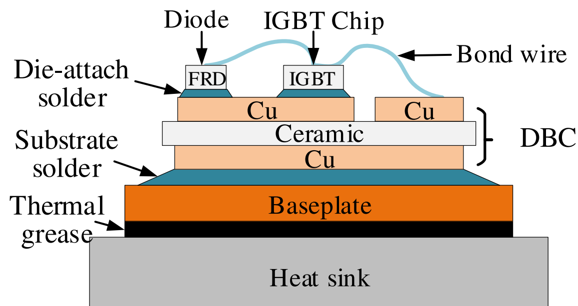

Fig. 2. Cross-sectional diagram of typical multilayer IGBT module.

source for electro-thermal coupling simulation, but this method cannot simulate the electrical characteristics of IGBT. Ref. [20] obtained the forward characteristics of IGBT through the experiment at different temperatures, and constructed a look-up table for junction temperature prediction. However, it is difficult to be applied in FEM because of the absence of exact expression. Based on some idealized assumptions, the electrical conductivity of IGBT is expressed as a linear function of temperature in [21], but it is only suitable for a constant current. However, the current load of IGBT is variable so this method is limited. A novel electro-thermal co-simulation method based on PSpice and Icepak is proposed in [22], which can solve the electrical and thermal characteristics of IGBT simultaneously, but the model is complex, computationally inefficient and difficult to run for a long time.

This paper aims to study more advanced FEM simulation model and experimental method to study the impact of solder degradation on the electro-thermal characteristics of IGBT, especially the on-state voltage V_{CE}. This paper is structured as follows: In section II, the impact mechanism of solder degradation on V_{CE} is analyzed and summarized in detail at first. Section III introduces a specialized experimental method to study solder degradation, and power cycling tests are carried out for the mechanism validation. Section IV proposes an electro-thermal model for IGBT based on FEM, including the simulation principle, the definition of IGBT equivalent electrical conductivity and a realistic 3D degradation model of the solder layer. Section V is a summarization of the paper.

II. Impact Mechanism Of Solder Degradation On V_{CE}

A. Information about the Studied IGBT Module

In order to illustrate the impact of solder degradation on V_{CE}, a case study of a 1200 V/50 A commercial IGBT module is given in this paper. The studied IGBT module adopts typical welded package structure, of which internal structure is shown in Fig. 1. The module includes two IGBT chips and two diode chips, which are configured as a half-bridge. The chips are welded on a standard DBC layer through die-attach solder layers, which is further welded to a copper baseplate. Aluminum bond wires are connected with the chips and the copper layer by ultrasonic welding. The structural distribution of the cross section is shown in Fig. 2.

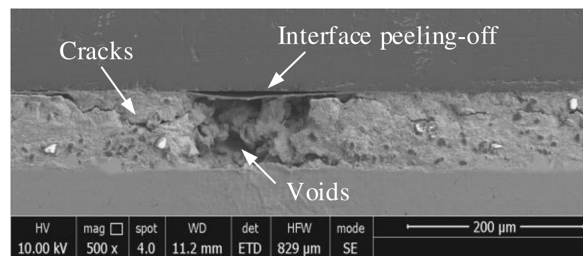

Fig. 3. Morphologies of die-attach solder after power cycling.

B. Analysis of Impact Mechanism

Existing studies shown that the degradation of solder mainly includes three forms: voids, fatigue cracks and interface peeling-off, which can be attributed to the cyclic disturbance of thermal stress and the mismatch of material properties [23]. The existence of voids is inevitable, even in the prime state when IGBT module packaged. Voids not only affect the heat dissipation performance of the IGBT module, but also cause stress concentration under cyclic thermal loads, which will lead to the initiation and propagation of cracks at the edge of voids. Interface peeling-off is an extreme phenomenon of cracks growth, and the chip-solder interface is characterized as the brittle material with high yield strength, low ductility and low toughness, which owns good resistance to thermal stress but low resistance to thermal shocks. Therefore, this phenomenon can often be observed under the condition of short-term strong heat shock. Fig. 3 shows a scanning electron microscope (SEM) image of die-attach solder from an IGBT module that is cut longitudinally after the power cycling, from which three typical degradation phenomena mentioned above can be observed simultaneously.

In fact, voids, cracks and fatigue-induced interface peeling-off all can have detrimental effects on dissipating devices. The degradation of solder layers will reduce the effective heat transfer area and increase the thermal resistance R_{th_jc} of IGBT module, which can significantly increase the junction temperature T_j of an IGBT or a diode, as shown in (1). Furthermore, since the heat flow within an IGBT module is almost one-dimensional, when there are relatively large defects in the solder layers, the heat must flow around them by generating a large local temperature gradient, which will reduce the heat dissipation performance of the module. Moreover, the die-attach solder provides both thermal and electrical conduction path simultaneously, so the degradation of which will also cause inhomogeneous current sharing, thus aggravating the problem of uneven temperature distribution of chips.

$$R_{th_jc} = \frac{T_j - T_c}{P_{loss}} \Rightarrow T_j = R_{th_jc} \times P_{loss} + T_c \qquad (1)$$

Where P_{loss} and T_c are the power loss and the case temperature of the IGBT module.

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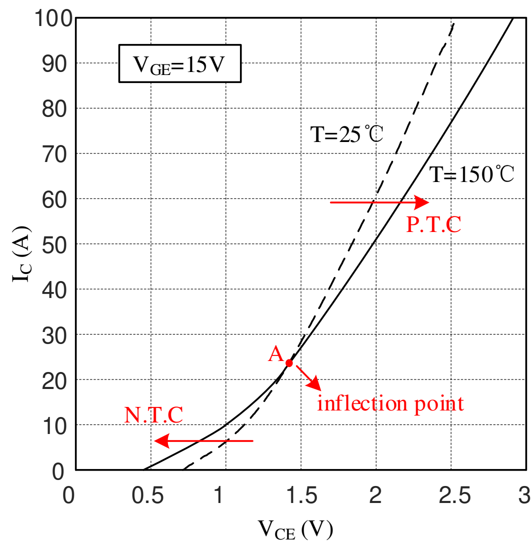


Fig. 4. Forward characteristics of the studied IGBT at typical temperatures.

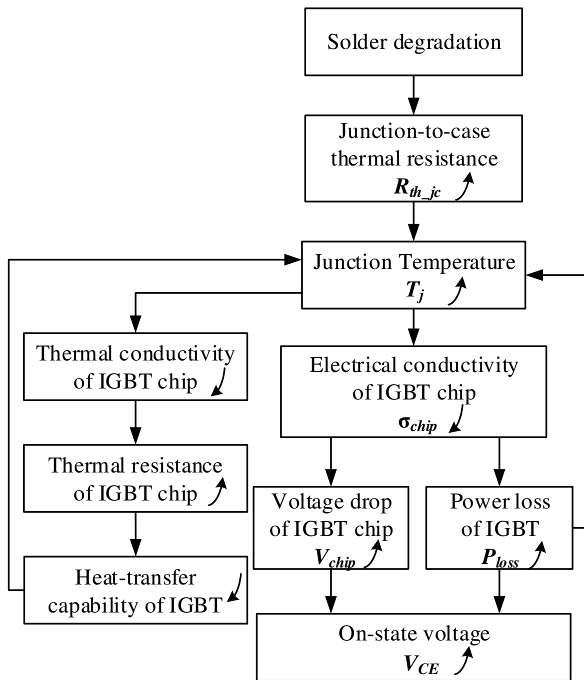
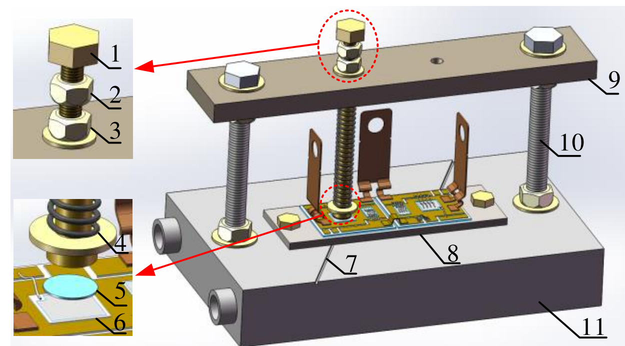


Fig. 5. Impact mechanism of solder degradation on V_{CE}.

To monitor thermal failure due to solders degradation, a 20% growth in R_{th_jc} is usually defined as the failure threshold for IGBT modules. However, it is well known that many electrical parameters of IGBT are strongly coupled with temperature, such as threshold voltage V_{th}, transconductance K_P, carrier diffusion coefficient $D_{n,p}$, carrier mobility $\mu_{n,p}$, etc [24]. Therefore, electrical and thermal characteristics of IGBT are also coupled. For the forward characteristic, on-state voltage V_{CE} is a function of T_j and collector current I_C when gate-emitter voltage V_{GE} is fixed, which can be described by

$$V_{CE} = f(T_j, I_C) \quad (2)$$

The forward characteristics of the studied IGBT at typical temperatures is shown in Fig. 4. The inflection point A is a common feature of an IGBT device when characterized at multiple temperatures. A negative temperature coefficient



1. Pressure bolt; 2. Clamp nut; 3. Limit nut; 4. Spring; 5. Molybdenum plate; 6. IGBT chip; 7. Thermocouple installation slot; 8. IGBT module; 9. Support plate; 10. Support bolt; 11. Water cooler.
Fig. 6. Press-packing setup for power cycling test of solder degradation.

(NTC) influences the characteristic below the point A, whereas a positive temperature coefficient (PTC) influences the characteristic above the point A. With the increase of temperature caused by solder degradation, the electrical conductivity characteristic of the IGBT will change, which can be described with the electrical conductivity of IGBT chip σ_{chip}. Power cycling tests generally operates at high current beyond rated value, and the impact of solder degradation on V_{CE} is positively correlated at this time. That is, V_{CE} will raise with the increase of T_j. Meanwhile, power losses will also increase and T_j would be further aggravated, which is a positive feedback process.

In addition, the temperature dependence of packaging materials cannot be ignored. In normal working temperature range of IGBT, the thermal conductivity of Al, Si, Cu are negatively correlated with temperature [19]. For example, the thermal conductivity of silicon chip can be expressed by (3) [25]. In other words, the increase of junction temperature will raise the thermal resistance of IGBT chips, which reduces the heat transfer ability and leads to heat accumulation in chips. This is also an important factor of V_{CE} increases due to solder degradation in accelerated aging tests. Fig. 5 is a summary about the impact mechanism of solder degradation on V_{CE}.

$$\lambda_{Si} = 24 + 1.87 \times 10^6 \cdot T^{-1.69} \quad W \cdot m^{-1} K^{-1} \quad (3)$$

III. Experimental Method And Mechanism Verification

A. Experimental Setup

As explained previously, various fatigue failure modes of IGBT packages are usually co-existing and hard to be decoupled, which leads to difficulty of correctly interpreting the results of power cycling. That is, the typically applied failure criteria as V_{CE} increase by 5% or R_{th_jc} increase by 20% very often do not reveal the real root causes [13]. Therefore, in order to study solder degradation independently, it is necessary to remove the influence of bond wires. For this purpose, a press-packing setup is designed and the structural design principle is shown in Fig. 6.

The setup consists of an epoxy resin support plate, two support bolts, a specially designed Cu pressure bolt with spring and several latex gaskets. The studied IGBT modules are removed bond wires firstly and fixed on the water cooler. The

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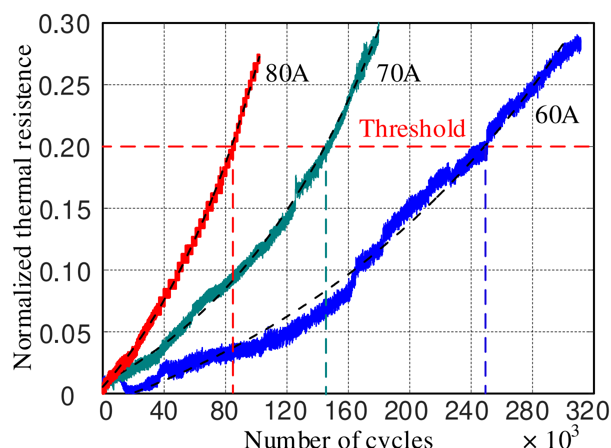
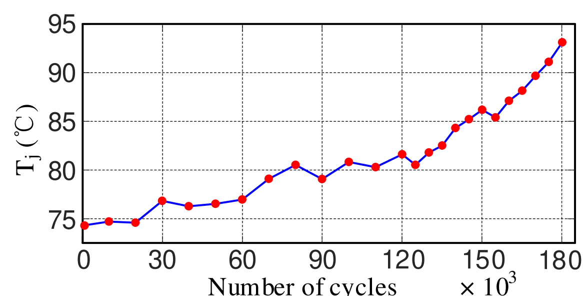


Fig. 7. Normalized junction-to-case thermal resistance of IGBTs during power cycling at cycling current of 60A, 70 A and 80 A.

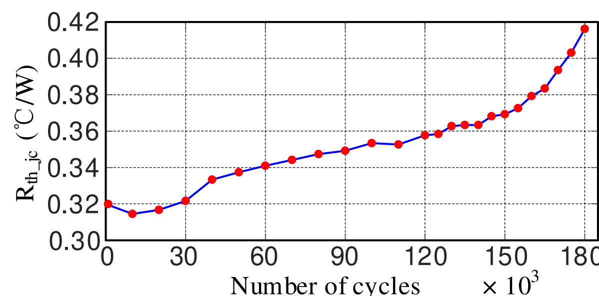
support plate is fixed with the water cooler through two support bolts. The pressure bolt is used to replace bond wires and connect with IGBT chip, which also acts as the electrical contact for the emitter terminal of the studied IGBT module. The pressure bolt is equipped with two nuts, one for providing pre-tightening force through compress the spring and the other for providing a position limit to the pressure bolt. A molybdenum plate is placed between IGBT chip and pressure bolt to provide good electrical contact and reduce thermal mismatch between them. The control of the pre-tightening force provided by the spring is an important work. The thermal stress inside the die-attach solder during power cycling is usually about several dozen MPa [26]. Through adjusting the compression length of the spring to adjust the pressure loaded on the chip surface, which is controlled below 0.25 MPa here. Therefore, the setup will not damage the chip and will not affect the study of solder failure mechanism. In addition, the power terminals and the gate bond wire remain unchanged and the packaging structure of the studied IGBT module was not changed too much. Through this setup, we could not only eliminate the influence of bond wires degradation, but also test several samples simultaneously, thus significantly improve the experimental efficiency and reduce the cost.

B. Power Cycling Test

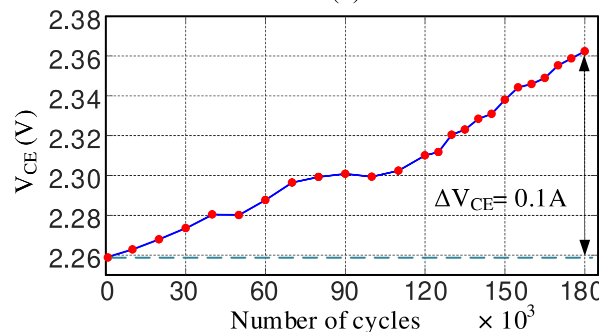
In order to verify the proposed mechanism, power cycling (PC) tests were used for the studied 1200V/50A IGBT modules using the press-packing setup. The cycling current I_C was limited as a fixed value of 60A, 70A and 80A, respectively, which is used to heat IGBT modules and cause degradation. The heating time and cooling time were both fixed at 1 s (t_{on}/t_{off} = 1s/1s). The junction temperature T_j during PC test was measured across the method of temperature sensitive electrical parameters (TSEP) at a low current of 100 mA. The calibration curves $T_j = f(V_{CE})$ for the studied IGBT modules were measured before PC test firstly. Package degradation caused by PC tests does not affect the calibration curve, which has been proved through experiments in [15]. The case temperature T_C was measured by thermocouples arranged at the bottom of the IGBT chip, and the on-state voltage V_{CE} was also measured during the cycling.



(a)



(b)



(c)

Fig. 8. Steady-state values of PC test under condition of 70A cycling current and measured at 50A test current. (a) Junction temperature T_j. (b) Junction-to-case thermal resistance R_{th_jc}. (c) On-state voltage V_{CE}.

The junction-to-case thermal resistance R_{th_jc} is a steady-state parameter, which should be measured after IGBT reaches thermal equilibrium. Therefore, the real-time measured thermal resistance in PC test is called quasi-thermal resistance R_{th_qua} here. In order to evaluate the degradation of solder through the criterion of thermal resistance increase by 20%, the measured R_{th_qua} was normalized to $\Delta R_{th_qua} / R_{th_qua_0}$, where the $R_{th_qua_0}$ is the initial value of R_{th_qua}. The experimental results are shown in Fig. 7. Exponential functions were used to fit the experimental data, similar laws can be found that R_{th_qua} increases nonlinearly with the number of cycles. The cycling current I_C shows a great influence on the cycles that IGBT reaches the failure threshold, that is, the greater I_C, the faster failure rate of solder. This is because the increased current will cause higher junction temperature fluctuation, which will cause the solder layer withstand greater thermal stress and accelerate the degradation.

The change of steady-state thermal resistance R_{th_jc} during PC tests were obtained by interval measurement. The power cycling is paused at intervals and the current I_C is switched to the constant rated current of 50A. Then, the on-state voltage V_{CE}, junction temperature T_j and case temperature T_c are measured

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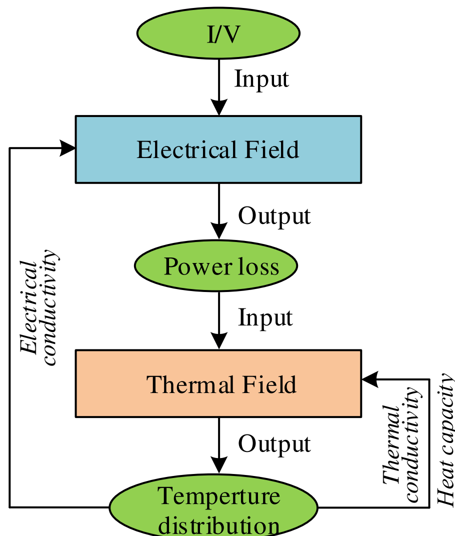

Fig. 9 Simulation principle of the FEM electro-thermal model.

respectively, thus R_{th_jc} can be obtained by (1). Fig. 8 shows the measurement results for the PC condition of 70A cycling current. In Fig. 8(a), T_j increases with the degradation of solder, which is similar to R_{th_jc} shown in Fig. 8 (b). Fig. 8 (c) clearly shows the impact of solder degradation on V_{CE}. At the end of 180,000 cycles, V_{CE} increased by about 0.1 V, which is a 4.42 % increase for the initial value 2.26 V. It should be noted that the use of the press-packing setup inevitably brings additional resistance, which leads to the measured on-state voltage of IGBT module is higher than the actual value. Therefore, the failure criterion of V_{CE} increase by 5% is no longer applicable here, but it does not affect the analysis about the change of V_{CE}. In the implemented PC tests, due to the effect of pressure spring, the IGBT chip and the pressure bolt are closely linked, so the change of V_{CE} can be attributed to the solder degradation totally.

IV. Finite Element Modeling And Simulation Analysis

In this section, a FEM electro-thermal model for studying solder degradation is introduced in details, including the simulation principle, the calibration of the equivalent electrical conductivity for IGBT chip and the 3D degradation model of solder layer based on X-ray image. Next, the impact of solder degradation on the electrical and thermal properties of IGBT are studied.

A. Simulation Principle of Electro-Thermal Model

Power losses will occur in IGBT when conducting current, and the temperature of IGBT module increases because of joule heating effect. In FEM simulation, the power loss is calculated firstly by solving electric current field under the given initial conditions, as shown in (4) [21]. Then the temperature distribution is calculated in thermal field, which is fundamentally governed by the diffusion convection-reaction partial differential equation (PDE) given as (5) [19]. Material properties, such as electrical conductivity, thermal conductivity, heat capacity, etc. have strong dependence on the temperature, thus affecting the calculation of electric and temperature field. Therefore, the heat transfer problem and the electrical problem must be solved simultaneously in order to accurately find the temperature and current distribution.

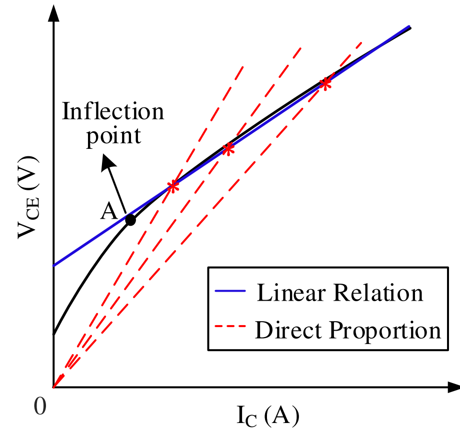

Fig. 10 Conversion of linear relation to direct proportion for R_{CE_equ}.

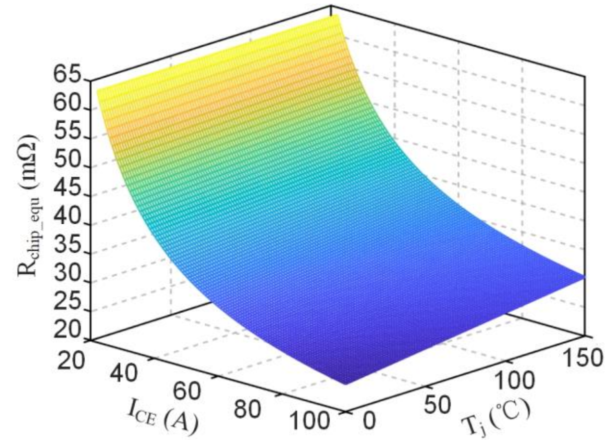

Fig. 11 The relationship between R_{chip_equ}, T_j and I_C of the studied IGBT.

$$Q_j = \nabla \cdot J = \nabla \cdot \sigma(-\nabla V) \quad (4)$$

$$\nabla \cdot (\lambda \cdot \nabla T) + \frac{\partial q}{\partial t} = \rho c_p \frac{\partial T}{\partial t} \quad (5)$$

where J is current density, V is the potential, T is temperature, q is the heat flux. ρ, σ, λ and c_p are the density, electrical conductivity, thermal conductivity and specific heat capacity of materials, respectively. The simulation principle of the established FEM electro-thermal model for IGBT is shown in Fig. 9. With the constantly updated temperature, the equivalent electrical conductivity of the IGBT chip is cycle recalculated and the real-time power loss can be obtained at the same time. Thus, the bidirectional coupling of electric field and thermal field can be realized.

B. Equivalent Electrical Conductivity of IGBT Chip

The calculation method to electric current field in FEM is generally based on Ohm's law, that is, the current is proportional to the voltage. However, the electrical characteristics of IGBT are essentially different from linear conductors. Meanwhile, the chip electrical conductivity σ_{chip} is not equivalent to that of chip material. Therefore, it is necessary to calibrate the parameter σ_{chip} of IGBT, which needs to satisfy both the forward characteristics of IGBT and the algorithm of Ohm's law.

The forward characteristics of the studied IGBT can be obtained from the datasheet, as shown in Fig. 4. As mentioned

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earlier, V_{CE} is a function of temperature and current. A detailed discussion on forward characteristic above the inflection of the studied IGBT module has been presented in [27], and the obtained analytic expression can be described as

TABLE I
RESISTANCE PARAMETERS OF EACH SECTION IN CIRCUIT

Section	Resistance (mΩ)
Collector power terminal	1.2904
Copper layer (collector to die-attach solder)	0.0889
Die-attach solder	0.0021
Al metallization of IGBT chip	1.0077e-4
Bond wires	1.0018
Copper layer (bond wires to emitter)	1.3812e-3
Emitter power terminal	1.2952
Sum up R_{bond}	3.6679

$$V_{CE} = (k \cdot T_j + b) \cdot I_C + c \qquad I_C > I_A \tag{6}$$

Where T_j is junction temperature of IGBT chip, I_C is collector current, I_A is the current at inflection point, k, b and c are fitting coefficients, respectively.

It is noted that the inflection point current I_A of the studied IGBT is about 22 A, and the current used in PC test is usually higher than it, so (6) can be applied to most PC tests. As shown of the blue solid line in Fig. 10, the fitted *V-I* curve is a continuous piecewise function when the temperature is fixed, which reflects the general linear relationship between V_{CE} and I_C, but not the direct proportion that fits Ohm's law. For any point on the solid line, connect it to the original point and then a series of straight lines could be plotted, as shown by red dotted lines in Fig. 10. The intersection of the dotted lines and the solid line reflects the actual forward characteristics of IGBT device. Meanwhile, the dotted lines can make V_{CE} and I_C conform to the proportional relationship, that is, Ohm's law. The set of all dotted lines slopes (V_{CE}/I_C) are defined as R_{CE_equ} in this work, which is called the equivalent resistance of IGBT and can be represented as

$$R_{CE_equ} = k \cdot T_j + c/I_C + b \qquad I_C > I_A \tag{7}$$

It is noted that the *V-I* curves are obtained by measuring the voltage between the power terminals, so the R_{CE_equ} in (7) is not the equivalent resistance of the IGBT chip. The on-state voltage of the IGBT module is the sum of voltage drop of the IGBT chip and the internal connections, such as the power terminals, copper layers and bond wires [28]. A detailed geometry of the studied IGBT module was created in a CAD program and further imported to the software ANSYS/Q3D [29]. Then, the corresponding resistance parameters of circuit sections (from the collector power terminal to the emitter power terminal) are extracted, as shown in Table I. Then, the equivalent resistance of IGBT chip R_{chip_equ} can be expressed as (8), where R_{bond} is the sum of all the resistance in the circuit except the chip. Fig. 11 is the visualization for (8).

$$R_{chip_equ} = k \cdot T_j + c/I_C + b - R_{bond} \qquad I_C > I_A \tag{8}$$

Fig. 11 reflects the mathematical relationship among the equivalent resistance of IGBT chip R_{chip_equ}, collector current I_C and junction temperature T_j, which conforms to the actual forward characteristics of the IGBT. Furthermore, R_{chip_equ} is equal to the ratio of voltage and current in numerical calculation, which obeys Ohm's law. Finally, the equivalent conductivity of IGBT chip σ_{chip} for FEM simulation can be obtained as

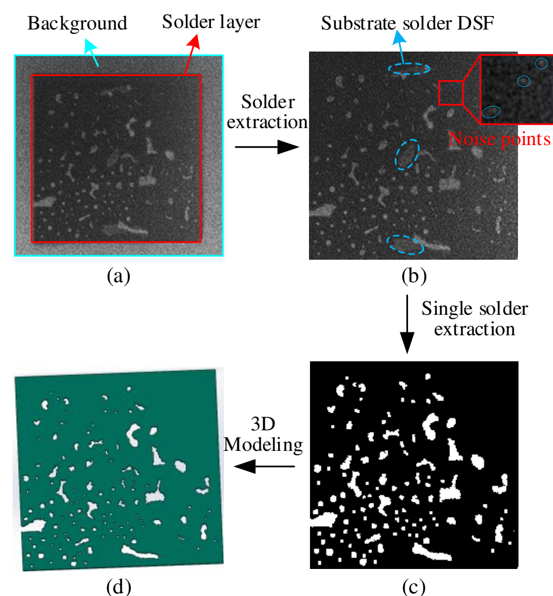

Fig. 12 Process of 3D modeling for the degraded solders. (a) Original image from X-ray. (b) Solder profile with noise and DSF. (c) Binary image of die-attach solder. (d) 3D geometric model of die-attach solder.

$$\sigma_{chip} = \frac{d}{S \cdot R_{chip_equ}} \tag{9}$$

Where d and S are the chip thickness and area of the studied IGBT module.

C. 3D Degradation Model of Solder Layer

In terms of the FEM-based simulation for solder degradation, it is necessary to create a detailed geometry model of the solder layers containing degraded structure features (DSF), such as voids and fatigue cracks, which can be obtained from the X-ray machine. As shown in Fig. 12(a), the degraded solder layer of the studied IGBT module under the condition of 70A cycling current was observed after the PC test. However, for 3D modeling that needs to consider structural details, the original image has the disadvantages of low contrast, noisy signal and blurred defect edge for which is hard to be used directly. Aiming at this point, a multi-platform-based modeling method for the degraded solder layer is introduced.

The process of this work can be shown in Fig. 12. First, the original gray image obtained by X-ray is imported to MATLAB, and according to the difference of gray value between the solder layer and the background, the regions belonged to solder can be distinguished and extracted, as shown in Fig. 12(b). Some noise points could be found in the image, and DSF of both die-attach solder and substrate solder exist simultaneously. The noise points are eliminated by means of wavelet enhancement. In addition, X-ray attenuates with the increase of penetration thickness, which results in the gray value of substrate solder DSF on image lower than that of die-attach solder. Therefore, the die-attach solder can be distinguished from the substrate solder by gray threshold segmentation, and the DSF of the two layers can be extracted separately. In this way, a binary image only containing the DSF of die-attach solder is shown in Fig. 12(c). Next, an important procedure is to extract the contour

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TABLE II
LAYER COMPOSITION AND THICKNESS OF THE STUDIED IGBT MODULE

Layer	Material	Thickness(μm)
Metalization	Al	6
IGBT chip	Si	150
Die-attach solder	SnAgCu	85
DBC copper	Cu	300
Ceramic	Al_2O_3	380
Substrate solder	$Sn_{63}Pb_{37}$	50
Baseplate	Cu	3000

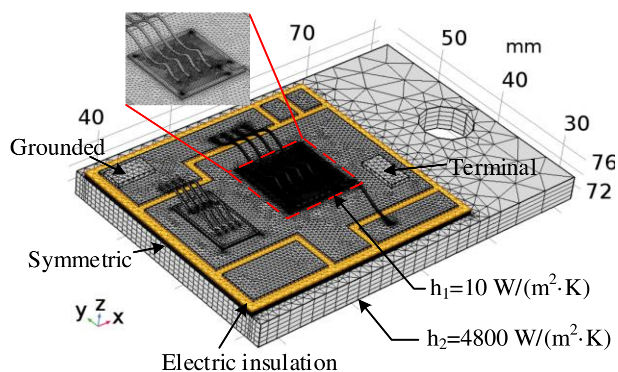


Fig. 13 Meshing and boundary conditions of the FEM model.

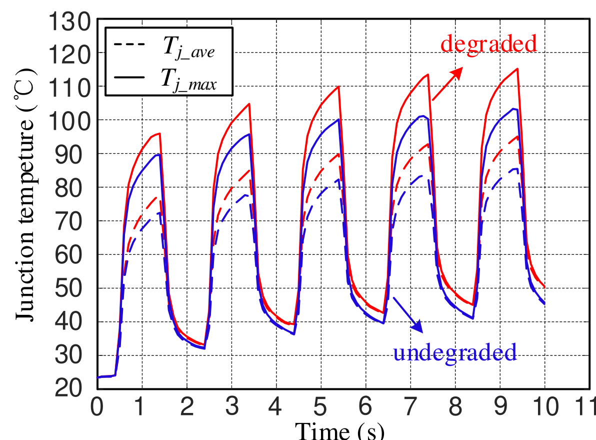
data of degraded solder layer from the acquired binary images and further convert them into AutoCAD readable form [30]. Then the contour shape of solder layer containing DSF can be obtained.

For the geometry of solder layers, the transverse and longitudinal dimensions are quite different. For example, the area of the die-attach solder layer is 9×9 mm^2, while the thickness is only 90 μm. Besides, it is well known that the degradation in transverse direction of solder layers, such as the size of defect structures, void ratio, etc., are the main factors affecting the heat transfer performance of IGBTs [3, 8, 9]. For these reasons, the transversal DSF are considered primarily in this work. Finally, the 3D degradation model of the solder layers for FEM simulation is completed in SolidWorks, as shown in Fig. 12(d). The results shown that the established model can truly reflect the situation of the degraded solder layer.

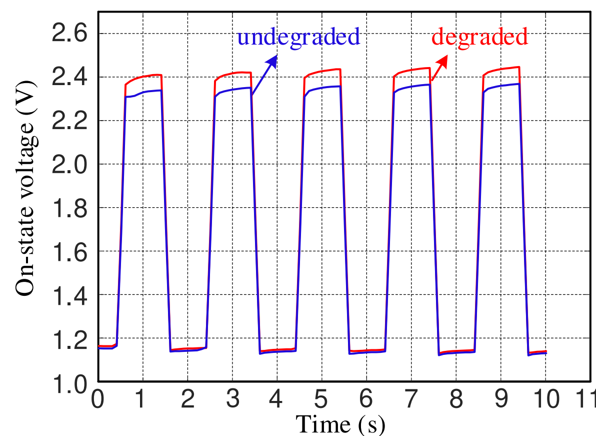
D. Electro-thermal Coupling Simulation and Analysis

In order to better understand the experimentally results in the PC tests as well as further study and verify the impact mechanism of solder degradation on V_{CE}, the electro-thermal coupling simulation was carried out using the FEM software COMSOL Multiphysics. As is clear previously, the theory and regarded geometry combined compose a complicated problem. Thanks for the optimized multi-physical field coupling algorithm, the bidirectional coupling between electric field and temperature field shown in Fig. 9 can be implemented in the simulation platform efficiently.

FEM is a kind of numerical method based on structure and material. To ensure the accuracy of structural parameters, a Device Under Test (DUT) is longitudinally dissected after the PC test. Then, the thickness parameters of layers are extracted by the SEM, as shown in Table II. Just as shown in Fig. 9, temperature dependence of materials is crucial for the electro-thermal coupling simulation. The thermal conductivity λ_{chip} and electrical conductivity σ_{chip} of IGBT chip can be defined



(a)



(b)

Fig. 14 Transient simulation results of junction temperature and on-state voltage at 70A cycling current. (a) Junction temperature T_{j_max} and T_{j_ave}. (b) On-state voltage V_{CE}.

according to (3) and (9), respectively. For the parameters of other layers used in the simulation, such as electrical conductivity, thermal conductivity, heat capacity and so on, can be obtained from the COMSOL material library. In order to improve simulation efficiency, only half of the geometric structure of DUT is modeled, while the other half is equivalent by symmetric boundary conditions. For the same reason, the heat transfer structures (including thermal conductive silicone grease, water-cooled plate and air) below the baseplate are not modeled, but are equivalent with a lumped heat transfer coefficient of 4800 W/(m^2·K), which can be calibrated through a series of steady-state experiments under different current loads. In addition, due to the silicone gel is removed from the IGBT module, a heat transfer coefficient of 10 W/(m^2·K) is used to simulate the natural convection. Besides, radiation is neglected and the ambient temperature is set as 23.5 ℃. The meshing and boundary conditions of the FEM model are shown in Fig. 13.

Two simulations are carried out for studying the impact of solder degradation, of which the simulation conditions are identical except the geometrical structure of solder layer. To highlight the impact of solder degradation on the electro-thermal characteristics of IGBT, the solder layers in the first simulation are set to be ideal, that is, no defects occurred. In the

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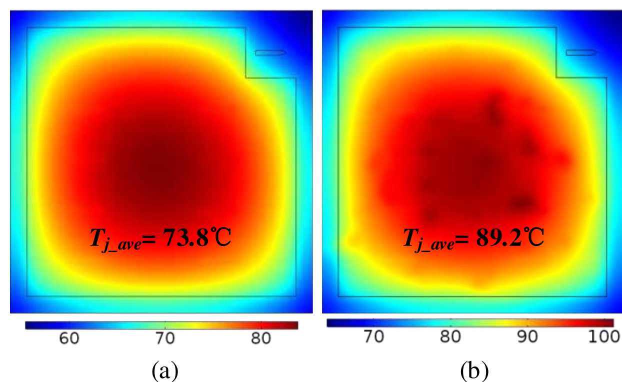
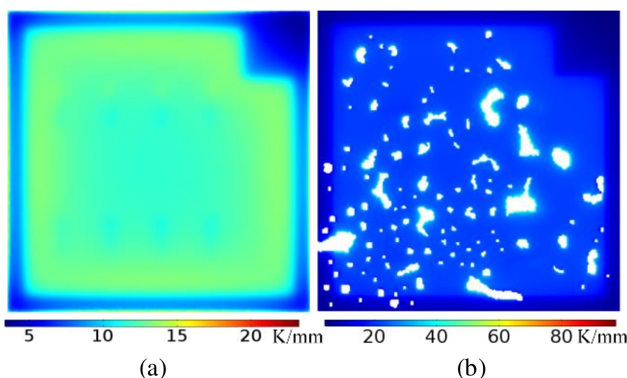


(a) (b)

Fig. 15 Steady-state simulation results of IGBT chip temperature distribution carried out at 50A test current. (a) Without solder degradation. (b) With solder degradation.



(a) (b)

Fig. 16 Steady-state simulation results of temperature gradient in solder layers carried out at 50A test current. (a) undegraded solder. (b) Degraded solder.

second simulation, the used solder layers correspond to the real structure of the DUT at 180,000 cycles of the PC test (70 A cycling current), which are modeled in the method shown in Fig. 12. A power cycling is simulated firstly and the applied current load is a series of square waves with the peak value of 70A, which is consistent with the previous PC test (t_{on}/t_{off}= 1s/1s).

The junction temperature T_j of the chip and on-state voltage V_{CE} are extracted, as shown in Fig. 14. It can be found in Fig. 14(a) that the IGBT has almost reached steady state after 5 cycles. The degradation of solder layers leads to the increase of T_j, and the difference between maximum temperature T_{j_max} and average temperature T_{j_ave} reflects the uneven temperature distribution inside the chip. In the twice simulations, the structure of solder layers is the only variable, so the V_{CE} change in Fig. 14(b) can be attributed to the increase of T_j caused by solder degradation. Due to the used current load belongs to the P.T.C region of the studied IGBT, so the increase of T_j leads to the raise of V_{CE}, which is consistent with previous experimental results. For the same reason, V_{CE} increases gradually during the heating stage of each power cycle, which proves that the established model can accurately simulate the electro-thermal coupling effect of IGBT.

Then, just as the experiment operated early, steady-state simulations under 50A current are also carried out and the temperature distribution of the IGBT chips are derived, as shown in Fig. 15. It can be found that the solder degradation further aggravates the uneven temperature distribution of the chip while causing the T_j to rise. As the previous mechanism

TABLE Ⅲ
COMPARISON OF SIMULATION AND EXPERIMENT RESULTS

Condition		T_{j_ave}(℃)	R_{th_jc}(℃/W)	V_{CE}(V)	ΔV_{CE}(V)
Simulation	Undegraded	73.8	0.297	2.02	0.07
	Degraded	89.2	0.402	2.09	
Experiment	Undegraded	74	0.32	2.26	0.1
	Degraded	93.5	0.416	2.36	

analysis, when there are relatively large defects in the solder layer, heat must flow around them by generating a large local temperature gradient, which can be clearly observed in Fig. 16.

Table Ⅲ is the comparison of steady-state results between simulation and experiment. In this work, the normalized parameter ΔV_{CE} is used to evaluate the impact of solder degradation on the on-state voltage of the IGBT module. It can be found that ΔV_{CE} caused by solder degradation is slightly below 0.1 V, in which the simulation is 0.07 V and the experiment is 0.1 V, while the difference between experiment and simulation reaches over 0.2 V. It is noted that the use of the press-packing setup introduced inevitably additional parasitic resistance, including the resistance of the pressure bolt and the molybdenum plate, as well as the contact resistance, which causes the measured initial V_{CE} in experiment is higher than the actual value of the original module. Under this press-packing condition, the introduced resistance, especially contact resistance, has a great influence on V_{CE} but it is difficult to measure accurately [31]. For this point, the parameter V_{CE} cannot be used to characterize solder degradation here. However, for both the simulations and experiments, the V_{CE} change is only caused by solder degradation. Therefore, the parameter ΔV_{CE} rather than V_{CE} is used to characterize the impact of solder degradation on the on-state voltage of the IGBT module in this work.

In general, there is a good agreement between the simulation and experimental results. The simulation results show that the degradation of solder leads to the increase of V_{CE} from the initial 2.02 V to 2.09 V, which is about 3.47%. This corresponds to the end of the PC test at 180,000 cycles, as shown in Fig. 8. At this time, the solder has exceeded the failure threshold of 20% growth in R_{th_jc}. It shows that with the aggravation of solders degradation, the impact of which on V_{CE} change cannot be ignored anymore. Meanwhile, the necessity of decoupling analysis for different failure modes is also confirmed. In practical applications, V_{CE} is an important parameter used to reflect the degradation of bond wires. With the help of the proposed simulation and experiment methods, it is hopefully to study the impact of solder degradation and bond wires degradation on V_{CE} separately, and the contribution of them to V_{CE} can be calculated quantitatively. Then, based on the change of V_{CE}, the fatigue state of solder layers and bond wires could be evaluated simultaneously.

V. CONCLUSION

The impact mechanism of solder degradation on the V_{CE} was analyzed in this paper, and a new type of press-packing setup was designed to study the degradation of solder layers. The setup can decouple different failure modes, thus eliminating the effect of bond wires degradation. Meanwhile, a finite element electro-thermal coupling model was proposed, which can

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reflect the defect structure features of the degraded solder layers more accurately. Using the flexibility of the simulation model can overcome the limitation of the experimental means and further study the failure mechanism. The proposed mechanism analysis was validated by the simulation and experimental results. The proposed experimental and simulation methods are general, which provided powerful means for the reliability study of solder layers and suitable for other types IGBT modules and other working conditions.

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