Impact of Strained-Si Thickness and Ge Out-Diffusion on Gate Oxide Quality for Strained-Si Surface Channel n-MOSFETs

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***Abstract*—Surface channel strained-silicon MOSFETs on relaxed $Si_{1-x}Ge_x$ virtual substrates (VSs) have been established as an attractive avenue for extending Si CMOS performance as dictated by Moore's law. The performance of a surface channel Si n-MOSFET is significantly influenced by strained Si/SiO_2 interface quality. The effects of Ge content (20, 25, and 30%) in the VS and strained-Si thickness (6, 5.5, 4.7, and 3.7 nm) on the strained Si/SiO_2 interface have been investigated. The interface trap density was found to be proportional to the Ge content in the VS. Fixed oxide charge density reduces to a lower limit at higher strained-Si thickness for any Ge content in the VS, and the value increases as the strained-Si thickness is reduced. There is a high concentration of interface trap charge and fixed oxide charge present for devices with a strained-Si channel thickness below 4.7 nm. To investigate the effect of strained Si/SiO_2 interface quality on MOSFET devices fabricated using a high-temperature CMOS process, the performance of surface channel n-MOSFETs has been correlated with channel thickness. It is noted that the drain–current rapidly decreases at low gate voltages for channel thicknesses less than 4.7 nm. The performance of both MOS capacitors and MOSFETs degraded below a strained-Si thickness of 4.7 nm irrespective of the Ge content in the VS even up to 30%. TCAD simulations have been carried out to analyze the effect of strained Si/SiO_2 interface on electrical characteristics. Performance degradation in thin strained-Si channels is primarily attributed to gate oxide quality. The out-diffused Ge accumulates at the strained Si/SiO_2 interface, introducing a significant amount of interface traps and fixed oxide charges during thermal oxidation. Interface trap density and fixed oxide charge density significantly increased when the Ge concentration at the surface becomes more than 6%. This paper suggests that a minimum strained-Si layer thickness of $\sim$ 5.0 nm is required to achieve a good strained Si/SiO_2 interface quality for surface channel strained-Si n-MOSFETs, fabricated using a high thermal budget CMOS process.**

***Index Terms*—Channel thickness, fixed oxide charge, gate oxide quality, Ge out-diffusion, SiGe virtual substrate, strained-Si, surface channel, thermal budget, trap charge.**

Manuscript received June 23, 2005; revised November 21, 2005. This work was supported by the Engineering and Physical Sciences Research Council (EPSRC). The review of this paper was arranged by Editor G. Groeseneken.

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Digital Object Identifier 10.1109/TED.2006.872086

I. Introduction

Surface channel strained-silicon (strained-Si) MOSFETs on relaxed $Si_{1-x}Ge_x$ virtual substrates (VS) seem to be gaining popularity as the next step in extending the Si CMOS platform because of enhancements of in-plane mobility of both electrons and holes compared to bulk Si [1]–[4]. A thin epitaxial film of silicon grown on a relaxed SiGe VS will conform to the larger lattice spacing of SiGe and will experience biaxial tensile strain. The magnitude of strain in the silicon layer increases with Ge content in the VS provided the strained-Si layer is thinner than the critical thickness h_c [5]. Improved device performance over bulk Si has been reported in strained-Si n- and p-MOSFETs [6]–[8]. Recently, strained-Si devices have also been proven to be scalable [9] and n-MOSFETs with gate lengths down to 25 nm have shown 15%–30% performance enhancement over bulk Si. While performance gains over bulk Si are impressive, the overall theoretical predictions for strained Si/SiGe MOSFETs are yet to be achieved in real devices [3]. By increasing the amount of Ge in the VS, and therefore increasing the strain, higher device performance is theoretically possible. However, such performance gains are often not realized due to the deleterious effects of strain relaxation, surface roughness, alloy scattering in high Ge-content material, and interface quality between strained-Si and gate oxide [10], [11].

The strained-Si thickness is a crucial parameter in this very sensitive design space. If a strained-Si layer is grown above critical thickness, the strain in the epitaxial layer may relax during high-temperature CMOS processing and misfit dislocations are formed. These misfit dislocations are effective carrier scattering sites, which will degrade device performance. In addition, if substantial strain is lost from the Si layer through misfit dislocations, carrier mobilities will also decrease due to strain loss. Apart from that, if the channel is too thick, Ge content in the VS and mobility enhancement are unnecessarily conservative [12]. On the other hand, if the channel is too thin, the strained-Si layer may be unable to contain the inversion layer charge, leading to an increase in carrier scattering and a loss of device performance. Conventional oxidation techniques for thermally grown oxide layers on a Si substrate typically involve the consumption of a significant amount of Si during the fabrication process. In addition, there is an additional Si consumption due to various other processing steps such as cleaning and etching. Finally, high thermal budget device fabrication gives rise to

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Ge diffusion from the SiGe VS, which effectively reduces the Si channel thickness. Any Ge reaching the strained Si/SiO_2 interface significantly degrades gate oxide properties, resulting in an increase in interface state density $(D_{\rm it})$ and fixed oxide charge density (Q_f/q), which degrade device performance.

One of the key considerations in fabricating strained-Si channel devices is the interface quality between the strained-Si layer and the gate oxide, since its robustness is vital for performance enhancement and relies on the integrity of the strained layer structure. This is especially important in SiGe MOS technology, where a low thermal budget process is necessary to avoid Ge diffusion at the strained Si/SiO_2 interface. Consequently, many researchers have fabricated strained Si/SiGe devices using reduced thermal budget processing [13]–[16]. The quality of this dielectric is, however, poorer than that of the thermal oxide. Moreover, previous n-MOSFETs, fabricated using reduced thermal budgets, were long-channel devices [15], [16]. Reducing the thermal budget of the process could be an option to avoid Ge diffusion, but may also lead to an unacceptable increase in device parasitics mainly visible for short channel devices, which will offset the advantages gained by the high mobility channel. Therefore, high thermal budget processing may be an alternative to control parasitic resistances that become increasingly important for short channel devices [4], [11].

There are only few reports available on the impact of Ge diffusion and strained-Si layer thickness on device performance. Currie *et al.* [16] have reported mobility data for n-MOSFET devices having surface channel thickness below the critical thickness, but the devices were fabricated using reduced thermal budget. Fiorenza *et al.* [17] have studied strained-Si MOSFETs with silicon thicknesses below and above the critical thickness to understand the maximum strained-Si thickness limitation, and these were fabricated using a high thermal budget. Strained-Si MOSFETs with Si films beyond their critical thickness have little loss of mobility enhancement but greatly increased OFF-state leakage current [17]. The impact of surface Si layer thickness on device performance was predominantly investigated for p-MOSFETs having a strained SiGe buried layer [18], [19]. Kwa *et al.* [20] have investigated the impact of Si cap layer thickness on dual-channel n-MOSFET devices. The performances of devices having channel thickness below 7 nm show a considerable increase in gate oxide charge and interface trap density.

Therefore, to enable successful commercialization, new issues that were not examined during the early phases of strained-Si technology development for surface channel strained-Si n-MOSFET devices must be studied. In this paper, we report the effect of strained-Si channel thickness and Ge content in the VS on the strained Si/SiO_2 interface to investigate the limitations on the strained-Si channel thickness for surface channel n-MOSFET devices, fabricated using a high thermal budget.

II. Experimental

Strained-Si MOS capacitors and MOSFETs were fabricated on relaxed $Si_{1-x}Ge_x$ VSs with $x = 0.2, 0.25,$ and 0.3. The relaxed SiGe VSs were grown on graded buffer layer. A grading rate of 10% Ge/μm was employed for the graded buffer layer on which constant composition VSs were grown. The VSs were of 1-μm thickness and B-doped to 5×10^{17} cm^{-3}. The VSs were grown at 650 °C by ultralow pressure CVD (ULCVD) in a modified MBE system [21]. Strained-Si cap layers of 6.0-, 5.5-, 4.7-, and 3.7-nm thicknesses were grown on top of the relaxed $Si_{1-x}Ge_x$ layer, as shown in Fig. 1. The strained-Si layer growth temperature was 550 °C. The initial thickness of the strained-Si layer was specified to allow for the consumption of approximately 6.0 nm during processing. Transmission electron microscope (TEM) analyses were carried out to verify the strained-Si layer thicknesses of a fully processed device. Fig. 2(a)–(c) shows the cross-sectional TEM images of the thermally grown gate oxide on a strained Si/$Si_{1-x}Ge_x$ substrate. The strained-Si layer thickness was 6.0 nm and the gate oxide thickness was 6.5 nm as measured from TEM images.

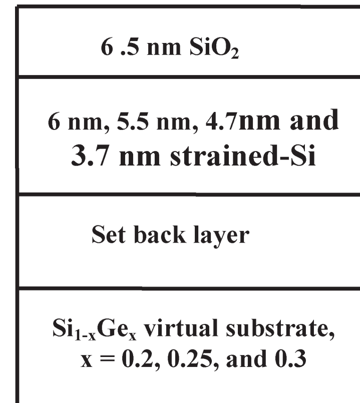


Fig. 1. Schematic diagram of the layer structure after device processing.

Strained-Si MOSFET devices were fabricated using a high thermal budget CMOS technique. The gate oxide was thermally grown at 800 °C for 1 h, resulting in approximately 6.5 nm gate oxide. Post-oxidation annealing was carried out in N_2 ambient at 800 °C for improving the quality of the strained Si/SiO_2 interface. Polysilicon was deposited for the gate electrode implanted with P and annealed at 800 °C for 30 min, arsenic was implanted into the source and drain through a thermally grown oxide and annealed at 1050 °C for 20 s. The MOSFETs studied here have a gate dimension of 2.0 μm $\times$ 10 μm (length $\times$ width), and capacitors have a dimension of 100 μm $\times$ 100 μm. Capacitance–voltage (C–V), conductance–voltage (G–V), and drain–current gate voltage $(I_{\rm ds} - V_{\rm gs})$ characteristics were measured using an HP 4284A LCR meter and an HP 4155A pico-ammeter, respectively.

III. Results and Discussion

Raman spectroscopy is usually used to verify the strained state of the epitaxial layers. In the present study, Raman spectroscopic experiments were performed on processed devices, and the Raman shifts of the Si–Si vibrational mode in strained-Si are plotted in Fig. 3 as a function of Ge composition in VS. Fig. 3 shows that following device processing, the intended

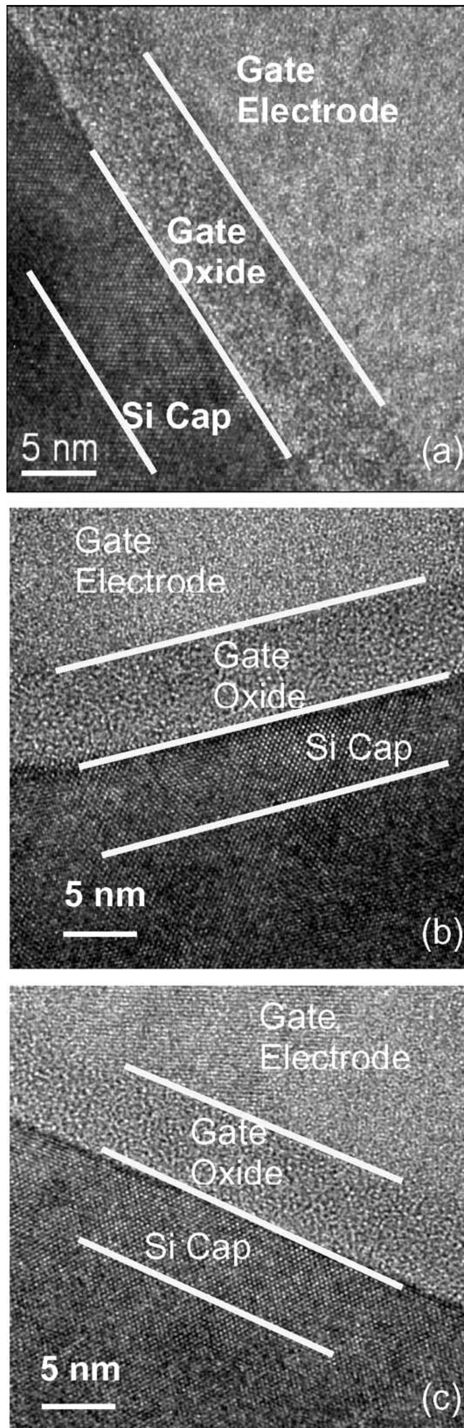


Fig. 2. High-resolution TEM image of the gate oxide and the strained-Si layer. The strained-Si layer is grown on relaxed (a) $Si_{0.8}Ge_{0.2}$, (b) $Si_{0.75}Ge_{0.25}$, and (c) $Si_{0.7}Ge_{0.3}$ VS. The strained-Si and gate oxide thickness are 6 and 6.5 nm, respectively.

level of strain is maintained in the channels for all alloy compositions in the VSs. However, a substantial increase in the surface threading dislocation density of the $Si_{0.70}Ge_{0.30}$ wafer compared with the $Si_{0.80}Ge_{0.20}$ wafer was found. Defect density was found to increase for higher Ge compositions, and it ranges from approximately 1×10^6 to 2×10^6 cm^{-2}. Details of the material characterization will be found elsewhere [11].

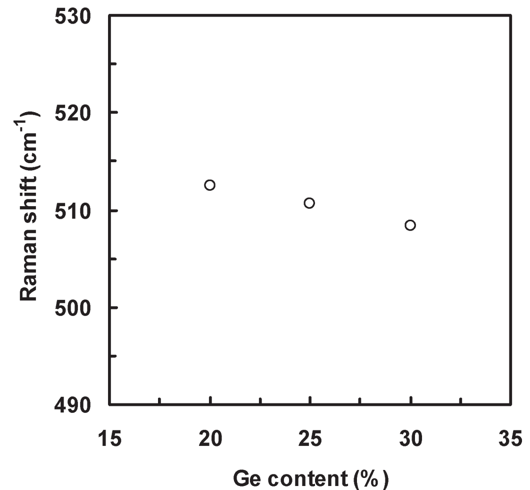


Fig. 3. Raman peak position of the Si–Si mode in the Si channel as a function of Ge content in the relaxed SiGe VS.

Fig. 4(a) shows typical high-frequency (1 MHz) C–V characteristics measured on 100 μm $\times$ 100 μm capacitors fabricated on Si and strained $Si/Si_{1-x}Ge_x$ substrate with SiO_2 as the gate oxide. Both bulk Si and strained-Si MOS capacitors were fabricated using a high thermal budget CMOS process. The strained-Si devices had a channel thickness of 6.0 nm. The C–V curves for all the SiGe devices show a plateau in the accumulation region. The plateau in C–V characteristics shows hole confinement at the strained Si/SiGe interface at a lower value of gate voltage. This occurs as the gate voltage is swept from flat band to accumulation. In strained-Si MOS capacitors, holes are confined at the strained Si/SiGe heterointerface. As a result, the net capacitance in the strained-Si wafers is the series combination of oxide capacitance and the capacitance associated with the strained Si/SiGe quantum well. A similar observation was found in Swain *et al.* [22], where confinement was described as kinks in the C–V characteristics. The capacitance of the bulk Si in accumulation is solely attributed to the gate oxide. Thus, plateaux in the C–V curves are observed for strained-Si devices but not for bulk Si devices. From Fig. 4(a), it is noted that the depletion capacitance at the inversion region increases with Ge content in the VS. This is attributed to the increase of donor type impurities in the semiconductor substrate of the MOS capacitor. This is possible as nonsubstitutional Ge atoms create donor-like defects in the strained Si/SiGe layers [24]. Another possibility is the dependency of activation rate of the impurities on Ge fraction in SiGe VS. Fig. 4(b) shows the effect of strained-Si thickness in the C–V curves of strained $Si/Si_{0.8}Ge_{0.2}$ MOS capacitors. The plateau in the C–V curves is noticeable for devices with channel thicknesses of 6 and 5.5 nm. The curve for the capacitor with channel thickness of 4.7 nm shows no plateau or peak, whereas the curve for the thinnest device with channel thickness of 3.7 nm shows an additional peak in the depletion region. The plateau in the accumulation part of the C–V curve for thicker device is due to the confinement of holes at the heterojunction between strained-Si and relaxed SiGe layers [25]. The peak in the thinnest device is due to the presence of a large number of interface traps at the strained Si/SiO_2 interface. Fig. 4(c)

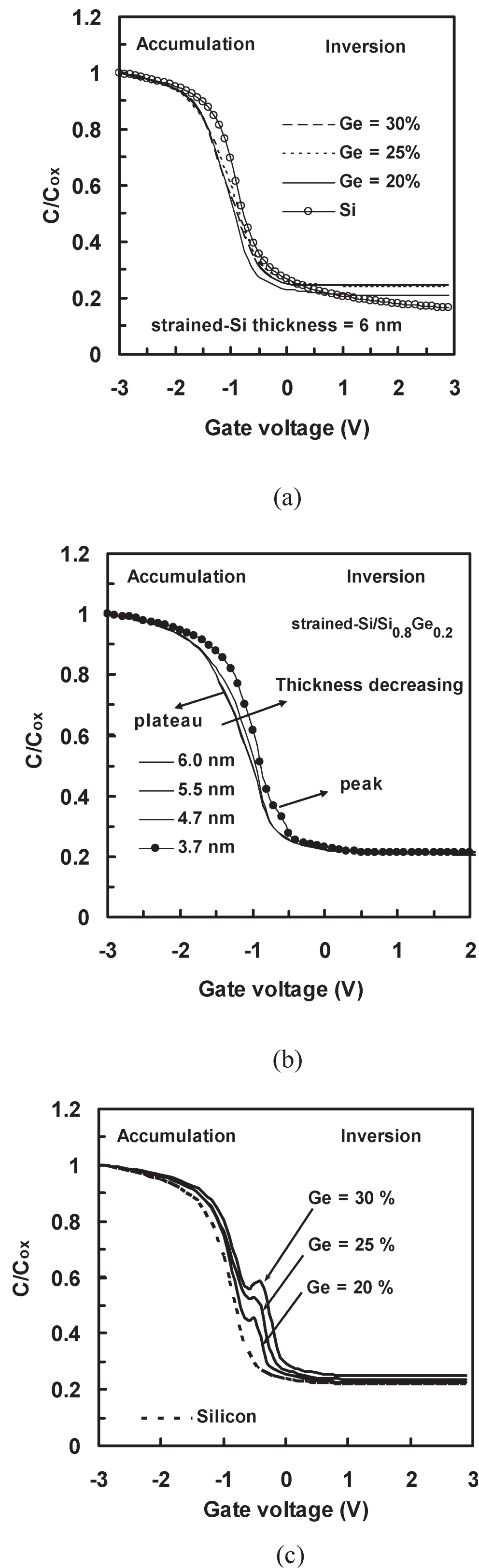


Fig. 4. (a) High-frequency (1 MHz) C–V characteristics of MOS capacitors. MOS capacitors are fabricated on Si and strained $\mathrm{Si/Si_{1-x}Ge_x}$ substrate ($x = 0.2, 0.25,$ and 0.3). The thickness of the strained-Si layer is 6.0 nm. (b) C–V characteristics of strained $\mathrm{Si/Si_{0.8}Ge_{0.2}}$ MOS devices at 1 MHz for different strained-Si channel thicknesses. (c) C–V characteristics of MOS capacitors with strained-Si layer thickness of 3.7 nm. The peak in the weak inversion region increases with Ge content in the VS, showing higher interface trap densities.

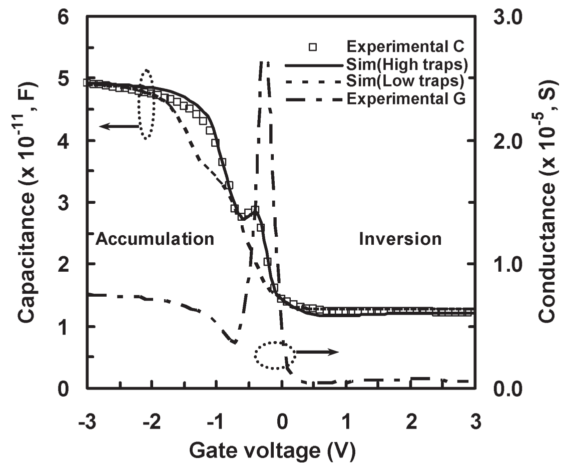


Fig. 5. Capacitance and conductance characteristics as a function of gate for the strained $\mathrm{Si/Si_{0.7}Ge_{0.3}}$ MOS capacitor having a channel thickness of 3.7 nm. The area of the MOS structure is 10^{-4} $\mathrm{cm^2}$.

shows the C–V characteristics at a frequency of 1 MHz of the surface channel strained $\mathrm{Si/Si_{1-x}Ge_x}$ $(x = 0.2, 0.25, 0.3)$ MOS capacitors, having a strained-Si channel thickness of 3.7 nm. The C–V characteristic of bulk Si devices fabricated on the same run is also included for comparison. The C–V curves for all the SiGe devices show a peak in the weak inversion region, indicating a high interface trap density. From Fig. 4(c), it is observed that the MOS capacitor with the highest Ge percentage (30%) shows the most prominent peak in the C–V characteristics. The magnitude of the peak is reduced as the Ge percentage is decreased. The reason for this reduction is the decrease in D_{it} at the strained $\mathrm{Si/SiO_2}$ interface as the Ge content in the VS is reduced.

Series resistance (R_s) is one of the major sources of small signal energy losses in MOS capacitors. This causes serious errors in parametric extractions such as D_{it} and Q_f/q from admittance measurements. The error can be reduced by employing series resistance corrections on the measured C–V and G–V data [23]. Fig. 5 shows the effect of series resistance on admittance characteristics for thermally grown $\mathrm{SiO_2}$ films on strained $\mathrm{Si/Si_{0.7}Ge_{0.3}}$ substrate with channel thickness of 3.7 nm, measured at 1 MHz. The presence of a peak in the G–V characteristics indicates that interface traps are responsible for the dominant loss.

A more detailed study for the characteristics of the increased interface trap density and its resulting peak in the C–V curve has been performed. Simulations of the C–V characteristics were also performed using Medici, a commercial TCAD device simulator [26]. Two sets of simulation were performed. The first was using an ideal device characteristic where a nominal amount of interface trap density was included in the simulation. In the second set of simulations, the same parameters were used but with an increased interface trap density $(9.2 \times 10^{12}\ \mathrm{eV^{-1}\,cm^{-2}})$. The results of these two different simulations are shown in Fig. 5. From the simulation of the ideal $\mathrm{Si_{0.7}Ge_{0.3}}$ MOS capacitor with nominal interface trap density, Sim(Low traps) exhibits a normal or "expected" C–V curve with a plateau. The plateau is attributed to the confinement of holes at a strained $\mathrm{Si/Si_{0.7}Ge_{0.3}}$ interface when a negative voltage

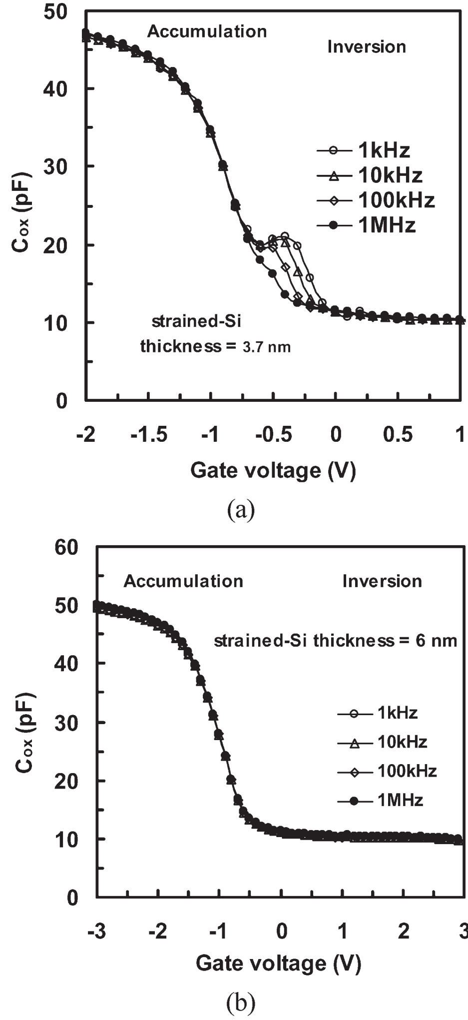


Fig. 6. Frequency dispersion in C–V characteristics of thermally grown SiO_2 films on strained $Si/Si_{0.8}Ge_{0.2}$ substrate. Thickness of the strained-Si layer is (a) 6.0 nm and (b) 3.7 nm.

is applied to the gate. In case of simulation, where a high value of interface trap density is included, Sim(High traps), in Fig. 5, the simulated C–V curve closely matches with the experimental curve including the loss of the plateau and the rise of the peak during weak inversion regions. The influence of the high level of interface trap densities is also confirmed by the G–V characteristics. In an experimental G–V curve, conductance reaches a peak value (in weak inversion) when loss is dominated by generation and recombination through interface traps at the surface (strained-Si/SiO_2 interface) as the interface trap time constant varies inversely with carrier density at the interface [27]. The G–V characteristics as seen in Fig. 5 reach a peak value as the gate voltage is swept to the weak inversion (-0.2 V) and drops to a low value in the strong inversion (> 0.2 V) regions.

Fig. 6(a) and (b) shows the corrected C–V curves at the indicated frequencies for strained $Si/Si_{0.8}Ge_{0.2}$ capacitors. Measurements were performed at frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz. Fig. 6(a) presents the C–V characteristics of strained $Si/Si_{0.8}Ge_{0.2}$ MOS capacitors having a channel thickness of 3.7 nm. The C–V characteristics measured at all frequencies do not show the presence of a plateau. However, the peak during weak inversion is present for all frequencies measured and varies with frequency. The peak is observed to be more prominent as the measurement frequency is reduced. As the frequency is reduced, the peak is "stretched out" and covers a larger gate voltage range across the weak inversion region. This "stretching" of the C–V curve is due to generation and recombination in the interface traps as the frequency is varied [23], [28]. At high frequencies, the time period of the ac voltage applied to the gate is short, since it is inversely proportional to the frequency. As a result of the short time period, interface traps with a longer trap response time will not be able to permit charges to move in and out of the interface states in response to the applied signal [29]. This results in a reduced effect of interface traps on the measured C–V characteristics. Similarly, at low frequencies, the time period of the ac voltage is increased, leading to an increase in the number of interface traps able to respond to this signal. This is due to the increased number of interface traps having a smaller trap response time compared to the bigger time period of the ac gate voltage. With the increase in the generation and recombination rate in interface traps, its effect on the measured C–V characteristics would increase as well. This is observed as the "stretching" of the C–V curves as the gate voltage is reduced. However, it is noted that no frequency dispersion in the C–V characteristics is observed when the thickness of the strained-Si layer is 6 nm. The stretching of C–V peaks in the depletion region along the voltage axis may be due to the discrete distribution of interface states. Different gate voltages will activate different distribution levels in the band gap. In a later section, the inversion current level achieved in the thinnest strained-Si devices with high interface state density also indicates this type of unusual distribution.

Interface trap density $D_{\rm it}$ was determined from the combination of single-frequency C–V and G–V characteristics (Fig. 5) using Hill's method [30] for different strained-Si thicknesses and the Ge content in the VS. The expressions used for calculating the interface trap density and fixed insulator charge density are given by

$$D_{\rm it} = \frac{\left(\frac{2}{qA}\right)\left(\frac{G_{\max}}{\omega}\right)}{\left[\left(\frac{G_{\max}}{\omega C_{\rm ox}}\right)^2 + \left(1 - \frac{C_m}{C_{\rm ox}}\right)^2\right]} \tag{1}$$

and

$$\frac{Q_f}{q} = \frac{C_{\rm ox}}{Aq}(\phi_{\rm ms} - V_{\rm FB}) \tag{2}$$

where $G_{\max}$ is the maximum conductance in G–V plot with its corresponding capacitance (C_m), $C_{\rm ox}$ is the oxide capacitance, ω is the angular frequency, $V_{\rm FB}$ is the flat band potential, A is the gate area of the capacitor, and $\phi_{\rm ms}$ is the difference between metal work function (Φ_m) and semiconductor work function (Φ_s), i.e., $\Phi_{\rm ms} = \Phi_m - \Phi_s$. In a strained Si/SiGe structure, Φ_m is unaffected while Φ_s needs to be redefined. $\phi_s(\text{unstrained Si}) = \phi_F(\text{unstrained Si}) + \chi_{\rm Si}$, where ϕ_F (unstrained Si) is the Fermi potential measured from the

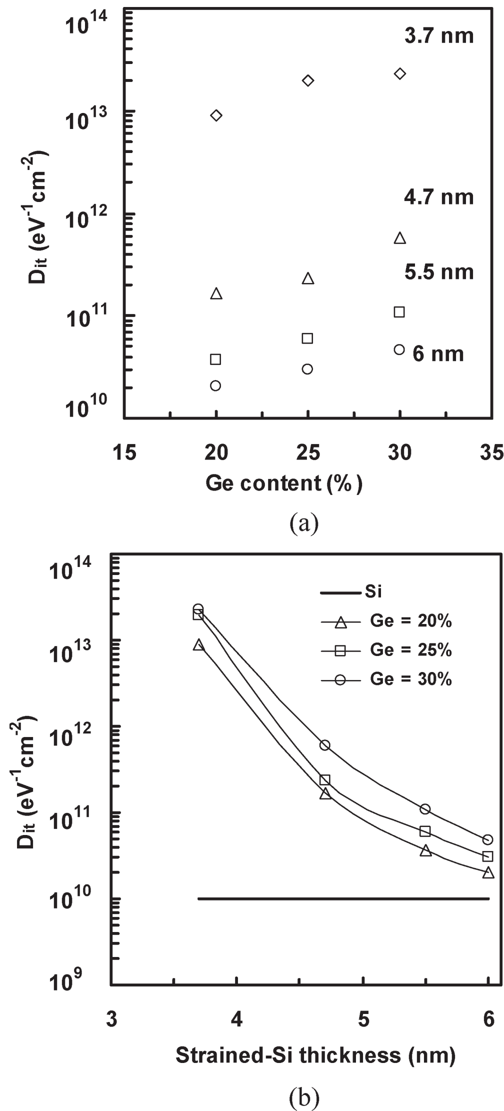


Fig. 7. Variation in the interface state density (a) as a function of Ge content in the VS and (b) as a function of strained-Si thickness of poly-Si/SiO_2 strained-Si MOS structure.

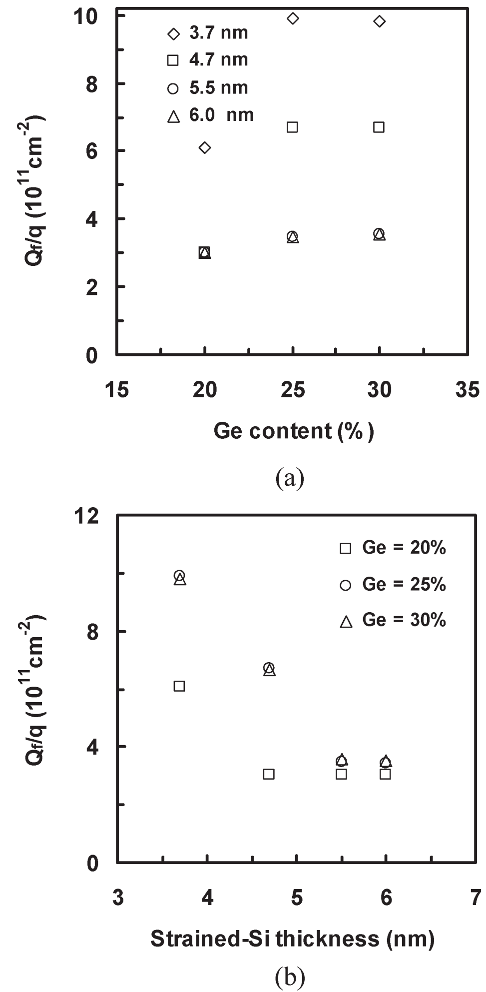


Fig. 8. Fixed oxide charge density (a) as a function of Ge content in the VS and (b) as a function of strained-Si thickness.

conduction band edge to the Fermi level and χ_s is the electron affinity of Si measured from the vacuum level to the conduction band edge. By taking the electron affinity of unstrained SiGe VS (χ_{siGe}) as reference, the electron affinity of strained-Si $(\chi_{\mathrm{strained\ Si}})$ is estimated to be $\phi_s(\text{strained-Si}) = \phi_F(\text{strained-Si}) + \chi_{\mathrm{SiGe}} + \Delta E_C$, where ΔE_C is the conduction offset. The flat band voltage V_{FB} is determined from the flat band capacitance value.

Fig. 7(a) shows the variation of D_{it} with Ge content in the VS for different strained-Si channel thicknesses. The results indicate that the mid-gap D_{it} of strained Si/SiO_2 is higher than that of bulk Si/SiO_2 but has an acceptable value of about $\sim 3 \times 10^{10}\ \mathrm{eV}^{-1}\ \mathrm{cm}^{-2}$ for a device of channel thickness 6 nm and Ge content $< 30\%$. From Fig. 7(a), we note that D_{it} increases with Ge content in the VS for all strained-Si layer thicknesses. These results are in excellent agreement with the observations of Wang *et al.* [31], where a significant degradation in gate oxide interface quality was also observed for SiGe alloy compositions with a maximum Ge mole fraction of 0.3. Gate oxide was deposited on strained-Si wafers by using electron cyclotron resonance sputtering techniques at a low temperature of 130 °C [32]. As the surface roughness of the strained-Si layer is increased with Ge content in the VS, there is a strong relationship between D_{it} and surface roughness of the strained-Si layer [31]. Moreover, D_{it} seems to increase more rapidly as the strained-Si thickness is reduced. D_{it} drastically increases below a strained-Si thickness of 4.7 nm, resulting from the Ge pileup at the strained Si/SiO_2 interface [16], [32]. A comparison between Figs. 6(a) and 7(b) indicates an increase of two orders of magnitude for D_{it}, and frequency dispersion is clearly observed in the C–V characteristics. Wang *et al.* [31] have also investigated the dependency of D_{it} of strained Si/SiO_2 interface with strained-Si thickness. They reported that D_{it} shows independence of strained-Si thickness, but the strained-Si thickness is in the range of 20–100 nm, which is thicker than the critical thickness [5], [11]. D_{it} has also been calculated using subthreshold swing (SS), and the calculated values are 5.1×10^{11}, 6.2×10^{11}, and 7.8×10^{11} for 20%, 25%, and 30% Ge composition in the relaxed SiGe VS, respectively, for a strained-Si thickness of 6 nm. The D_{it} values extracted using SS are slightly higher than those extracted using the C–V method.

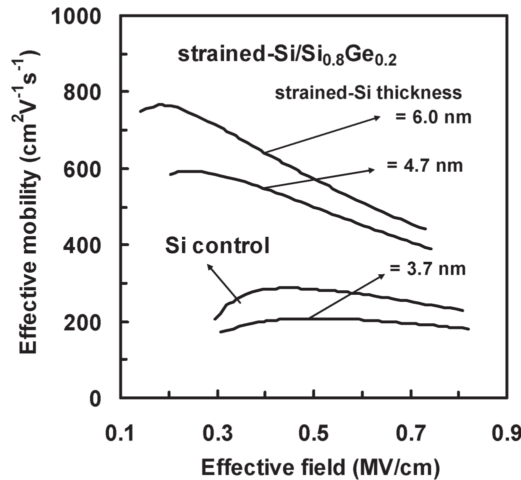
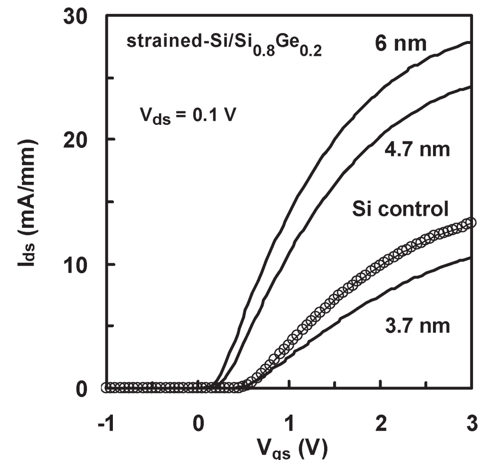


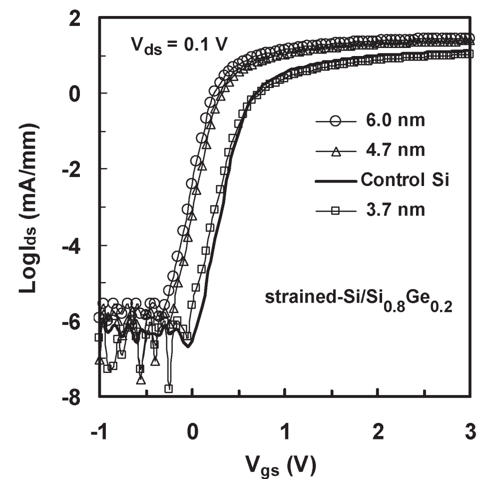
Fig. 9. Electron effective mobility as a function of effective field for control Si and strained-Si MOSFETs with different strained-Si thicknesses. The effective mobility for thinner strained-Si MOSFET is below the mobility for the control Si MOSFET across the effective field.

The fixed oxide charges calculated from the flat-band voltages are negative. Fig. 8(a) shows the variation of fixed oxide charge density with Ge content in the VS. During high-temperature oxidation of the strained-Si layer, Ge diffuses from the VS and piles up at the strained-Si/oxide interface where oxygen can be incorporated as Si–O–Si or Si–O–Ge bond structure. The weaker Ge–O bonds are easily broken, leaving a Si–O dangling bond structure [33], [34]. This dangling bond can trap an electron and becomes a negative fixed charge state. It is observed from Fig. 8(b) that Q_f/q reduces to a lower limit at a higher strained-Si thickness for any Ge content in the VS, and the value increases as the strained-Si thickness is reduced.

The mobility and subthreshold characteristics are highly sensitive to the gate oxide interface quality, and thermal oxidation of Ge causes a high interface trap density [35]–[37]. Figs. 9 and 10 indicate the effect of Ge diffusion on MOSFET characteristics. Fig. 9 shows the variation of effective mobility $(\mu_{\rm eff})$ as a function of effective field $(E_{\rm eff})$ for control Si and strained-Si MOSFETs having different strained-Si thicknesses. The mobility enhancement factor is significantly higher, ~ 2.2 times, at an effective field of 0.4 MV/cm for strained-Si MOSFETs having a strained-Si thickness of 6 nm. However, the mobility enhancement factor reduces with reduced strained-Si thickness. There is significant degradation of $\mu_{\rm eff}$ as the strained-Si thickness is reduced to 3.7 nm. Moreover, $\mu_{\rm eff}$ is lower than that of control Si across the whole range of $E_{\rm eff}$. This indicates that with the reduction of strained-Si layer thickness, the performance of the MOSFET degrades as well. The mid-gap $D_{\rm it}$ values for the capacitors for all SiGe VS compositions, with strained-Si channel thickness as parameter, are shown in Fig. 7(b). The state-of-the-art oxide quality, with mid-gap $D_{\rm it}$ values of approximately 3×10^{10} cm^{-2} eV^{-1} for all MOS capacitors, fabricated on VSs up to 25% Ge composition and strained-Si channel thickness of 6 nm, is demonstrated. There is a threefold increase in $D_{\rm it}$ values for the gate oxide grown on SiGe VS compared to the oxide grown on the VS with lower Ge contents, for the channel thickness of 6 nm. However, there are two orders of magnitude increase in $D_{\rm it}$ for the gate



(a)



(b)

Fig. 10. Drain–current versus gate voltage characteristics for the 2.0-μm gate length strained Si/$Si_{0.8}Ge_{0.2}$ n-MOSFET devices with different channel thicknesses presented (a) in logarithmic scale and (b) in linear scale.

oxide grown on the thinner strained-Si layer compared with the oxide grown on a thicker strained-Si layer, as shown in Fig. 7(b). High interface state densities will increase Coulombic scattering rates and thus degrade the effective carrier mobility of a MOS inversion layer at low vertical fields [38]. Therefore, the effective carrier mobility in the MOS inversion channel is degraded due to Ge out-diffusion since Ge atoms can create interface states at the strained Si/SiO_2 interface. In addition, fixed charges residing at the gate oxide lowers mobility over a wide range of vertical effective fields.

Fig. 10 shows the $I_{\rm ds} - V_{\rm gs}$ characteristics for 2-μm gate length at $V_{\rm ds} = 0.1$ V of control Si and strained Si/$Si_{0.8}Ge_{0.2}$ n-MOSFETs with different strained-Si channel thicknesses. From Fig. 10(a), it is noted that the strained-Si MOSFET with channel thickness of 6 nm shows the best performance, having the highest saturation drain–current of 27.9 mA/mm. However, it has a saturation drain–currents of 24.3 and 10.4 mA/mm for strained-Si MOSFETs, having channel thicknesses of 4.7 and 3.7 nm, respectively. The drain–currents at a gate voltage of 1.0 V are 14.1, 10.8, and 2.5 mA/mm for strained-Si MOSFETs with channel thicknesses of 6, 4.7, and 3.7 nm, respectively.

Although the value of the inversion current is 2.5 mA/mm for the thinnest strained-Si layer, it should be noted that the interface state density is too high [Fig. 7(b)] for the formation of a normal inversion layer along the channel. Thus, the result indicates that there may not be a continuous distribution of interface states from mid-gap to band edges, rather some discrete patches of interface states distributed within the band gap. There is almost a fivefold increase in magnitude of the drain–current at low gate voltage when the channel becomes thicker than 5 nm [39]. It is noted that drain–current at a low gate voltage is reduced after the channel becomes thinner than 4.7 nm, which is due to an increase of trapped charges and fixed oxide charges [23], [38]. The ON-state drain–current rapidly decreases below a strained-Si thickness of 4.7 nm. This can be attributed to poor confinement in the strained-Si channel, since electrons start to conduct through the low mobility relaxed SiGe VS. Electron mobility enhancement increases slightly for channels in the 4–5 nm thickness range to approximately 1.5, but poor confinement limits them to values much reduced compared to thicker channel devices. In fact, once the channel thickness increases beyond 5 nm, mobility enhancement is significantly increased. Currie *et al.* [16] have also shown that mobility enhancement of the device decreased below a strained-Si thickness of 5 nm for the device fabricated using low thermal budget. Fig. 10(b) indicates that the OFF-state current and the subthreshold characteristics of strained-Si devices are equivalent to that of bulk Si devices and relatively insensitive to the channel thickness if the channel thickness is higher than 5 nm. Devices having channel thickness lower than 5 nm show a high subthreshold slope due to higher interface trap densities [40]. It is worth mentioning that the present investigation is applicable up to a 5-nm thin-strained-Si channel layer with 30% Ge content in the VS. The inversion layer is approximately 5 nm thick; thus, if the strained-Si channel thickness is less than 5 nm, it will be unable to hold the inversion layer and inversion charges will "spill-over" to the parasitic channels. Furthermore, it has been reported that strained-Si MOSFET performance saturates in terms of drain–current, transconductance, etc., for 25% Ge content in the VS [4], [16]. So, the present study provides a high thermal budget processing guideline of an allo wable thickness for a strained-Si layer with the highest possible Ge content in the VS. To fabricate a working strained-Si MOSFET, a minimum channel thickness of 5 nm is required, irrespective of Ge composition in the VS. On the other hand, the strained-Si channel thickness will further be limited with the increase of Ge content in the VS. In the present study, gate oxide was grown to be 6.5 nm. The process is predicted to be applicable up to 3 nm of the gate oxide thickness, and below this, other tunneling mechanisms will start to occur and thus, for thinner gate oxides, device reliability will be a concern.

The correlation of interface trap density and fixed oxide charge to Ge content in the VS and strained-Si thickness could be explained by the Ge out-diffusion toward the strained Si/SiO_2 interface. A model was used to estimate the amount of Ge atoms that out-diffuse into the strained-Si epilayer [41]. Fig. 11 shows a simulation of the Ge diffusion as a function of device depth. The depth of "0" indicates the strained Si/SiO_2 interface. Silvaco [42], a commercial process simulator package, performed the simulation using Athena. The Ge concentration before and after undergoing the high-temperature processing steps is shown in Fig. 11(a) for devices fabricated on strained $Si/Si_{0.75}G_{0.25}$ with different channel thicknesses, varying from 3.7 to 6 nm. Fig. 11(b) shows the variation of Ge concentration at the strained Si/SiO_2 interface with Ge content in the VS. In the simulation, a strained-Si thickness of 3.7 nm was grown on top of the SiGe VS. Simulations for various Ge contents in the VS (20, 25, and 30%) were performed, and the resulting diffusion from each run was plotted together in Fig. 11(b). As shown in Fig. 11, the out-diffused Ge concentration at the strained Si/SiO_2 interface is increased more than 8% for the highest Ge percentage (30%) in the SiGe VS for a channel thickness of 3.7 nm. Fig. 12 shows the variation of $D_{\rm it}$ and Q_f/q with Ge concentration at strained Si/SiO_2 interface, where a significant amount of $D_{\rm it}$ and Q_f/q increased when the Ge concentration at the surface becomes more than 6%. It is also seen from Fig. 12 that the value of $D_{\rm it}$ increases by one order of magnitude for an increase of Ge content at

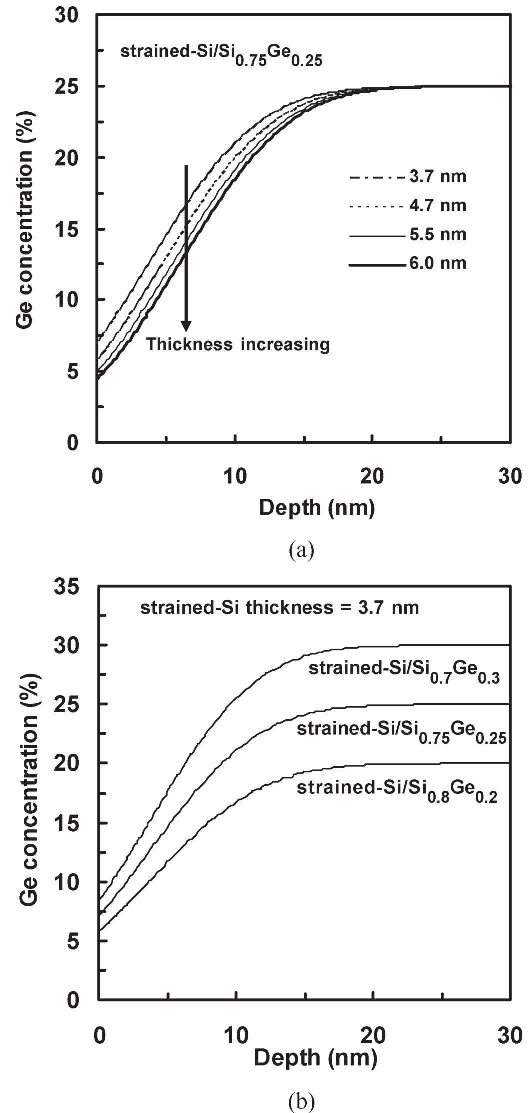


Fig. 11. TCAD simulated data indicating Ge diffusion through the strained-Si surface channel during device processing. (a) different channel thicknesses. (b) Varying Ge content in the VS.

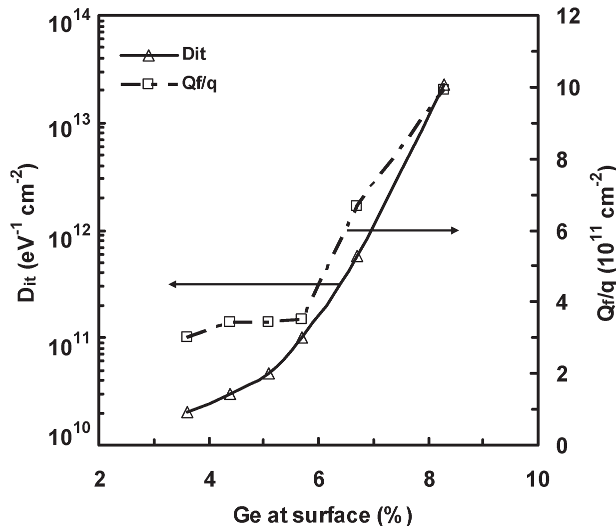


Fig. 12. Variation in the interface state density and fixed oxide charge density as a function of Ge concentration at the strained Si/SiO_2 interface. The Ge concentrations at the surface have been calculated using TCAD simulation. Interface trap density and fixed oxide charge density significantly increased when Ge concentration at the surface becomes higher than 6%.

the surface from approximately 6.7 to 8.3%. It is to be noted that $D_{\rm it}$ is the interface trap density that is proportional to the number of defects at the interface. Thus, if the out-diffused Ge atoms contribute to the interface state density, a logarithmic dependency is expected and that explains the increase of one order of magnitude of $D_{\rm it}$ with the nominal increase of Ge fraction at the surface. The increase of interface trap density causes the peak to appear in the depletion region of C–V and G–V characteristics as observed in Figs. 3(c) and 5, and reduces the mobility, resulting in the reduction of drain–current as observed in Figs. 9 and 10.

IV. Summary

We have investigated the effect of strained-Si channel thickness and Ge out-diffusion on the characteristics of strained Si/SiO_2 interface in order to optimize n-MOSFET device performance, fabricated using a high thermal budget CMOS process. Surface channel strained-Si MOS capacitors and n-MOSFETs were fabricated with channel thicknesses of 3.7, 4.7, 5.5, and 6 nm on relax $Si_{1-x}Ge_x$ $(x = 0.2, 0.25, \text{ and } 0.3)$ VS. C–V, G–V, and drain–current drain voltage characteristics have been used to study the interface properties of poly-Si/SiO_2/strained Si/$Si_{1-x}Ge_x$ structure. The variations in C–V characteristics with channel thickness and Ge content in the VS have been physically explained and accurately modeled using TCAD simulation. Interface trap density increases with Ge content in the VS and is also dependent on strained-Si thickness. The degradation of gate oxide quality ($D_{\rm it}$ and Q_f/q) occurs for a higher Ge content in the VS ($> 25\%$) and for thinner devices (< 5 nm), fabricated using a high thermal budget CMOS process. It was found that there is a significant increase in $D_{\rm it}$ and Q_f/q when the Ge concentration at the strained Si/SiO_2 interface is more than 6%. Surface channel strained-Si MOSFET performance has been correlated with channel thickness using C–V curves. It is noted that the drain–current at a low voltage is increased five times after the channel becomes thicker than 4.7 nm, which is due to a decrease in the number of trapped charges and fixed oxide charges. The ON-state drain–current rapidly decreases below a strained-Si thickness of 4.7 nm due to poor confinement and surface scattering. It is also seen that the off-state current is relatively insensitive to channel thickness, whereas subthreshold slope increased for devices having a channel thickness of 3.7 nm. The analyses undertaken in the present study suggest that a minimum strained-Si layer thickness of ~ 5 nm for up to 25% of Ge content in the VS is required to achieve a good strained Si/SiO_2 interface for surface channel strained-Si n-MOSFET, fabricated using a high thermal budget CMOS process.

Acknowledgment

The authors would like to thank members of the U.K. HMOS consortium.

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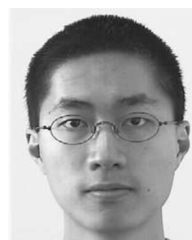

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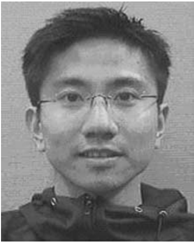

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