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Impact of the Stacking Order of HfO_x and AlO_x Dielectric Films on RRAM Switching Mechanisms to Behave Digital Resistive Switching and Synaptic Characteristics

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ABSTRACT Resistive random access memory (RRAM) devices with analog resistive switching are expected to be beneficial for neuromorphic applications, and consecutive voltage sweeps or pulses can be applied to change the device conductance and behave synaptic characteristics. In this paper, RRAM devices with a reverse stacking order of 6-nm-thick HfO_x and 2-nm-thick AlO_x dielectric films were fabricated. The device with $TiN/Ti/AlO_x/HfO_x/TiN$ stacked layers exhibited digital resistive switching, while the other device with $TiN/Ti/HfO_x/AlO_x/TiN$ stacked layers could demonstrate synaptic characteristics that were analog set and reset processes under consecutive positive and negative voltage sweeps or a train of potentiation and depression pulses. Moreover, this device could also implement synaptic learning rules, spike-timing-dependent plasticity (STDP). Varying temperature measurements and linear fittings of the measured data were conducted to analyze current conduction mechanisms. As a result, the variation of resistive switching behavior between these two devices is attributed to the varying effectiveness of the oxygen scavenging ability of the Ti layer when put into contact with either AlO_x or HfO_x . Moreover, AlO_x functioned as a diffusion limiting layer (DLL) in the device with $TiN/Ti/HfO_x/AlO_x/TiN$ stacked layers, and gradual modulation of the production and annihilation of oxygen vacancies is the cause of synaptic characteristics.

INDEX TERMS Resistive random access memory (RRAM), bilayered dielectric films, synaptic characteristics, diffusion limiting layer (DLL), conductive filament (CF), spike-timing-dependent plasticity (STDP).

I. INTRODUCTION

Resistive random access memory (RRAM) devices using transition metal oxides (TMOs) such as TiO_x [1], ZrO_x [2], AIO_x [3]–[4], HfO_x [5]–[6], and TaO_x [7]–[8] as resistive switching layers (RSLs) have been proposed and considered as promising future alternatives to next-generation non-volatile memory, owing to their advantages of fast writing ability and read access, low power consumption, high-density integration, long retention time, and CMOS process compatibility [9]–[14]. Furthermore, a RRAM device with analog resistive switching can behave synaptic characteristics

by applying consecutive voltage sweeps or pulses appropriately, and this kind of RRAM device is considered a promising candidate for neuromorphic applications. Neurons communicate with each other by numerous synapses, and their synaptic weight can be adjusted by the ionic (e.g., Na^+ or Ca^{2+}) flow through them [15]–[16]. This scenario is similar to a filamentary switching-based RRAM device with the top electrode (TE) and bottom electrode (BE) connected by conductive filaments (CFs) comprising defects such as oxygen vacancies. To function as a neuromorphic device, the RRAM device must exhibit gradual resistance change instead of digital resistive switching, and the evolution and properties of CFs under set and reset processes play an important role in determining resistive switching behavior [17]. RRAM devices have been demonstrated as neuromorphic devices with different dielectric films, such as single-layered AlO_x [18], HfO₂ [19], and WO_x [20] as well as bilayered SiO₂/TaO_x [21] and TaO_x/TiO₂ [22]–[23]. However, the relation of the oxygen scavenging effect and the stacking order of bilayered dielectric films on resistive switching behavior has not yet been investigated thoroughly. Therefore, in this paper, RRAM devices with TiN/Ti/2-nm-thick AlOx/6-nm-thick HfOx/TiN and TiN/Ti/6nm-thick HfOx/2-nm-thick AlOx/TiN stacked layers were fabricated and measured. Linear fittings of the measured data were also conducted to analyze current conduction mechanisms, and the variation of resistive switching behavior between these two RRAM devices is investigated. Finally, a mechanism is proposed to explain the cause of synaptic characteristics.

II. DEVICE FABRICATION

Initially, six-inch p-type (100)-oriented crystalline silicon wafers with a 1-µm-thick thermal oxide layer deposited by low-pressure chemical vapor deposition (LPCVD) were used as substrates. A 100-nm-thick TiN layer was deposited by radio frequency (RF) sputtering and patterned to act as the BE of the RRAM device through lithography and dry etching. Next, 6-nm-thick HfO_x and then 2-nm-thick AlOx dielectric films were deposited by atomic layer deposition (ALD) at 250 °C to act as the RSL. Tetrakis(dimethylamino)hafnium (TDMAH, $[(CH_3)_2N]_4Hf$ and trimethylaluminum (TMA, Al(CH₃)₃) were used as precursors for the deposition of HfO_x and AlO_x, respectively. Then, a 10-nm-thick Ti interposing layer was deposited by RF sputtering to scavenge oxygen from the RSL. Finally, a 100-nm-thick TiN layer was deposited by RF sputtering to act as the TE of the RRAM device, and then lithography and dry etching were conducted to complete the fabrication. For comparison, a RRAM device with a reverse stacking order of bilayered dielectric films of 2-nm-thick AlOx and then 6-nm-thick HfOx was also fabricated. The device area of both devices was the same 25 μ m².

III. RESULTS AND DISCUSSION

Figs. 1(a) and 1(b) show the schematic diagrams of RRAM devices comprising TiN TE/Ti/2-nm-thick $AlO_x/6$ -nm-thick HfO_x/TiN BE (device A) and TiN TE/Ti/6-nm-thick $HfO_x/2$ -nm-thick AlO_x/TiN BE (device B) stacked layers. The main difference between these two devices is the reverse stacking order of the bilayered dielectric films, which means that the Ti layer contacts AlO_x and HfO_x in devices A and B, respectively. Furthermore, both AlO_x and HfO_x films were amorphous structure since they were deposited by ALD at 250 °C.

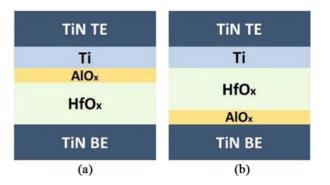


FIGURE 1. Schematic diagrams of RRAM devices with (a) TiN TE/Ti/AlO_x/HfO_x/TiN BE and (b) TiN TE/Ti/HfO_x/AlO_x/TiN BE stacked layers. And both HfO_x and AlO_x dielectric films were amorphous structure.

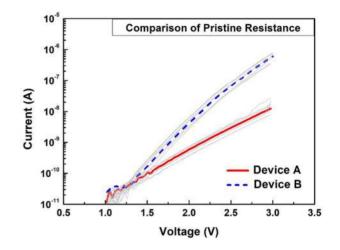


FIGURE 2. The comparison of pristine resistance between devices A and B summarized from respective 10 fresh devices.

Fig. 2 shows the comparison of pristine resistance between devices A and B summarized from respective 10 fresh devices. Fresh device A exhibited higher resistance (lower current) than fresh device B, although the total dielectric film thickness of both devices was the same. The variation of pristine resistance is attributed to higher oxide enthalpy of formation (or standard heat of formation) for AlO_x than HfO_x. According to the previous literature [24], an oxide will be more difficult to decompose if it has higher enthalpy of formation. Therefore, there will be fewer oxygen vacancies produced in the RSL of device A because the Ti is in contact with AlO_x instead of HfO_x.

Fig. 3(a) shows the typical DC sweep *I-V* curves of device A under 0.75 μ A current compliance, and the low operation current is attributed to highly resistive AlO_x and HfO_x. The device exhibited digital resistive switching with forming, set, and reset voltages of 3.12 V, 2.35 V, and -1.30 V, respectively, and a higher than 1 order of magnitude on/off resistance ratio at 0.2 V read voltage (V_{Read}). Fig. 3(b) shows retention properties of the high resistance state (HRS) and low resistance state (LRS) with V_{Read} of 0.2 V at 85 °C baking temperature for device A, and it exhibited good data retention capability. Fig. 3(c) shows the relation of

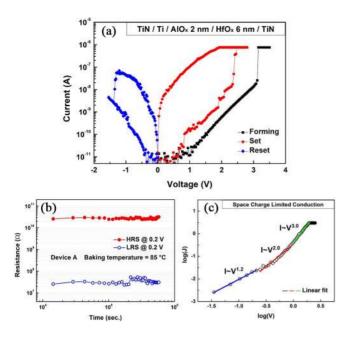


FIGURE 3. (a) Typical DC sweep measurement of device A with digital set and reset under 0.75 μ A current compliance. (b) Retention properties of the HRS and LRS with V_{Read} of 0.2 V at 85 °C baking temperature for device A. (c) Relation of log(*J*) vs. log(V) for the LRS curve of set process in (a).

 $\log(J)$ vs. $\log(V)$ for the LRS curve of the set process in Fig. 3(a). It can be found that the $\log(J)$ vs. $\log(V)$ curve can be divided into three regions with different slopes, as presented by the blue, red, and green lines in Fig. 3(c). In the low voltage region (blue line), the curve slope was 1.2, indicating ohmic conduction and that most electrons were thermally generated in the low voltage region. When the applied voltage was increased (red line), the amount of electrons injected from the electrode to the dielectric films increased, and partially trapped electrons were released from the dielectric film traps as well. The slope of the curve increased to 2.0, and this transport process was recognized as space charge limited conduction (SCLC). By further increasing the applied voltage (green line), the curve slope increased to approximately 3.0, the conduction current would vary fast owing to traps filled with electrons, and it corresponded to trap-filled SCLC (TF-SCLC).

Despite the high oxide enthalpy of formation for AIO_x , there were still oxygen vacancies produced in both dielectric films because the oxygen scavenging effect of Ti and the thickness of the Ti layer was much thicker than the AIO_x film. Moreover, during the 0 to 3 V set process, oxygen vacancies would also be produced because of the bondbreaking triggered by the applied electric field. This scenario is the cause for the ohmic conduction in the lower voltage region and SCLC as well as TF-SCLC in the higher voltage region.

Fig. 4(a) shows the typical DC sweep *I*-*V* curves of device B with discrete 4 V, 5 V, and 6 V stop voltages for set processes, and the respective stop voltages for reset processes

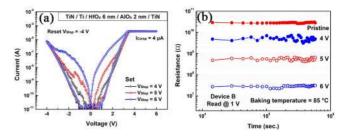


FIGURE 4. (a) Typical DC sweep measurements of device B with discrete 4 V (black), 5 V (red), and 6 V (blue) stop voltages for set processes. The respective stop voltages for reset processes were the same -4 V. (b) Retention properties of multilevel states, including the pristine state and the states with 4 V, 5 V, and 6 V stop voltages, with V_{Read} of 1 V at 85 °C baking temperature for device B.

were the same (-4 V). It is apparent that although the thickness of the AlO_x and HfO_x dielectric films for both devices A and B were the same, the resistive switching characteristics shown in Fig. 3(a) for device A and Fig. 4(a) for device B were much different. Device B exhibited forming-free characteristics with non-abrupt set and reset processes under 4 μ A current compliance. Although the results likewise showed digital resistive switching, multilevel characteristics could be achieved by applying different stop voltages for set processes. Fig. 4(b) shows retention properties of multilevel states, including the pristine state and the states with 4 V, 5 V, and 6 V stop voltages, with V_{Read} of 1 V at 85 °C baking temperature for device B, and it also exhibited good data retention capability.

From Fig. 4(a), the non-linearity property can be found for the set processes with 4 V and 5 V stop voltages and it is a signature of trap-assisted tunneling (TAT) with defects (trap states). To analyze the current conduction mechanisms and understand the possible evolution scenario of CFs, linear fittings of the measured data were also conducted. Figs. 5(a) and 5(b) show the relation of $ln(I/V^2)$ vs. I/V and ln(J) vs. I/E, respectively, for the LRS curve with 4 V stop voltage for the set process of device B. The linear fittings exhibited a straight line with negative slope in the higher voltage region for Fig. 5(a) and the lower voltage region for Fig. 5(b). The linear fitting results indicated that the current conduction mechanisms were Fowler-Nordheim (FN) tunneling for Fig. 5(a) and TAT for Fig. 5(b).

For the fresh device B, the oxygen scavenging effect of the Ti layer would mainly take effect on the 6-nm-thick HfO_x film, and there were only a few oxygen vacancies produced in the 2-nm-thick AlO_x film because of the Ti/HfO_x/AlO_x stacking order. Therefore, when applied 4 V stop voltage, it can be concluded that CFs would first be formed in HfO_x and that the current was conducted through AlO_x by FN tunneling in the higher voltage region because of the band bending. It is worth noting that some defects (oxygen vacancies) might be produced in the AlO_x film after current conducted through it because of the bond-breaking triggered by the applied electric field. And this is the reason for TAT in the lower voltage region. Furthermore, Figs. 5(c) and 5(d) show the

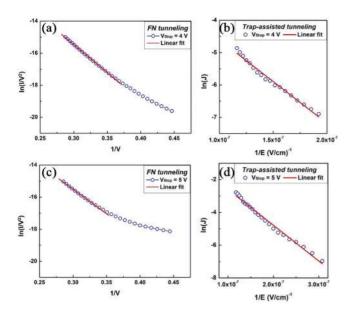


FIGURE 5. Relation of (a) $ln(I/V^2)$ vs. 1/V and (b) ln(J) vs. 1/E for the LRS curve with 4 V stop voltage for the set process in the higher and lower voltage regions, respectively, of device B. (c) and (d) are the same linear fittings as (a) and (b), respectively, but with 5 V stop voltage of device B.

same linear fittings as Figs. 5(a) and 5(b), respectively, but with 5 V stop voltage for the set process of device B. The linear fitting results also indicated that the current conduction mechanisms were FN tunneling in the higher voltage region and TAT in the lower voltage region. Although the current conduction mechanisms were the same for both 4 V and 5 V stop voltages, it can be found that, in the lower voltage region, device B exhibited higher LRS current with 5 V stop voltage according to Fig. 4(a). The reason for the higher current was that with a 5 V applied stop voltage under the same 4 µA current compliance, the device would experience a 4 µA current flow for a longer time. As a result, additional defects (oxygen vacancies) were produced in the AlO_x film and facilitated the process of TAT. When further increased the applied stop voltage to 6 V, more oxygen vacancies were produced and the non-linearity property was reduced as shown in Fig. 4(a). Therefore, it can be concluded that the weak CF had been formed in the AIO_x film.

То verify the proposed tunneling mechanism, Fig. 6(a) shows the DC sweeps with 5 V stop voltage of LRS device B under varying 25, 45, 65, 85, 105, 125, 145, and 165 °C. It can be found that the LRS current increased with increasing temperature. Based on this temperature dependence and sub-µA operation, it can be conjectured that the current conduction is non-metallic. Furthermore, Fig. 6(b) shows relation of ln(J) vs. 1/E for the curves corresponded to Fig. 6(a), and all the linear fittings under different temperatures exhibited a straight line with negative slope. The linear fitting results confirmed that the current conduction mechanism in the lower voltage region was mostly dominated by TAT.

Based on the linear fitting results mentioned above, CFs would first be formed in the HfO_x and that oxygen vacancies

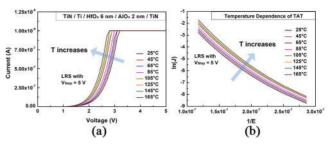


FIGURE 6. Temperature dependence of device B under LRS with 5 V stop voltage. (a) DC sweeps under varying 25, 45, 65, 85, 105, 125, 145, and 165 °C. The LRS current increased with increasing temperature. (b) Relation of In(J) vs. 1/E for the curves corresponded to (a). The linear fitting results confirmed the current conduction mechanism in the lower voltage region was TAT.

would be produced in the AIO_x after current conducted through it when the applied stop voltage was larger than 4 V. In addition, according to previous literatures, owing to the high activation energy of approximately 1.3 eV and the low oxygen diffusion coefficient at room temperature for oxygen diffusion in amorphous AI_2O_3 [25]–[26], the diffusion speed of oxygen ions and vacancies in the AIO_x film would be slow, and AIO_x therefore functioned as a diffusion limiting layer (DLL) [21] in device B. With the currentinduced oxygen vacancies and the limited diffusion speed of oxygen ions and vacancies in the AIO_x film, it can be concluded that the gradual resistance change can be achieved by applying either consecutive positive and negative voltage sweeps or a train of potentiation and depression pulses.

Fig. 7(a) shows the analog set process (potentiation) of device B under consecutive sweeps using 6 V stop voltage, and lower 1.5 µA current compliance was set to ensure a gradual resistance change. Fig. 7(b) shows the analog reset process (depression) of device B under consecutive sweeps using -4 V stop voltage without setting the current compliance. When consecutive 6 V DC sweeps were applied, current-induced oxygen vacancies were preferentially produced near the CFs in the AlO_x film, and the CFs became thicker. Furthermore, when consecutive -4 V DC sweeps were applied, oxygen ions moved more slowly and randomly because of the AlO_x DLL, resulting in uniform annihilation of oxygen vacancies, and the CFs became thinner. It can be concluded that the gradual resistance change in device B during potentiation and depression is attributed to the gradual modulation of the CF size in the AlO_x film. Inserted graphs in Figs. 7(a) and 7(b) show the proposed mechanisms for potentiation and depression, respectively.

Fig. 8 shows the comparison of conductance change behaviors under the voltage pulses of devices A and B. Fig. 8(a) shows potentiation and depression measurements of device A by applying 32 consecutive (3.0 V, 10 μ s) positive voltage pulses and 32 consecutive (-1.6 V, 10 μ s) negative voltage pulses. As a result, device A showed initial abrupt conductance change and then saturated under the voltage pulses. Furthermore, after applying 5 V stop voltage to device B, potentiation and depression characteristics had also

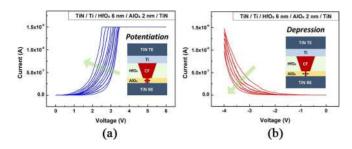


FIGURE 7. (a) Analog set process (potentiation) of device B under consecutive sweeps using 6 V stop voltage. (b) Analog reset process (depression) of device B under consecutive sweeps using -4 V stop voltage. Inserted graphs in (a) and (b) show the proposed mechanisms for potentiation and depression, respectively.

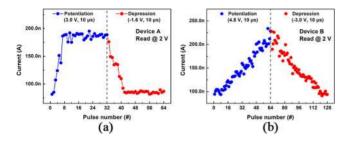


FIGURE 8. Potentiation and depression measurements of (a) device A by applying 32 consecutive (3.0 V, 10 μ s) positive voltage pulses and 32 consecutive (-1.6 V, 10 μ s) negative voltage pulses and of (b) device B by applying 64 consecutive (4.8 V, 10 μ s) positive voltage pulses and 64 consecutive (-3.0 V, 10 μ s) negative voltage pulses. Device A showed abrupt conductance change under the voltage pulses, while device B showed gradual resistance change during potentiation and depression.

been measured by applying 64 consecutive (4.8 V, 10 μ s) positive voltage pulses and 64 consecutive (-3.0 V, 10 μ s) negative voltage pulses, which are shown as Fig. 8(b). It can be found that device B showed gradual resistance change with good linearity during potentiation and depression, which was beneficial for neuromorphic applications.

Finally, synaptic learning rules in biological brains, such as spike-timing-dependent plasticity (STDP), had been implemented on device B, and it is typically measured according to the device conductance. The STDP behavior was measured with device B after applying 5 V stop voltage with 1 μ A current compliance. Fig. 9(a) shows the applied spikes used for STDP measurement. The pre-spike pulses were applied to the TiN TE electrode, and the post-spike pulses were applied to the TiN BE electrode. The pre-spike was composed of a train of 10 μ s negative pulses with -0.9, -1.1, -1.3, -1.5, -1.7, -1.9, -2.1, and -2.3 V pulse amplitudes, followed by a train of 10 μ s positive pulses with 4.1, 3.9, 3.7, 3.5, 3.3, 3.1, 2.9, and 2.7 V pulse amplitudes. The interval between neighboring pulses was 10 µs. The post-spike was composed of a $(-1.5 \text{ V}, 10 \text{ }\mu\text{s})$ negative voltage pulse and a $(1.5 \text{ V}, 10 \text{ }\mu\text{s})$ $10 \,\mu s$) positive voltage pulse with the same interval of $10 \,\mu s$. And the relative timing between the first positive pre- and post-spikes was denoted as Δt . The overlapping parts created between these two spikes would result in different conductance change (synapse weight change). Fig. 9(b) shows the

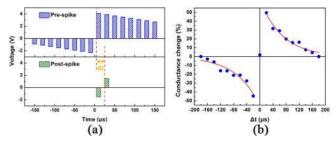


FIGURE 9. STDP behavior measured with device B. (a) The applied spikes used for STDP measurement. The pre-spike pulses were applied to the TiN TE electrode, and the post-spike pulses were applied to the TiN BE electrode. The pre-spike was composed of a train of 10 μ s negative pulses with -0.9, -1.1, -1.3, -1.5, -1.7, -1.9, -2.1, and -2.3 V pulse amplitudes, followed by a train of 10 μ s positive pulses with 4.1, 3.9, 3.7, 3.5, 3.3, 3.1, 2.9, and 2.7 V pulse amplitudes. The interval between neighboring pulses was 10 μ s. The post-spike was composed of a (-1.5 V, 10 μ s) negative voltage pulse and a (1.5 V, 10 μ s) positive voltage pulse with the same interval of 10 μ s. And the relative timing between the first positive preand post-spike was denoted as Δ t. (b) The measured conductance change (synapse weight change) as a function of Δ t for device B.

measured conductance change as a function of Δt for device B, and the conductance change was negative for $\Delta t < 0$, whereas it was positive for $\Delta t > 0$. Furthermore, linear fittings of the measured data can be described as follows:

$$\Delta W(\Delta t) = \begin{cases} \alpha^+ \times exp\left(\frac{-\Delta t}{\tau^+}\right) & \text{if } \Delta t > 0\\ -\alpha^- \times exp\left(\frac{-\Delta t}{\tau^-}\right) & \text{if } \Delta t < 0 \end{cases}$$
(1)

where ΔW is the conductance change and α^+ , α^- , τ^+ , and τ^- are fitting parameters. The measurement result was analogous to the STDP behavior observed in the hippocampus [27], and the implementation of important synaptic learning rules of device B made it suitable for neuromorphic applications.

IV. CONCLUSION

In conclusion, RRAM devices with a reverse stacking order of 6-nm-thick HfOx and 2-nm-thick AlOx dielectric films were proposed and investigated. Device A with TiN/Ti/AlO_x/HfO_x/TiN stacked layers exhibited digital resistive switching with forming, set, and reset voltages of 3.12 V, 2.35 V, and -1.30 V, respectively, and the linear fitting of the set process LRS curve showed that the current conduction mechanism was trap-controlled SCLC. Furthermore, device B with TiN/Ti/HfOx/AlOx/TiN stacked layers exhibited forming-free characteristics with non-abrupt set and reset processes under 4 µA current compliance. The linear fitting results indicated that the current conduction mechanisms were FN tunneling in the higher voltage region and TAT in the lower voltage region for both 4 V and 5 V stop voltages. Varying temperature measurements of device B were also conducted to confirm that the current conduction mechanism in the lower voltage region was mostly dominated by TAT. The variation of resistive switching behavior between devices A and B is attributed to the varying effectiveness of the oxygen scavenging ability of the Ti layer when put into contact with either AlO_x or HfO_x .

Furthermore, with the current-induced oxygen vacancies in the AlO_x film and the fact that AlO_x functioned as a DLL in the device B, the production and annihilation of oxygen vacancies could be gradually modulated in the AlO_x film. Therefore, the synaptic characteristics, which were analog set and reset processes, could be achieved by applying a train of 64 consecutive (4.8 V, 10 μ s) potentiation pulses and 64 consecutive (-3.0 V, 10 μ s) depression pulses. And device B showed gradual resistance change with good linearity during potentiation and depression. Finally, the implementation of important synaptic learning rules in biological brains, such as STDP, of device B made it suitable for neuromorphic applications.

REFERENCES

- D.-H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO₂ resistive switching memory," *Nat. Nanotechnol.*, vol. 5, no. 2, pp. 148–153, Feb. 2010. doi: 10.1038/NNANO.2009.456
- [2] Q. Liu et al., "Improvement of resistive switching properties in ZrO₂-based ReRAM with implanted Ti ions," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1335–1337, Dec. 2009. doi: 10.1109/LED.2009.2032566.
- [3] W. Kim, S. I. Park, Z. Zhang, and S. Wong, "Current conduction mechanism of nitrogen-doped AlO_x RRAM," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2158–2163, Jul. 2014. doi: 10.1109/TED.2014.2319074.
- [4] W. Banerjee *et al.*, "Occurrence of resistive switching and threshold switching in atomic layer deposited ultrathin (2 nm) aluminium oxide crossbar resistive random access memory," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 333–335, Feb. 2015. doi: 10.1109/LED.2015.2407361.
- [5] K.-C. Chuang *et al.*, "Effects of electric fields on the switching properties improvements of RRAM device with a field-enhanced elevated-film-stack structure," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 622–626, 2018. doi: 10.1109/JEDS.2018.2832542.
- [6] H. Y. Lee *et al.*, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO₂ based RRAM," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2008, pp. 297–300. doi: 10.1109/IEDM.2008.4796677.
 [7] Z. Wei *et al.*, "Highly reliable TaO_x ReRAM and direct evidence
- [7] Z. Wei *et al.*, "Highly reliable TaO_x ReRAM and direct evidence of redox reaction mechanism," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2008, pp. 293–296. doi: 10.1109/IEDM.2008.4796676.
- [8] J. J. Yang *et al.*, "High switching endurance in TaO_x memristive devices," *Appl. Phys. Lett.*, vol. 97, no. 23, pp. 1–3, Dec. 2010. doi: 10.1063/1.3524521.
- [9] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, Jul. 2009. doi: 10.1002/adma.200900375.
- [10] H.-S. P. Wong et al., "Metal–oxide RRAM," Proc. IEEE, vol. 100, no. 6, pp. 1951–1970, Jun. 2012. doi: 10.1109/JPROC.2012.2190369.
- [11] Y. Y. Chen *et al.*, "Endurance/retention trade-off on HfO₂/metal cap 1T1R bipolar RRAM," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1114–1121, Mar. 2013. doi: 10.1109/TED.2013.2241064.
- [12] R. Aluguri and T.-Y. Tseng, "Overview of selector devices for 3-D stackable cross point RRAM arrays," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 294–306, Sep. 2016. doi: 10.1109/JEDS.2016.2594190.
- [13] H. Zhao *et al.*, "High mechanical endurance RRAM based on amorphous gadolinium oxide for flexible nonvolatile memory application," *J. Phys. D Appl. Phys.*, vol. 48, no. 20, pp. 1–7, Apr. 2015. doi: 10.1088/0022-3727/48/20/205104.
- [14] S. Long, C. Cagli, D. Ielmini, M. Liu, and J. Suñé, "Analysis and modeling of resistive switching statistics," *J. Appl. Phys.*, vol. 111, no. 7, pp. 1–19, Apr. 2012. doi: 10.1063/1.3699369.
- [15] Y. Abbas *et al.*, "Compliance-free, digital SET and analog RESET synaptic characteristics of sub-tantalum oxide based neuromorphic device," *Sci. Rep.*, vol. 8, no. 1, pp. 1–10, Jan. 2018. doi: 10.1038/s41598-018-19575-9.

- [16] H. Tian *et al.*, "A novel artificial synapse with dual modes using bilayer graphene as the bottom electrode," *Nanoscale*, vol. 9, no. 27, pp. 9275–9283, Jun. 2017. doi: 10.1039/C7NR03106H.
- [17] J. Woo *et al.*, "Linking conductive filament properties and evolution to synaptic behavior of RRAM devices for neuromorphic applications," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1220–1223, Sep. 2017. doi: 10.1109/LED.2017.2731859.
- [18] Y. Wu *et al.*, "AlO_x-based resistive switching device with gradual resistance modulation for neuromorphic device application," in *Proc. 4th IEEE Int. Memory Workshop (IMW)*, Milan, Italy, May 2012, pp. 1–4. doi: 10.1109/IMW.2012.6213663.
- [19] J. Woo *et al.*, "Optimized programming scheme enabling linear potentiation in filamentary HfO₂ RRAM synapse for neuromorphic systems," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5064–5067, Dec. 2016. doi: 10.1109/TED.2016.2615648.
- [20] R. Yang *et al.*, "On-demand nanodevice with electrical and neuromorphic multifunction realized by local ion migration," *ACS Nano*, vol. 6, no. 11, pp. 9515–9521, Oct. 2012. doi: 10.1021/nn302510e.
- [21] Z. Wang *et al.*, "Engineering incremental resistive switching in TaO_x based memristors for brain-inspired computing," *Nanoscale*, vol. 8, no. 29, pp. 14015–14022, Apr. 2016. doi: 10.1039/C6NR00476H.
- [22] I.-T. Wang, Y.-C. Lin, Y.-F. Wang, C.-W. Hsu, and T.-H. Hou, "3D synaptic architecture with ultralow sub-10 fJ energy per spike for neuromorphic computation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2014, pp. 665–668. doi: 10.1109/IEDM.2014.7047127.
- [23] Y.-F. Wang, Y.-C. Lin, I.-T. Wang, T.-P. Lin, and T.-H. Hou, "Characterization and modeling of nonfilamentary Ta/TaO_x/TiO₂/Ti analog synaptic device," *Sci. Rep.*, vol. 5, no. 1, pp. 1–9, May 2015. doi: 10.1038/srep10150.
- [24] H. Choi *et al.*, "The effect of tunnel barrier at resistive switching device for low power memory applications," in *Proc. 3rd IEEE Int. Memory Workshop (IMW)*, Monterey, CA, USA, May 2011, pp. 1–4. doi: 10.1109/IMW.2011.5873243.
- [25] T. Nabatame *et al.*, "Comparative studies on oxygen diffusion coefficients for amorphous and γ-Al₂O₃ films using ¹⁸O isotope," *Jpn. J. Appl. Phys.*, vol. 42, no. 12, pp. 7205–7208, Dec. 2003. doi: 10.1143/JJAP.42.7205.
- [26] R. Nakamura *et al.*, "Diffusion of oxygen in amorphous Al₂O₃, Ta₂O₅, and Nb₂O₅," *J. Appl. Phys.*, vol. 116, no. 3, pp. 1–8, Jul. 2014. doi: 10.1063/1.4889800.
- [27] G.-Q. Bi and M.-M. Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *J. Neurosci.*, vol. 18, no. 24, pp. 10464–10472, Dec. 1998. doi: 10.1523/JNEUROSCI.18-24-10464.1998.



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