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Impact of VCO and PLL Phase Noise on Distributed Beamforming Arrays With Periodic Synchronization

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ABSTRACT Distributed beamforming between separate wireless nodes in a distributed antenna array requires significant coordination of the relative electrical states of the systems to achieve and maintain a phase-coherent state. A principal factor impacting distributed phase coherence is the relative stability of the local oscillators on each node. Ensuring a coherent state requires the distribution of a reference frequency such that all nodes are operating on the same basis frequency. To support distributed beamforming, the reference frequency must furthermore be distributed wirelessly, typically using a phase-locked loop (PLL) on the secondary nodes. In large arrays, the wireless link used for frequency distribution will have limited capacity, necessitating intermittent updates during which the oscillators are locked, and between which their frequencies will drift. The stability of the oscillator therefore plays an important role in the overall performance relative to the update time. In this paper, we discuss the sources of phase noise generated by the reference oscillator and the PLL, and analyze the impacts of phase noise and update interval on distributed beamforming performance. We provide a framework for analyzing distributed beamforming performance from oscillator and PLL parameters in general, and we analyze beamforming performance for two specific cases using nominal high-stability and low-stability voltage-controlled oscillators, with a parametric comparison between their impact on beamforming performance.

INDEX TERMS Coherent distributed array, distributed beamforming, frequency locking, oscillator noise, phase locked loop, phase noise, wireless frequency synchronization.

I. INTRODUCTION

Increasing connectivity between separate wireless systems has led to significant improvements in capabilities based on distributed cooperation. Furthermore, the rise in distributed cooperation has generated significant interest in the possibilities of coordinating separate systems coherently, where synchronization is obtained at the level of the wavelength of the wireless operation. If synchronized within a fraction of a wavelength, separate systems can coordinate their wireless emissions to implement coherent distributed beamforming, achieving, in effect, a distributed phased array. Other than increasing the transmitted power to a base station, beamforming has many applications such as improv-

ing imaging capabilities of remote sensing systems [1], [2], clutter suppression for weather radars [3], and maximizing the sum secrecy rate of multibeam satellite downlink networks [4], among others. Whether implemented between smart devices for increased range or throughput, between small satellites to mimic the operation of a larger satellite, or on a swarm of small unmanned aerial vehicles for remote sensing, distributed beamforming promises to provide reliable, adaptable wireless functionality with equivalent or better performance than a single large system can provide, at a fraction of the cost. Achieving distributed coherence necessitates accurate synchronization of the electrical states of each individual element. Principally, the elements need to be frequency locked, phase aligned, and time aligned. Two main topologies have been explored for distributed synchronization: closed-loop [5]–[7] and open-loop [8]. In

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closed-loop distributed beamforming, feedback is provided by the destination node in some form. This may represent a base station providing even small amounts of information regarding the signal throughput of the array, which is then used by each node to adjust their phase states to increase beamforming performance with regards to defined metrics. In open-loop distributed beamforming, the nodes in the array self-align, without relying on feedback from the destination. Closed-loop systems require less coordination between the nodes in the array, however in many cases such systems are limited by the ability to beamform only to the destination node, as the array does not have sufficient information to steer a beam arbitrarily, thus limiting the technique primarily to communication applications. In contrast, open-loop systems can arbitrarily steer beams to any direction, enabling applicability to any wireless application, from communications to remote sensing. Open-loop systems, however, require significantly more coordination between the individual node to achieve and maintain a phase coherent state.

In either topology, there are many factors that influence the ability to coherently transmit a signal from a collection of separate nodes, involving the system hardware, the inter-node coordination, and the environment. Coordination errors are critical, and have been studied extensively, for instance relating to time synchronization [9], [10] and frequency synchronization in closed-loop distributed beamforming [5]–[7], [12]–[14], and in open-loop distributed beamforming [11]. In some of the closed-loop approaches referenced above, channel errors are also corrected; for open-loop systems, far-field beamforming in media that varies little over the domain of the nodes can mitigate the effects of channel differences. But in all cases, the intrinsic hardware on each node will impact the beamforming ability. Of the hardware components that impact beamforming, phase error due to differences between the local oscillators is among the most fundamental, and is present in general, regardless of whether the system operates open-loop or closed-loop. Phase, frequency, and time errors due to the voltage-controlled oscillator (VCO) and phase-locked loop (PLL) in the frequency synchronization circuits are the focus of this paper.

The stability of the local oscillator on each node is a principal factor influencing the ability to achieve and maintain relative phase coherence between nodes, regardless of whether feedback is used or not. The primary challenge stems from the phase noise of the oscillator [15] and the PLL used on the nodes [16], as well as the intermittent synchronization that is generally necessary in distributed beamforming. For even moderately-sized arrays (i.e. more than five nodes or so), any frequency synchronization topology will generally necessitate time-duplexing of the wireless coordination between the nodes to achieve scalability. This intermittent synchronization results in frequency random walk or frequency drift on each node between synchronization intervals. It is thus important to characterize the impact on phase coherence due to oscillator instability and update interval. Wireless frequency synchronization has been achieved using

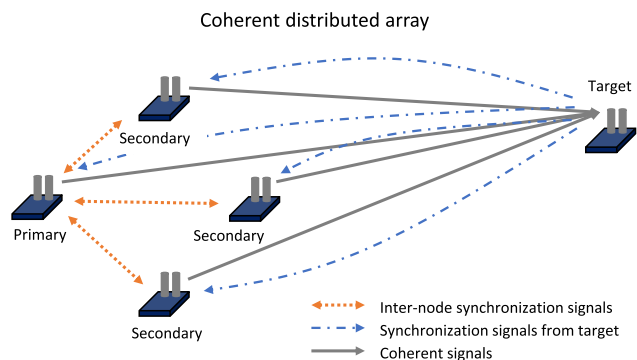


FIGURE 1. General architecture of coherent distributed arrays where the nodes achieve synchronization using inter-node signals, and external signals from the targeted location. A hierarchical topology is shown, where the secondary nodes achieve synchronization in reference to a primary nodes. As an example, the secondary nodes would lock their oscillators frequencies to the frequency of the oscillator of the primary node.

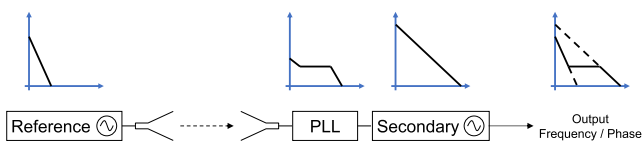


FIGURE 2. Phase noise profile of the wirelessly synchronized secondary nodes where the reference oscillator has lower phase noise in comparison to the phase noise of the locked oscillator.

bursts of synchronization packets [17], coupled-oscillators [18], optically-locked voltage controlled oscillators [19], and global positioning system (GPS) phase information [20], among other approaches. Here we consider a general architecture where PLLs are used to synchronize the frequency on a set of secondary nodes to a reference signal transmitted by a primary node [11], [24], [25]. Specifically, we are interested in both topologies, open-loop and closed-loop, that fit the model in Fig. 1, where wireless frequency synchronization is performed within the array in a primary/secondary architecture. In such architectures, the secondary nodes lock their frequencies to one primary node or to an external device. This results in a phase noise profile on the locked secondary nodes that is a combination of the phase noise of the reference oscillator, the PLL on the secondary node, and the oscillator in the PLL, as shown in Fig. 2. Although the array portrayed in Fig. 1 would likely implement element-level digital beamforming, the analysis in this work does not presume a specific beamforming approach, and is thus applicable for both analog and digital beamforming arrays.

General evaluations of phase noise effects in coherent distributed systems have been presented in prior works [21]–[23]. To our knowledge, the literature lacks explicit evaluation of the effects of the phase noise of oscillators and PLLs on coherent beamforming in coherent distributed arrays. We specifically analyze in this paper the phase noise of locked and unlocked PLLs, and we study the impact of synchronization update rate on coherent beamforming performance. It is assumed that the antennas used for wireless

frequency synchronization are not used for other wireless functions in this work; beamforming could be implemented with the same antennas or could use separate antennas. The frequency synchronization signals are considered as both continuous wave (CW) and pulsed signals which can be generated using the approach described in [11], [24], [25], where an adjunct self mixing circuit is used to demodulate a 10 MHz reference signal from a CW two-tone signal. The coherent gain is investigated for array sizes of $N = 2, 10, 20,$ and 100 for the case where phase, frequency, and timing errors are present. We provide a general framework for evaluating distributed beamforming performance in terms of phase noise and update interval, and assess the performance of nominal high quality and low quality VCOs.

II. PHASE NOISE OF OSCILLATORS AND PHASE-LOCKED LOOPS

A. OSCILLATOR PHASE NOISE

One of the important metrics for an oscillator is its spectral purity. Ideally, an oscillator is described using a sine wave with nominal voltage v_0 and nominal angular frequency w_0 :

$$v(t) = v_0 \sin(w_0 t). \tag{1}$$

In practice, due to fluctuations of the amplitude and phase of the output signal, the spectrum of an oscillator extends around w_0 , along with extra spurs and harmonics at the frequencies $2 w_0, 3 w_0, 4 w_0,$ etc. The instantaneous output of the oscillator can be represented by

$$v(t) = v_0 [1 + A(t)] \sin [w_0 t + \phi(t)] + v_{\text{harmonics}}(t) + v_{\text{spurs}}(t) \tag{2}$$

where $A(t)$ represents the amplitude fluctuations, and $\phi(t)$ refers to the phase fluctuations. Phase noise is a combination of spurious signals represented by $v_{\text{spurs}}(t)$ and random phase fluctuations. Spurious signals are usually caused by external noise sources such as noise on power supply and bias currents, while random phase fluctuations tend to be generated internally to the oscillator. The phase noise of an oscillator is quantified and represented by the single-sideband (SSB) phase noise, which is defined by the ratio of power at an offset f_m with 1 Hz bandwidth over the total power for a SSB. The phase noise is obtained from [26]

$$L(f_m) = 10 \log \left(\frac{P_{\text{noise}}(f_m)}{P_{\text{sig}}} \right) = 10 \log \left(\frac{v_{n,RMS}^2(f_m)}{v_{c,RMS}^2} \right) \tag{3}$$

where P_{sig} is the signal power, $v_{c,RMS}^2$ is the root mean square (RMS) amplitude of the carrier, and $v_{n,RMS}^2(f_m)$ is the RMS amplitude of the signal representing the phase noise at an offset frequency f_m . The oscillator noise is in general the result of both amplitude modulated and phase modulated noise, thus the phase noise (3) can be written as

$$L(f_m) = 10 \log \left(\frac{S_{\phi}(f_m)}{2} + \frac{S_a(f_m)}{2} \right) \tag{4}$$

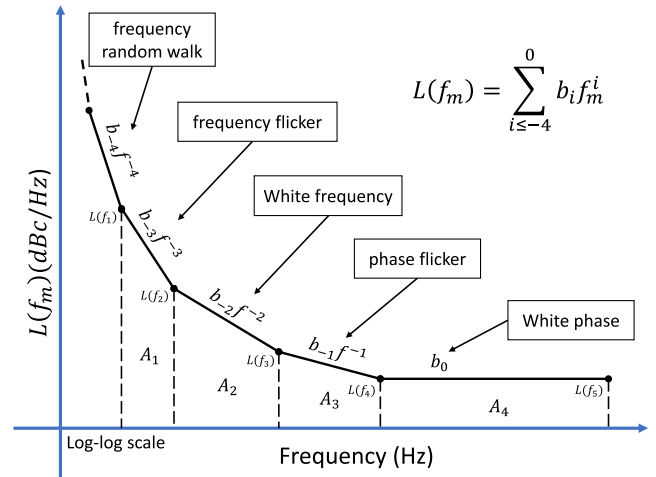


FIGURE 3. General shape of the phase noise of an oscillator. The variables b_i represent the noise power associated with each phase noise type.

where $S_{\phi}(f_m)$ represents the double-sideband (DSB) phase noise spectral density and $S_a(f_m)$ represents the DSB amplitude noise spectral density. Generally, close to the carrier, phase modulated noise dominates and dictates the power of the phase noise, while at far offsets, both phase modulated and amplitude modulated noises contribute equally.

The spectral profile of the phase noise of an oscillator can be approximately modeled by considering the dominant noise contributions in different frequency regions. The result is a piecewise linear profile in dBc/Hz, where each line segment has a specific slope as shown in Fig. 3, where the regions have slopes of 0 (0 dB/decade), $1/f$ (−10 dB/decade), $1/f^2$ (−20 dB/decade), $1/f^3$ (−30 dB/decade), $1/f^4$ (−40 dB/decade).

The noise profile of an oscillator is shaped by the passive and active components in the circuit, such as MOSFETs, BJTs, and resonators. For instance, the injected noise is shaped by the VCO resonator where the flat noise becomes $1/f^2$ and the $1/f$ noise becomes $1/f^3$ at the output of the oscillator [27], [28].

Many models for the phase noise of an oscillator exist [27]–[29]. An early model of the phase noise of an oscillator was derived by Leeson [27], and is based on a linear time-invariant (LTI) approach. The Leeson phase model is given by

$$L(f_m) = 10 \log \left[\frac{FkT_e}{2P_{\text{sig}}} \left(1 + \left(\frac{f_0}{2Q_L f_m} \right)^2 \right) \left(1 + \frac{f_k}{f_m} \right) \right] \tag{5}$$

where F is the effective noise figure of the oscillator, k is the Boltzmann constant 1.38×10^{-23} J/K, T_e is the temperature in K, f_0 is the nominal frequency of the oscillator, Q_L is the loaded quality factor of the resonator, and f_k is the flicker noise corner frequency in the phase noise, which is not always equal to the flicker noise corner frequency of the active devices.

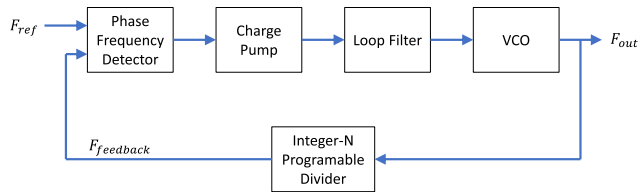


FIGURE 4. Typical architecture of PLL with frequency synthesizer. F_{ref} represents the input frequency to the PLL, this frequency can be lower version than the input reference frequency, which can be generated using frequency dividers. F_{out} is the output frequency of the VCO, while the $F_{feedback}$ is a divided version of the F_{out} .

B. PLL PHASE NOISE

A PLL is a control system that disciplines the frequency and phase of an oscillator using a reference input signal [26], [30], [31]; a common architecture is shown in Fig. 4 where a PLL with frequency synthesizer is used [32]. A frequency synthesizer is an electronic circuit that generates multiple frequencies out of a single reference frequency, and it is mainly used to ensure that the feedback frequency is equal to the input reference frequency. PLLs are necessary for cooperative systems such as distributed wireless systems where every node needs to be operating at the same frequency to achieve coherent beamforming. Phase noise of a VCO placed inside of a PLL is shaped in accordance to the PLL specifications and the reference signal phase noise characteristics. In a free running configuration, the phase noise of the VCO in the PLL does not change. On the other hand, when the VCO is operating inside a locked PLL, the phase noise of the locked VCO is referred to as PLL phase noise and is characterized by the transfer function of the PLL, where the noise is contributed using various blocks in the PLL. The PLL transfer function acts as a low pass filter for the phase noise contribution from the reference, phase frequency detector, divider, and charge pump, and as a high pass filter for the VCO phase noise, and the phase noise generated by the control line. Thus, within the loop bandwidth (up to the frequency of the loop filter f_{LF}), the phase noise contribution from the VCO and control line is suppressed. Consequently, the bandwidth of the PLL should be chosen at the point where the VCO phase noise intersects the close-in phase noise, which minimizes the PLL phase noise. If the PLL bandwidth is too low, a bump in the phase noise manifests beyond the loop cutoff frequency; if it is too high, the PLL noise floor extends, which is greater than the phase noise of the VCO. The close-in PLL phase noise in dBc is represented as [26]

$$L_0 = L_{PLL,nf} + 20 \log(N) + 10 \log(f_{ref}) \quad (6)$$

where $L_{PLL,nf}$ represents the PLL noise floor, which results from the specifics of its design. A typical PLL output phase noise is represented in Fig. 5; the first region represents the reference phase noise, the second is dominated by L_0 , and the third region is dominated by the phase noise of the VCO. While PLLs have a finite locking time to achieve a phase-locked state, this time is typically on the order of microseconds [26], [33], which is significantly shorter

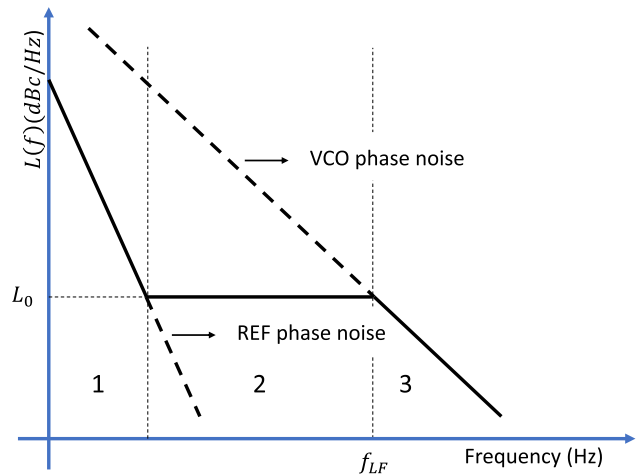


FIGURE 5. Typical PLL phase noise profile. In the first region, the PLL phase noise is dominated by the phase noise of the reference signal; in region 2, the PLL noise floor becomes higher than the phase noise of the reference signal; finally in region 3, the phase noise is dominated by the locked VCO. f_{LF} represents the frequency of the loop filter of the PLL, where this frequency needs to be selected appropriately to optimize the PLL phase noise.

than anticipated locking signals in a pulsed synchronization approach.

III. PHASE NOISE OF LOCKED AND UNLOCKED OSCILLATORS IN FREQUENCY AND TIME

A. TIME JITTER

In the time domain, fast fluctuations of the phase noise are represented as time jitter in seconds or phase jitter in radians. The jitter is extracted from the phase noise profile of the desired oscillator or PLL starting at frequencies 10 Hz and above. Below 10 Hz, the phase noise is dominated by the random walk FM noise which translates to drift in time and frequency, and is discussed below. To calculate the jitter, the integrated phase noise power A is obtained by evaluating the following equation

$$A = 10 \log (A_1 + \dots + A_n) \quad (7)$$

where the total area A from Figs. 3 or 5 (depending whether the oscillator is locked or unlocked) is broken into the separate areas A_1 through A_n . The areas represented by A_i can be calculated by

$$A_i = 10^{\{[L(f_i)+L(f_{i+1})]/2+10 \log(f_{i+1}-f_i)\}/10}. \quad (8)$$

The phase noise can be integrated until any desired frequency, depending on the application. Often it is integrated up to $f_0/2$, which is half of the nominal frequency for a given oscillator; this is the approach taken in this work. The RMS phase jitter is obtained from

$$\text{Phase Jitter} = \sqrt{2 \times 10^{A/10}}. \quad (9)$$

Similarly, the RMS time jitter is obtained from

$$\text{Time Jitter} = \frac{\text{Phase Jitter}}{2\pi f_0}. \quad (10)$$

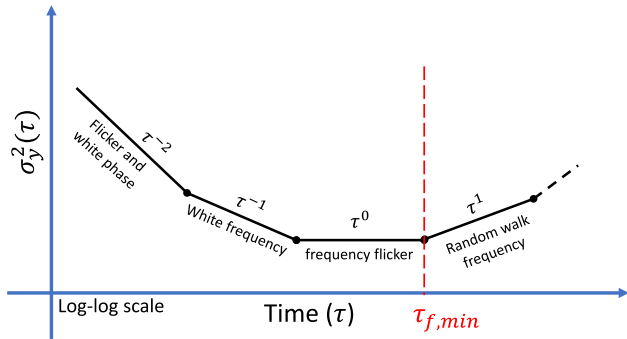


FIGURE 6. AVAR profile for an oscillator. $\tau_{f,min}$ represents the instance where the AVAR starts to become mainly dominated by the random walk FM noise. Later on, when analyzing the RMS frequency drift, it is important to select a value $\tau_f \geq \tau_{f,min}$.

B. ALLAN DEVIATION AND FREQUENCY DRIFT

The Allan variance (AVAR) and Allan deviation (ADEV) are measures of the frequency stability in oscillators, and are represented by $\sigma_y^2(\tau)$ and $\sigma_y(\tau)$ (the ADEV is the square-root of the AVAR). Both AVAR and ADEV can be a two-sample or M-sample variance and they are used with the notations $\sigma_y^2(M, T_s, \tau)$ and $\sigma_y(M, T_s, \tau)$, where T_s represents the time between measurements and τ the observation time for a single measurement. The commonly used AVAR for oscillators is $\sigma_y^2(\tau) = \langle \sigma_y^2(2, \tau, \tau) \rangle$, where $T_s = \tau$ and $M = 2$ [34]. The M-sample AVAR is obtained from

$$\sigma_y^2(M, T_s, \tau) = \frac{1}{M-1} \left\{ \sum_{i=0}^{M-1} \bar{y}^2(t+iT_s, \tau) - \frac{1}{M} \left[\sum_{i=0}^{M-1} \bar{y}(t+iT_s, \tau) \right]^2 \right\} \quad (11)$$

where \bar{y} is the average fractional frequency obtained from

$$\bar{y}(t, \tau) = \frac{1}{\tau} \int_0^\tau y(t+x)dx \quad (12)$$

here the average is taken over observation time τ , and $y(t)$ is the fractional-frequency error which can be obtained from

$$y(t) = \frac{f(t) - f_0}{f_0} \quad (13)$$

where $f(t)$ is the oscillator frequency and f_0 is the nominal frequency. The 2-sample variance $\sigma_y^2(\tau)$ can then be calculated from

$$\sigma_y^2(\tau) = \langle \sigma_y^2(2, \tau, \tau) \rangle = \frac{1}{2} \langle (\bar{y}(t+\tau, \tau) - \bar{y}(t, \tau))^2 \rangle. \quad (14)$$

AVAR or ADEV can be obtained from a phase noise profile [35], [36]; the curve in Fig. 3 is transformed in the calculation of $\sigma_y^2(\tau)$ to Fig. 6. The shape of the curve in Fig. 6 is analyzed in [37]. The main advantage in analyzing $\sigma_y^2(\tau)$ or $\sigma_y(\tau)$ is that it is possible to study the random frequency drifts in a frequency locked or unlocked oscillator which are challenging to detect using the phase noise data.

The ADEV is interpreted as follows: an ADEV of 10^{-11} for $\tau = 1$ s represents an instability in frequency between two observations 1 s apart with a relative RMS value of 10^{-11} . Thus, for a 100 MHz oscillator, this is equivalent to

0.001 Hz RMS drift for 1 s update time or 1 Hz update rate. Thus, the RMS frequency drift values for the update times of interest can be obtained using

$$\text{RMS Frequency Drift} = \sigma_y(\tau_f) f_0 \sqrt{\frac{T}{\tau_f}} \quad (15)$$

where T is the update time and τ_f is chosen once the random frequency walk asymptote τ becomes visible in the AVAR, ideally at $\tau_{f,min}$ in Fig. 6. A proper selection of τ_f is necessary in order to have accurate estimates for the RMS frequency drift. Starting from $\tau_{f,min}$ the variance in the AVAR plot is dominated by the random walk FM noise.

The RMS frequency drift in (15) is shaped by the phase noise of the input reference signal if the VCO is locked using a PLL, whereas in the case of a free running VCO, the RMS frequency drift is shaped by the phase noise of the VCO itself even if it is placed in a PLL. In coherent distributed arrays, if all secondary nodes are locked using a continuous reference input signal, the evaluation of RMS frequency drift is not necessary since all the oscillators in the array will drift synchronously; i.e. there is no relative drift between the oscillators. On the other hand, if the secondary nodes are frequency locked using pulsed reference signals, the oscillators of the secondary nodes will drift differently in comparison to each other between synchronization intervals; in this case it is important to evaluate the frequency drift at the end of the update interval to assess the worst potential errors between nodes.

C. TIME DRIFT

The RMS time drift for an oscillator can be extracted in a similar fashion to the RMS frequency drift, but instead of analyzing the ADEV measurements, it is determined by analyzing the time deviation (TDEV) data which is obtained by measuring the standard deviation of the timing errors in an oscillator. TDEV is recorded for various observation times τ , and in order to properly estimate the RMS time drift, it is important to select the appropriate observation time τ_t , which represents the observation time at which the effect of time drift dominates that of time jitter; thus τ_t is chosen for the time when the TDEV starts to have a positive slope, similar to how τ_f is obtained for the ADEV. The RMS time drift can be estimated for various update times through

$$\text{RMS Time Drift} = \text{TDEV}(\tau_t) \sqrt{\frac{T}{\tau_t}}. \quad (16)$$

Similarly to the RMS frequency drift, the RMS time drift needs to be evaluated in the case where the input reference signals are not continuous.

IV. DISTRIBUTED BEAMFORMING ANALYSIS

The performance of a distributed beamforming operation can be characterized in various ways, but often the most straightforward one is to evaluate the obtainable gain in the mainbeam of a distributed beamforming operation with phase

errors relative to an ideal distributed beamforming operation. In particular, we evaluate the coherent gain G_c , defined by

$$G_c = \frac{|s_r s_r^*|}{|s_i s_i^*|} \quad (17)$$

where $s_r = \sum_{n=1}^N s_r(n)$ is the summation of the signals from the distributed transmitters with phase noise, $s_i = \sum_{n=1}^N s_i(n)$ is the ideal summation of the transmitted signals without noise; the coherent gain is thus bounded by $0 \leq G_c \leq 1$. The coherent gain is a general metric that can be tied directly to signal strength and signal-to-noise ratio (SNR), therefore, it can be used to characterize the performance of any wireless operation, such as the increase in throughput of communications systems or the detection performance of radars.

Generally, the received signal at the far field from a network of N arbitrarily placed transmitting nodes can be represented by

$$s_r = \sum_{n=1}^N h_n A_n(t - \delta t(n)) \times e^{j[2\pi(f + \delta f(n))t + \phi_{s,n} - \phi_{c,n} + \delta \phi(n)]} \quad (18)$$

where h_n is the complex valued coefficient representing the propagation channel, A_n is the signal amplitude, $\delta t(n)$ represents the timing error, f is the signal frequency, $\delta f(n)$ is the frequency error, $\phi_{s,n}$ is the phase shift, $\phi_{c,n}$ is the correction applied to the phase shift which can be obtained through node localization, and $\delta \phi(n)$ is the instantaneous frequency and phase errors obtained from multiple factors. There are thus many factors that influence the ability to coherently transmit a signal from a collection of separate nodes, involving the system hardware, the internode coordination, and the environment. Since in this work we focus on phase noise induced errors, only the coherent gain degradation due instantaneous phase, frequency, and time errors is evaluated. Performance degradation due to errors in the calibration of propagation channel, phase, frequency, and time can be studied separately and evaluated as a compounded error.

We formulate the coherent gain in terms of the phase noise parameters described in Section III. To do this, we consider two scenarios: transmission of a CW signal, where phase errors are important but relative timing is not; and transmission of a signal with an arbitrary modulation where timing is necessary to ensure that the information carried in the transmitted signals appreciably overlaps at the target location. We denote the signals for each scenario as $s_{r,k}$ and $s_{i,k}$, where $k = 1$ in the unmodulated case and $k = 2$ in the modulated case; $s_{i,1}(n)$ can be represented as

$$s_{i,1}(n) = e^{j\left(\frac{f_c(n)}{f_0}(2\pi t f_0)\right)} \quad (19)$$

where $f_c(n)$ carrier frequency for node n . The received signal with errors is given by

$$s_{r,1}(n) = e^{j\left(\frac{f_c(n)}{f_0}(2\pi t[f_0 + \delta f(n)] + [\phi_0(n) + \delta \phi(n)]\right)} \quad (20)$$

where $\delta f(n)$ represents the frequency drift for the n^{th} oscillator, taken from a normal distribution with a standard deviation equal to the RMS value in (15), $\delta \phi$ represents the phase jitter, taken from a normal distribution with a standard deviation equal to the RMS value in (9), and ϕ_0 is used to adjust the initial phase at a desired observation time.

Since the signal model in (20) has a frequency offset $\delta f(n)$ varying over time as shown in (15), the phase in (20) must be adjusted to reflect the behavior of the changing frequency over time. At short intervals, the frequency offset can be approximated as changing linearly with a slope of t/T (this represents the average case), thus the phase at time T can be given by

$$\phi_{actual} = 2\pi \int_0^T f_0 + \frac{t}{T} \delta f(n) dt. \quad (21)$$

The total phase error at time T is then

$$\phi_0 = \phi_{actual} - 2\pi \int_0^T f_0 + \delta f(n) dt. \quad (22)$$

In the second scenario where the array transmits modulated waveforms, a binary phase-shift keying (BPSK) signal [38] was considered to represent a basic modulation format, where a modulation/phase mismatch results in nulling the beamformed signals. The bit rates were varied depending on the transmitted carrier; the results are general for pulse modulated waveforms of the same bandwidth. The ideal received signal $s_{i,2}(n)$ is given by

$$s_{i,2}(n) = \cos\left(\frac{f_c(m)}{f_0}(2\pi t f_0) + \pi(1 - b(t))\right) \quad (23)$$

where $b(t) = 0$ or 1 . The received signal with errors $s_{r,2}(n)$ is given by

$$s_{r,2}(n) = \cos\left(\frac{f_c(m)}{f_0}(2\pi t(f_0 + \delta f(n)) + \phi_0(n) + \delta \phi(n)) + \pi(1 - b(t + \delta t(n)))\right) \quad (24)$$

where $b(t + \delta t(n))$ is the desired bit for the time $t + \delta t(n)$ and $\delta t(n)$ represents both the time drift and jitter and is taken from a normal distribution with a standard deviation equal to the RMS value in (10). This normal distribution has a random offset equal to the random time drift, obtained from a normal distribution with standard deviation equal to RMS time drift obtained from (16).

V. PRACTICAL EXAMPLES

In this section we use the above framework to evaluate the impact on coherent beamforming gain in a distributed phased array in the presence of oscillator phase noise in multiple examples. We consider an array of multiple scattered nodes and use a threshold performance metric of $G_c \geq 0.9$, indicating that the distributed beamforming operation achieves 90% of the ideal beamforming gain (a degradation of less than 0.5 dB). We consider array sizes $N = 2, 10, 20$,

TABLE 1. SSB phase noise of the selected 100 MHz oscillators.

	VCO A	VCO B
$f_1 = 10$ Hz	-60 dBc/Hz	-110 dBc/Hz
$f_2 = 100$ Hz	-90 dBc/Hz	-140 dBc/Hz
$f_3 = 1$ kHz	-120 dBc/Hz	-165 dBc/Hz
$f_4 = 10$ kHz	-145 dBc/Hz	-185 dBc/Hz
$f_0/2 = 50$ MHz	-155 dBc/Hz	-190 dBc/Hz

and 100. We evaluate performance bounds on the mainbeam gain at frequencies extending from the microwave to the millimeter-wave bands, using two nominal 100 MHz oscillator phase noise profiles. First, we analyze the coherent gain in the presence of the reference signal being transmitted continuously without interruptions. Next, we evaluate the coherent gain for the case where the reference signal is transmitted using pulsed waveforms with a varying update time T . The reference signal is assumed to be broadcast wirelessly from an arbitrary location within the array. Each node receives the reference signal and inputs it to its PLL. As noted above, the locking time for a typical PLL is on the order of microseconds; it is reasonable to assume that the pulsed reference signal is of a sufficiently longer duration to support locking. We consider two oscillator phase noise profiles as shown in Table 1; VCO A represents a typical VCO, while VCO B represents a low phase noise VCO. The phase noise data, ADEV and TDEV used in this work are similar to what is available in the market or in the literature such as in [15], [39]–[41].

The phase noise of the VCO inside of a PLL has two possible phase noise behaviors depending on the locking status of the PLL. When the PLL is not receiving the frequency locking signals, the VCO is in a free-run mode, and the PLL output phase noise will correspond solely to that of the VCO. On the other hand, when the PLL is frequency locked, its phase noise will have a shape similar to that in Fig. 5. In this work we evaluate the coherent gain in a coherent distributed array for three architectures: 1) the reference signal generated using VCO A (the high-phase noise oscillator) and the secondary nodes are equipped with the same VCO A; 2) the reference signal generated using VCO B (the low-phase noise oscillator) and the secondary nodes are equipped with the same VCO B; and 3) the reference signal generated using VCO B from an external transmitter and the secondary nodes are equipped with VCO A. The case where the reference signal is generated using VCO A from an external transmitter and the secondary nodes are equipped with VCO B was not considered since in this case the phase noise of the reference VCO will be much higher than the phase noise of the VCOs used by the secondary nodes, which leads to an overall system performance similar to the first architecture.

Two assumptions are considered in this section; first, we assume that the phase noise profile of the input reference signal matches that of the reference oscillator. In practice, the phase noise is usually higher for the input reference signal since a large path loss might be present between the primary

and secondary nodes which would lead to a decrease in the received signal SNR on the secondary node. This decrease in signal power then may lead to an increase in white phase noise. In addition to that, interference might be present which would increase the phase noise. In order to deal with this assumption in practice, it is possible to estimate the phase noise of the input reference signal for the worst-case scenario to estimate a bound on beamforming performance. Second, we consider the case where no frequency multiplication or division is needed (which is the case when the frequency of the input signal is equal to the nominal frequency of the oscillator). In this case the phase noise of the input reference signal is equal to the phase noise of the input signal to the PLL. If the reference frequency requires multiplication/division by a factor M , the phase noise of input reference increases/decreases by a factor of $20 \log(M)$.

In the case where the same VCO is used as the reference and PLL VCO, the phase noise of the continuously locked PLL will resemble the phase noise of the VCO, since region 1 in Fig. 5 will overlap region 3. This means that the phase noise characteristics of the VCOs can be considered as the phase noise characteristics at the output of the PLL for architectures 1 and 2. For the third architecture, the phase noise at the output of the locked PLL will resemble that of Fig. 5. The close-in phase noise of the PLL was taken to be -130 dB/Hz until the frequency of the loop filter (matching typical PLL values), with a rapid decrease in magnitude beyond that point. In all the architectures, the loop filter was assumed to be appropriately selected to match the profile in Fig. 5. Based on the values in Table 1 and the approximated close-in phase noise of the PLL, the phase noise of the PLL for the three selected architectures is shown in Fig. 7.

For VCO A, the RMS of the phase jitter is equal to 2.7×10^{-3} rad and the RMS of the time jitter is equal to 4.37×10^{-12} s, calculated from (9) and (10), respectively. For VCO B, the RMS of the phase jitter is equal to 9.95×10^{-6} rad and the RMS of the time jitter is equal to 1.58×10^{-14} s. For the third architecture, when the nodes are continuously locked, the RMS of the phase jitter is equal to 1.85×10^{-4} rad and the RMS of the time jitter is equal to 2.95×10^{-13} s; in the intervals where the VCOs are not frequency locked, their RMS phase jitter and RMS time jitter are equal to that of their internal VCOs (VCO A in this case). The ADEV for VCO A at $\tau_f = 1$ s is $\sigma_y(1) = 10^{-10}$, while for VCO B at $\tau_f = 1$ s it is $\sigma_y(1) = 2.3 \times 10^{-12}$. The selected TDEV at $\tau_t = 1$ s for VCO A is $\text{TDEV}(1) = 8 \times 10^{-11}$ s, while for VCO B at $\tau_t = 1$ s it is $\text{TDEV}(1) = 2 \times 10^{-12}$ s. τ_f and τ_t values were inspired by datasheets of available VCOs in the market such as in [39]; a common practice is to show in the datasheets either the entire ADEV data of the VCO or to report τ_f at 1 s since this value is usually close to $\tau_{f,min}$; similar practice is done in regards to TDEV. Whenever the entire data for ADEV and TDEV is present, it is preferable to select the values of τ_f and τ_t at $\tau_{f,min}$ and $\tau_{t,min}$ since these values tend to capture the worst case scenario.

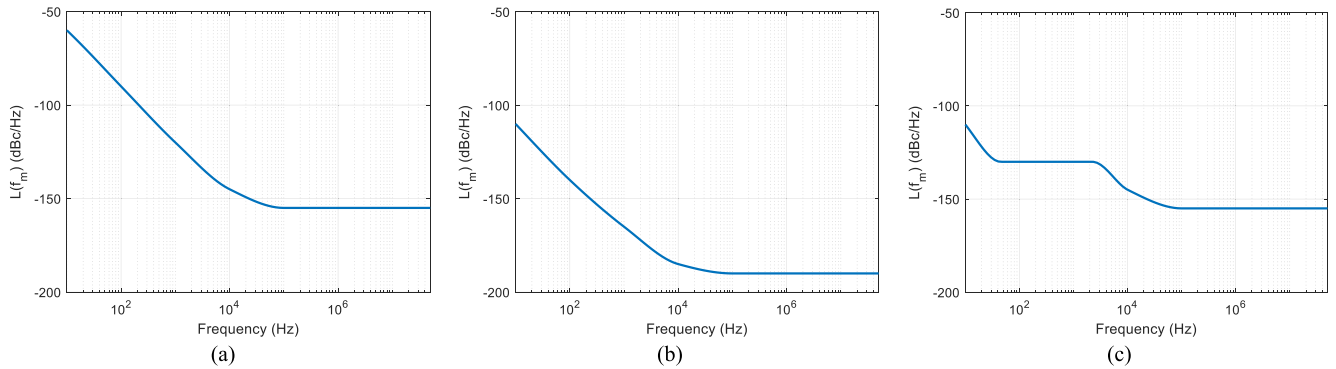


FIGURE 7. Phase noise of the locked PLLs for architectures: (a) 1, (b) 2, and (c) 3. In architecture 1, VCO A was being locked by the PLLs of the secondary nodes and it was used to generate the reference signals. In architecture 2, VCO A was replaced by VCO B. In architecture 3, VCO B was used to generate the reference signals, while VCO A was being locked by the PLLs of the secondary nodes. In all the architectures, the loop filter was assumed to be designed appropriately to minimize the phase noise of the PLLs.

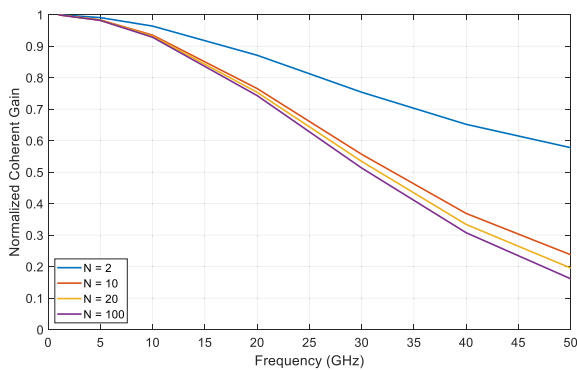


FIGURE 8. Coherent gain for various carrier frequencies for arrays of sizes $N = 2, 10, 20,$ and 100 with continuous locking for architecture 1 (using the high phase noise oscillator as the reference and PLL VCO) with the phase noise profile from Fig. 7a.

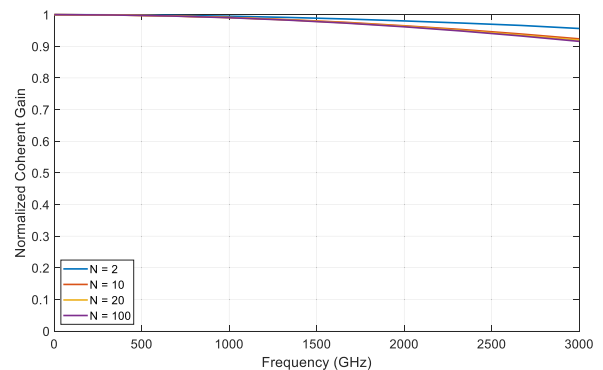


FIGURE 9. Coherent gain for various carrier frequencies for arrays of sizes $N = 2, 10, 20,$ and 100 with continuous locking for architecture 2 (using the low phase noise oscillator as the reference and PLL VCO) with the phase noise profile from Fig. 7b.

A. BEAMFORMING PERFORMANCE WITH CONTINUOUS SYNCHRONIZATION

When the PLLs of the secondary nodes receive the reference signal continuously without interruption, there are no relative frequency or time drifts, and furthermore the effects of timing errors are negligible (many orders of magnitude less than frequency errors). Thus, the signals can be modeled as in (20) with $\delta f(n) = 0$. The principal performance parameter is thus the carrier frequencies f_c that are supported by the chosen VCOs for distributed beamforming. Generally, with continuous locking, even oscillators with moderate to poor phase noise can support good distributed beamforming performance up to millimeter-wave frequencies. The coherent gain was plotted for the three architectures, multiple array sizes, and multiple f_c values; 1,000 Monte Carlo simulations were run for carrier frequencies up to 50 GHz for architecture 1, as for the second architecture, frequencies up to 3 THz were considered, and for the third architecture, frequencies up to 1 THz were evaluated. The results for architecture 1 are shown in Fig. 8. As it can be seen, when two nodes are used, at least 90% coherent gain can be achieved for frequencies below 17 GHz. As for the other array sizes, at least 90% coherent gain is achievable for frequencies below 12 GHz.

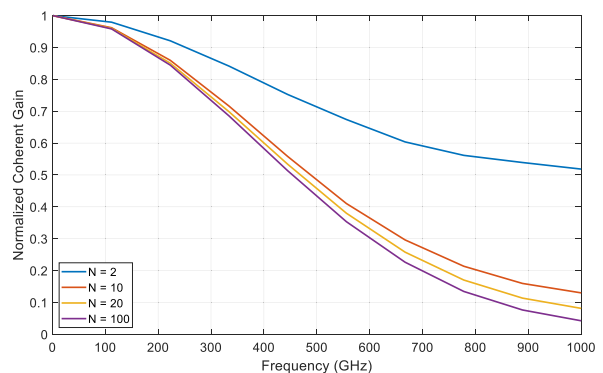


FIGURE 10. Coherent gain for various carrier frequencies for arrays of sizes $N = 2, 10, 20,$ and 100 with continuous locking for architecture 3 (using the low phase noise oscillator as the reference and the high phase noise oscillator as the PLL VCO) with the phase noise profile from Fig. 7c.

The results for architecture 2 are shown in Fig. 9. For all the array sizes that were used, much higher than 90% coherent gain can be achieved for frequencies higher than 3 THz. This frequency is very high for coherent distributed arrays, and in practice it is not feasible since there will be many other sources leading to phase errors. Nevertheless, this shows that the phase noise in the selected oscillator will not be a limiting factor for coherent transmission even at very high carrier

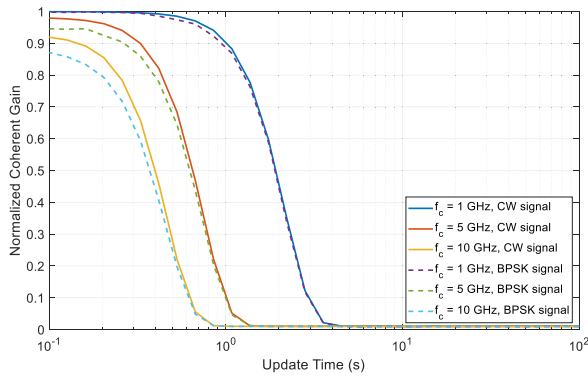


FIGURE 11. Coherent gain for CW and BPSK signals with periodic synchronization, where the jitter and frequency drifts (CW and BPSK), and timing errors (BPSK) were considered for nodes equipped with VCO A. Array size $N = 100$ was selected.

frequencies. Regarding the third architecture, the results are shown in Fig. 10. When two nodes are used, at least 90% coherent gain can be achieved for frequencies below 252 GHz. As for the other array sizes, at least 90% coherent gain is achievable for frequencies below 160 GHz. Clearly, continuous synchronization provides good distributed beamforming performance; if a low phase noise oscillator is used as the reference, good performance well beyond 100 GHz is attainable.

B. BEAMFORMING PERFORMANCE WITH PERIODIC SYNCHRONIZATION WITH PHASE AND FREQUENCY ERRORS

Practically, continuous synchronization is challenging to obtain in distributed beamforming. Here we analyze the impacts of periodic synchronization on beamforming performance. Due to the inherent drift of the oscillators, periodic synchronization is necessary, even with low phase noise oscillators. We analyze in this section the phase and frequency errors without considering the time jitter and time drift, an approach supporting CW beamforming without modulation; the transmitted signals are thus modeled as in (20). The coherent gain was analyzed for update times T between 100 ms and 100 s. 1000 Monte Carlo simulations were generated for the carrier frequencies of 1, 5, and 10 GHz, and the coherent gain was calculated for arrays with 100 elements (larger arrays generally yield more stringent requirements, as seen in Section V-A). The coherent gain was calculated for the last 100 wavelengths before the next update time to evaluate the worst case scenario, since the last few wavelengths represent the signal with the maximum drift before the next update. The phase noise profile for architectures 1 and 3 was obtained from the phase noise of VCO A, since the VCOs are free running, and the phase noise in architecture 2 was obtained from the phase noise of VCO B. The results are shown in Fig. 11 for architectures 1 and 3, and in Fig. 12 for architecture 2. When the high phase noise oscillator is used in a free-run mode or in the locked PLL, the jitter causes appreciable coherent gain degradation at higher frequencies,

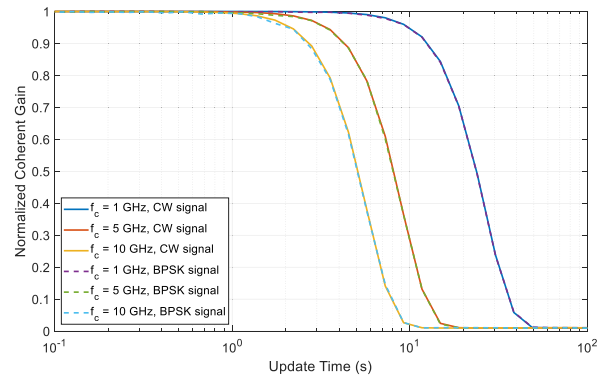


FIGURE 12. Coherent gain for CW and BPSK signals with periodic synchronization, where the jitter and frequency drifts (CW and BPSK), and timing errors (BPSK) were considered for nodes equipped with VCO B. Array size $N = 100$ was selected.

indicated by the fact that the curves never reach the ideal value of $G_c = 1$. Furthermore, update frequencies above 1 Hz are necessary to achieve reasonable coherent gain values. When the low phase noise oscillator is used as both reference and PLL VCO, the gain achieves the ideal value for relatively low update frequencies extending below 1 Hz.

C. BEAMFORMING PERFORMANCE WITH PERIODIC SYNCHRONIZATION WITH PHASE, FREQUENCY, AND TIMING ERRORS

In this section we consider modulated waveforms where timing is relevant, and perform the same analysis as in Section V-B with the addition of the timing errors, thus using (24) for the signal model. The BPSK signal was transmitted at bit rates relative to the transmitted carrier frequencies; for carrier frequencies of 1, 5, and 10 GHz, the bit rates were 100, 500, and 1000 Mbit/s. High bit rates were chosen to capture the effect of the timing errors in the worst case scenarios. Results for $N = 100$ are shown in Figs. 11 and 12 for the three architectures as explained in Section V-B. It can be seen that the timing errors have a small impact on the coherent gain, even for very high modulation rates. This result is expected since the timing requirements for a coherent operation are relative to the symbol rate, whereas the requirements for frequency and phase synchronization are relative to the carrier frequency. The degradation in coherent gain is more visible for VCO A since it had high TDEV in comparison to VCO B. It can be seen that in Fig. 11 the initial coherent gain for the 5 and 10 GHz carrier frequencies has dropped for the BPSK signals in comparison to the CW signals. Also, the decrease in coherent gain started at a slightly reduced update time for the BPSK transmission. Timing errors had a smaller effect in Fig. 12 due to the better stability of the oscillator.

The maximum carrier frequencies that can be achieved with 90% Coherent gain where the jitter, frequency drifts, and timing errors are considered for VCOs A (representing architectures 1 and 3) and B (representing architecture 2) with $N = 2$ and 100 in Fig. 13, demonstrating that the low

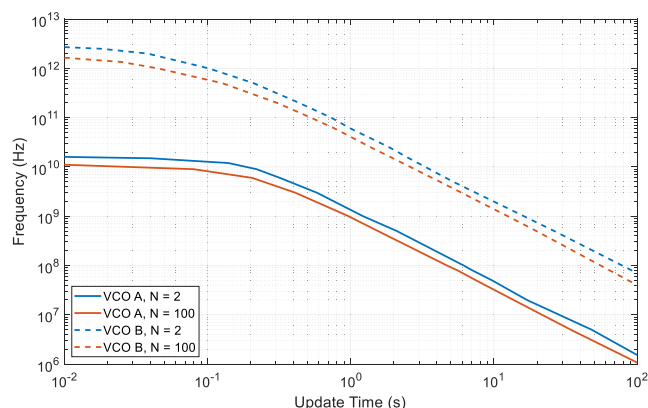


FIGURE 13. Carrier frequencies supporting 90% coherent gain for periodic synchronization with array sizes $N = 2$ and 100 , where the jitter, frequency drifts and timing errors were considered for nodes equipped with either VCO A or VCO B.

phase noise oscillator generally supports higher operating frequencies with longer update intervals.

VI. CONCLUSION

Distributed beamforming performance is highly dependent on the stability of the oscillators and whether the nodes in the array are synchronized continuously or periodically. We investigated the effects of oscillator- and PLL-induced errors in distributed beamforming arrays, providing a framework for analyzing the beamforming performance of a distributed array relative to metrics that are available in oscillator and PLL datasheets. We provided practical examples of the beamforming performance of a high phase noise oscillator and a low phase noise oscillator in three different architectures, considering phase jitter, time jitter, frequency drift, and time drift. The achievable coherent gain in a coherent distributed array with $N = 2, 10, 20,$ and 100 nodes was studied where only the errors produced by the oscillators were considered. We showed how the choice of oscillators, PLLs, and beamforming frequencies affected the required synchronization rates. With high beamforming frequencies, higher synchronization rates are needed to prevent significant degradation of the beamforming gain. Nevertheless, even with continuous frequency synchronization the phase jitter of the oscillators sets an upper bound on the possible beamforming frequencies. Timing errors had small to negligible effect on the beamforming gain for modulated signals, especially for the oscillator with low phase noise.

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