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Impedance-Based Stability and Transient-Performance Assessment Applying Maximum Peak Criteria

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***Abstract*—The impedance-based stability-assessment method has turned out to be a very effective tool and its usage is rapidly growing in different applications ranging from the conventional interconnected dc/dc systems to the grid-connected renewable energy systems. The results are sometime given as a certain forbidden region in the complex plane out of which the impedance ratio—known as minor-loop gain—shall stay for ensuring robust stability. This letter discusses the circle-like forbidden region occupying minimum area in the complex plane, defined by applying maximum peak criteria, which is well-known theory in control engineering. The investigation shows that the circle-like forbidden region will ensure robust stability only if the impedance-based minor-loop gain is determined at the very input or output of each subsystem within the interconnected system. Experimental evidence is provided based on a small-scale dc/dc distributed system.**

***Index Terms*—Minor-loop gain, sensitivity function, stability, switched-mode converter, transient performance.**

I. Introduction

THE foundation of the impedance-based stability and transient-performance analyses have been laid down in the mid-1970s by R. D. Middlebrook when publishing his famous input-filter design rules for a regulated converter in [1] and [2]. Since then, the minor-loop gain composing of the internal impedances of the downstream and upstream subsystems has been frequently used to assess the stability of interconnected systems in different application areas [3]–[23]. It has been recently noticed that the impedance ratio has to be computed in a certain way for predicting correctly the stability in the voltage- and current-fed applications [22], [23]: the numerator impedance has to be the internal impedance of the subsystem containing the voltage source or sink, and the denominator impedance the internal impedance of the subsystem containing the current sink or source, respectively.

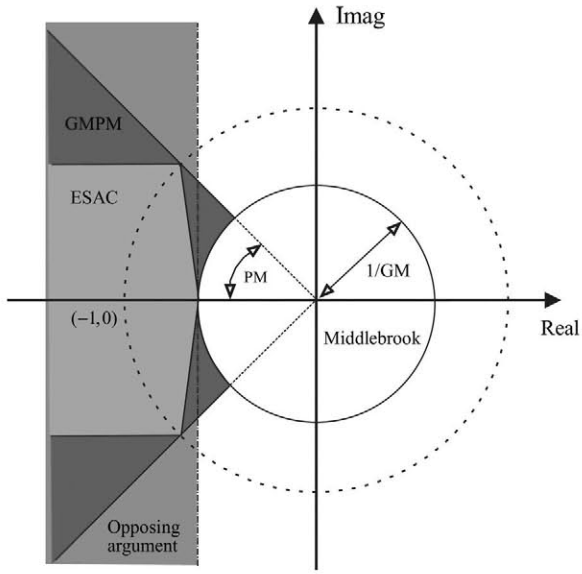


Fig. 1. Collection of forbidden regions in the complex plane according to [1]–[5].

It has been earlier customary to present the impedance-ratio-based stability regions as certain forbidden regions in the complex plane out of which the minor-loop gain shall stay for robust stability to exist as shown in Fig. 1. Middlebrook's input-filter design rules [1], [2] are considered to produce the forbidden region, which locates outside the circle having the center at origin and the radius of inverse of gain margin (GM). This has been considered to be quite conservative and cost inefficient to apply in general [3]. As a consequence, other less conservative forbidden regions or criteria have been proposed such as, e.g., energy systems analysis consortium (ESAC) [3], gain margin and phase margin (GMPM) [4], and opposing argument [5] criteria. According to Fig. 1, the least restrictive criterion is the ESAC criterion. Another less restrictive criterion has been proposed in [6]–[8], which is discussed more in detail in Section III. A comprehensive survey of forbidden regions can be found, e.g., in [9].

The design rules in [1] and [2] are developed to ensure robust stability as well as maintaining original transient performance intact when the *LC* filter is connected at the input terminal of a converter. Basically, all the criteria in [3]–[9] are developed to meet the same goals as in [1] and [2] but intended for more

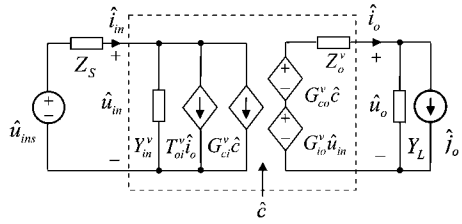


Fig. 2. Linear model of the VF–VO converter with nonlinear source Z_S and load Y_L.

general application areas than the source interactions caused by the input filter.

The whole set of Middlebrook's input-filter design rules imply that the requirements set for the minor-loop gain are insufficient to guarantee intact transient behavior as such but another implicit impedance parameter exists (i.e., input impedance at short-circuited output [10], [24], [25]) in terms of which no source-impedance intersection is allowed for ensuring intact transient performance.

This letter discusses the application of the circle-like forbidden region based on the application of the maximum peak criteria (MPC), which are well-known criteria in control engineering to design loop gains for ensuring robust stability [26]. The application of such a forbidden region is proposed earlier in [6]–[8] and applied recently, e.g., in [19] to assess the stability of a renewable energy-based microgrid. The forbidden region occupies much less space in the complex plane (i.e., the absolute minimum from the point of view of robust stability) than the previous criteria depicted in Fig. 1, and maintains the same level of robustness or even better. Although the discussions in this letter are limited to the conventional voltage-fed (VF) converters, the presented ideas and discussions are equally valid for different applications when the minor-loop gain and the relevant impedances are correctly defined as discussed in [13]–[15], [22], and [23]. The validity of the impedance-based minor-loop gain in assessing the stability of a general interconnected system at an arbitrary interface is proved explicitly in [11] and [22] based on system theory. The main contributions of this letter are the explicit revelation of the basis for the MPC-based forbidden region and the validity of the information extractable from the application of the criteria in terms of robustness of the stability in respect to the interface the minor-loop gain is determined.

The rest of this letter is organized as follows. The source and load-affected dynamic descriptions including the implicit impedance parameters and the stability assessment principles are briefly introduced in Section II. The MPC-based forbidden region is developed and compared to the other existing forbidden regions in Section III. Section IV provides experimental evidence, and the conclusions are drawn finally in Section V.

II. Source and Load-Interaction Formulation

The linear model of a conventional VF voltage-output (VO) converter can be given as shown in Fig. 2 inside the dashed line, where the superscript "v" denotes the voltage nature of the converter. The nonideal source and load are represented by the source impedance Z_S and the load admittance Y_L, while the general control variable is denoted by $\hat{c}$. This model is equally valid both at open and closed loops. An equivalent presentation for the linear model is given in (1) as a set of simultaneous equations from which the meaning of each transfer function can be easily deduced

$$\begin{cases} \hat{i}_{\rm in} = Y_{\rm in}^v \cdot \hat{u}_{\rm in} + T_{\rm oi}^v \cdot \hat{i}_o + G_{\rm ci}^v \cdot \hat{c} \\ \hat{u}_o = G_{\rm io}^v \cdot \hat{u}_{\rm in} - Z_o^v \cdot \hat{i}_o + G_{\rm co}^v \cdot \hat{c}. \end{cases} \tag{1}$$

The source-affected set of transfer functions can be determined from Fig. 2 by computing $\hat{u}_{\rm in}$ and substituting it into (1) with its new formulation. These procedures yield (2), where the implicit parameters $Y_{{\rm in}-\infty}^v$ and $Y_{{\rm in}-{\rm sco}}^v$ are ideal and short-circuit input admittances defined in (3). These special admittances are the same at open and closed loops

$$\begin{cases} \hat{i}_{\rm in} = \dfrac{Y_{\rm in}^v}{1+Z_S Y_{\rm in}^v} \cdot \hat{u}_{\rm ins} + \dfrac{T_{\rm oi}^v}{1+Z_S Y_{\rm in}^v} \cdot \hat{i}_o + \dfrac{G_{\rm ci}^v}{1+Z_S Y_{\rm in}^v} \cdot \hat{c} \\ \hat{u}_o = \dfrac{G_{\rm io}^v}{1+Z_S Y_{\rm in}^v} \cdot \hat{u}_{\rm ins} - \dfrac{1+Z_S Y_{{\rm in}-{\rm sco}}^v}{1+Z_S Y_{\rm in}^v} Z_o^v \cdot \hat{i}_o \\ \qquad + \dfrac{1+Z_S Y_{{\rm in}-\infty}^v}{1+Z_S Y_{\rm in}^v} G_{co}^v \cdot \hat{c} \end{cases} \tag{2}$$

$$Y_{{\rm in}-\infty}^v = Y_{\rm in}^v - \frac{G_{\rm io}^v G_{\rm ci}^v}{G_{\rm co}^v}$$

$$Y_{{\rm in}-{\rm sco}}^v = Y_{\rm in}^v + \frac{G_{\rm io}^v T_{\rm oi}^v}{Z_o^v}. \tag{3}$$

Correspondingly, the load-affected set of the transfer functions can be determined from Fig. 2 by computing $\hat{i}_o$ and substituting it into (1) with its new formulation. These procedures yield (4), where the implicit parameters $Z_{o-\infty}^v$ and $Z_{o-{\rm oci}}^v$ are ideal and open-circuit output impedances defined in (5). $Z_{o-\infty}^v$ is the same at open and closed loops but $Z_{o-{\rm oci}}^v$ depends on the state of feedback as indicated in (5)

$$\begin{cases} \hat{i}_{\rm in} = \dfrac{1+Z_{o-{\rm oci}}^v Y_L}{1+Z_o^v Y_L} Y_{\rm in}^v \cdot \hat{u}_{\rm in} + \dfrac{T_{\rm oi}^v}{1+Z_o^v Y_L} \cdot \hat{j}_o \\ \qquad + \dfrac{1+Z_{o-\infty}^v Y_L}{1+Z_o^v Y_L} G_{\rm ci}^v \cdot \hat{c} \\ \hat{u}_o = \dfrac{G_{\rm io}^v}{1+Z_o^v Y_L} \cdot \hat{u}_{\rm in} - \dfrac{Z_o^v}{1+Z_o^v Y_L} \cdot \hat{j}_o + \dfrac{G_{\rm co}^v}{1+Z_o^v Y_L} \cdot \hat{c} \end{cases} \tag{4}$$

$$Z_{o-\infty}^v = Z_o^v + \frac{G_{\rm io}^v G_{\rm co}^v}{G_{\rm ci}^v}$$

$$Z_{o-{\rm oci}}^v = Z_o^v + \frac{G_{\rm io}^v T_{\rm oi}^v}{Y_{\rm in}^v} = \frac{Z_o^v}{Y_{\rm in}^v} \cdot Y_{{\rm in}-{\rm sco}}^v. \tag{5}$$

The source and load-side minor-loop gains in (2) and (4) are $Z_S Y_{\rm in}^v$ and $Z_o^v Y_L$, respectively, where the internal input admittance and output impedance are usually considered to be their closed-loop values. Even if these minor-loop gains are designed to provide robust stability and transient performance, the transient behavior may be affected because of the source or load impedance intersections with the implicit impedance

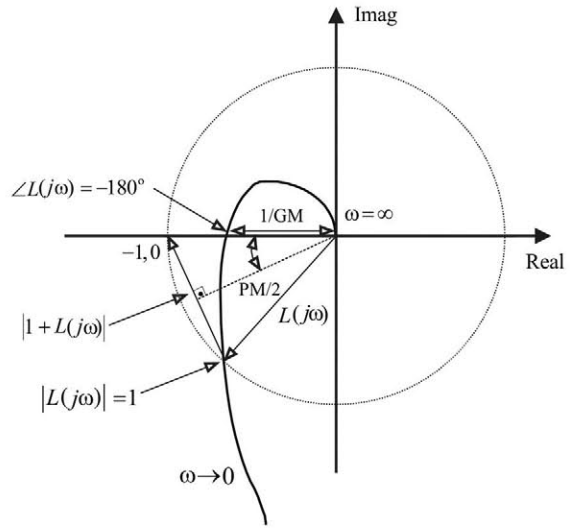


Fig. 3. PM and GM margin definitions [12].

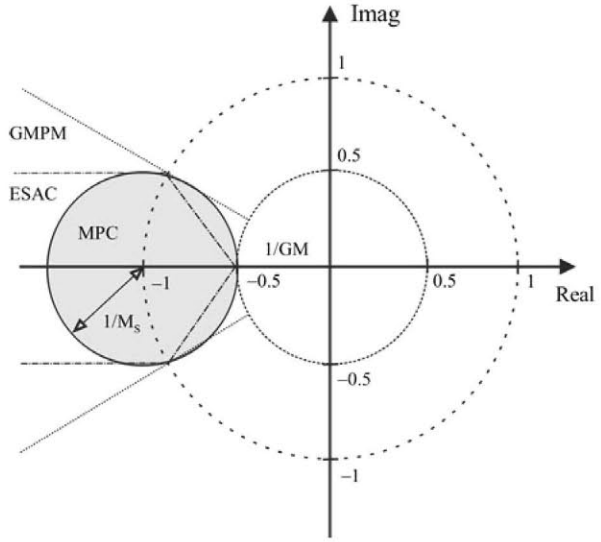


Fig. 4. MPC-based forbidden region versus ESAC and GMPM regions.

parameters in (2) and (4). The instability can occur also equally at open loop if the open-loop minor-loop gains do not satisfy the Nyquist stability criterion [11]. Such a situation applies, e.g., to the input-voltage-feedforward-controlled buck converter, which can be used as a bus converter in intermediate bus architectures without output-side feedback control, because of its negative-incremental input impedance at open loop [27], [28].

III. Maximum Peak Criteria

The small-signal output voltage of the output-voltage-feedback-controlled converter can be given according to (6), where $1/(1+L_{\rm out})$ and $L_{\rm out}/(1+L_{\rm out})$ are known as the sensitivity function S and complementary sensitivity function T in control engineering [26]. In (6), the open-loop transfer function is indicated by a subscript extension "$-o$," the output-voltage sensing gain as $G_{\rm se}$, and $L_{\rm out}$ denotes the output-voltage loop gain. It is well known that low phase margin (PM) and/or GM in the voltage loop ($L_{\rm out}$) (see Fig. 3 for the definitions of PM and GM) would cause resonant behavior (i.e., peaking) in the corresponding closed-loop transfer functions. The amount of peaking can be expressed in terms of PM ($|S_{\max}|_{\rm PM}$) and GM ($|S_{\max}|_{\rm GM}$) as given in (7) at the crossover frequencies of the gain and phase of the voltage loop [26]. The minor-loop gains in (2) and (4) form similar sensitivity functions as the voltage loop but based on the impedance ratios. Therefore, low margins in the minor-loop gain would cause peaking in the corresponding sensitivity function according to (7) and consequently, in the corresponding transfer functions in (2) and (4) [26]. It should be noted that the full effect of the described peaking affects only the internal or unterminated transfer functions of the corresponding converter, which is also the basic assumptions behind the MPC theory in [26]

$$\hat{u}_o = \frac{G^v_{{\rm io}-o}}{1+L_{\rm out}}\hat{u}_{\rm in} - \frac{Z^v_{o-o}}{1+L_{\rm out}}\hat{i}_o + \frac{L_{\rm out}}{G_{\rm se}(1+L_{\rm out})}\cdot\hat{c} \qquad (6)$$

$$|S_{\max}|_{\rm PM} = \frac{1}{\sqrt{2(1-\cos({\rm PM}))}} = \frac{1}{2\sin({\rm PM}/2)}$$

$$|S_{\max}|_{\rm GM} = \frac{1}{1-1/{\rm GM}}. \qquad (7)$$

The distance between the loop gain $L(j\omega)$ and the point $(-1,\ 0)$ can be always given as $-1-L(j\omega)$ according to Fig. 3. By denoting $|S_{\max}| = M_S$ and $L(j\omega) = \alpha + j\beta$, then $(1+\alpha)^2 + \beta^2 = 1/M_S^2$ forms a circle in the complex plane having the center at $(-1,\ 0)$ and the radius of $1/M_S$. This circle defines the forbidden region used in [6]–[8] for the minor-loop gain, out of which it shall stay for robust stability to exist. This criterion takes also into account the combined effects of both of the margins in (7) regardless of the frequency of occurrence. It is clear that the selection of the allowed peaking determines the area of the forbidden region. In Fig. 4, the MPC-based forbidden region (gray area), where $M_S = 2$ corresponding to PM $\approx 29.0^\circ$ and GM $= 6$ dB, is compared to the regions defined in [1]–[5] (see Fig. 1). For robust stability to exist, the minor-loop gain shall stay out of the defined MPC-based forbidden region and also satisfy the Nyquist stability criterion. The state of stability extractable from the behavior of the minor-loop gain is invariant to the interface at which the minor-loop gain is determined as discussed, e.g., in [3]. The state of the robustness of stability depends, however, on the interface at which the minor-loop gain is determined because of the hiding effects of the passive components such as capacitors and *LC* filters between the direct interface of the converter power stage and the applied interface. As a consequence, the robustness can be reliably determined only at the direct interface of a regulated converter as in assessing the effect of the input filter in [1] and [2]. The stability discussions in most of the referenced papers in this letter are related to the input-filter-related stability and performance issues. Evidence supporting the previous discussions is given in Section IV.

IV. Experimental Evidence

Fig. 5 shows a typical minor-loop gain measured at the interface between a switched-mode converter and its input filter,

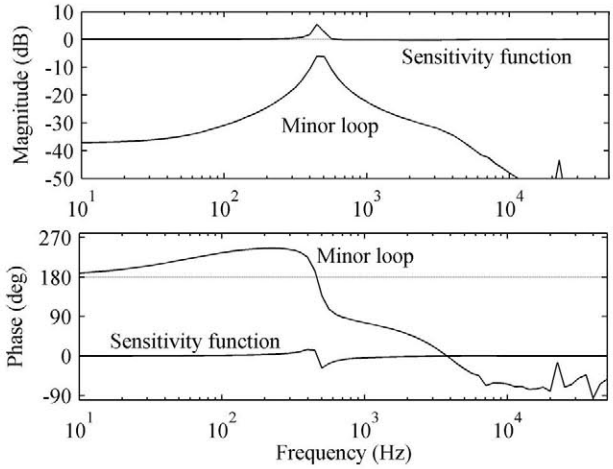


Fig. 5. Typical behavior of the minor-loop gain in the input-filter application with corresponding sensitivity function based on measurements from an authentic buck converter.

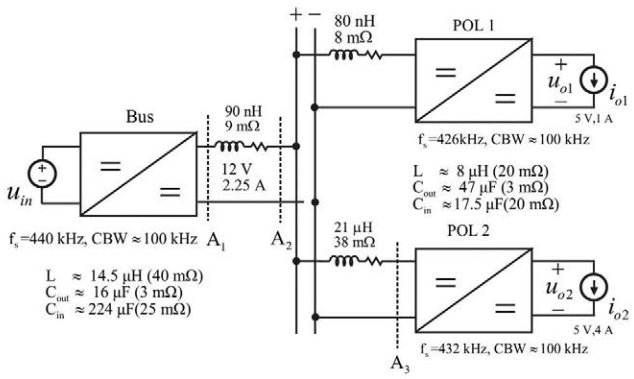


Fig. 6. Example distributed dc/dc system.

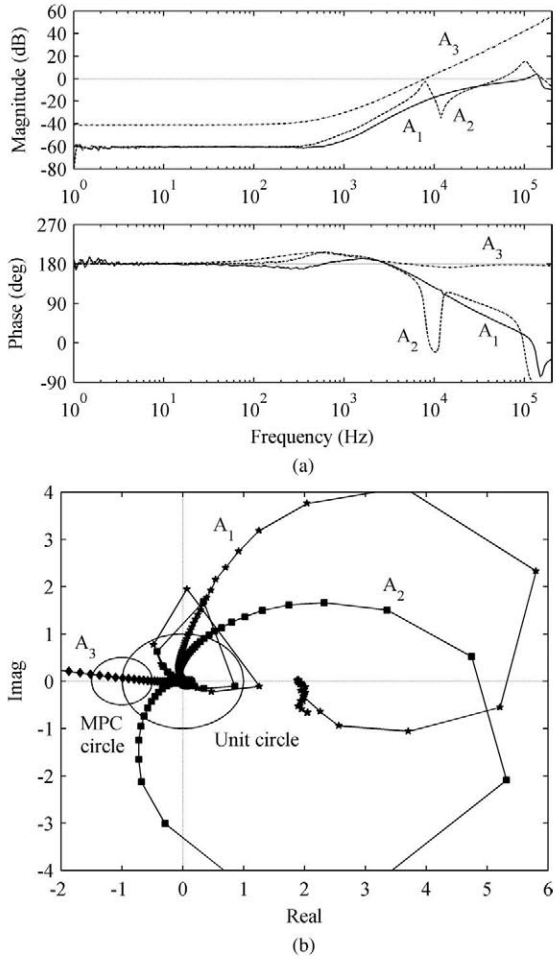


Fig. 7. Measured minor-loop gains at different interfaces within the system of Fig. 6 as (a) bode plot (A_1 : solid line, A_2 : dashed line, and A_3 : dash-dotted line) and (b) polar plot (A_1 : star, A_2 : square, and A_3 : diamond).

where GM is 6 dB and the corresponding peaking of the sensitivity function 6 dB. The input filter and the associated buck converter are specified in more detail in [16]. In order to obtain high enough attenuation, the resonant frequency of the filter has to be selected to be much less than the crossover frequency of the output-voltage loop. As a consequence, in order to assure stability, the input filter has to be designed so that its output-impedance peak does not intersect with the closed-loop input impedance of the converter. In addition, to avoid affecting the output impedance of the converter, the GM of the minor-loop gain has to be large enough. Therefore, the allowed complex-plane region is inside the circle having the center at the origin and the radius of inverse of GM as Middlebrook's design rules dictate [1], [2]. It is obvious that the design rules are, in general, too restrictive but quite proper for input-filter design as Fig. 5 depicts.

An experimental distributed dc/dc system composing of one bus converter and two point-of-load (POL) converters is shown in Fig. 6. The converters are nonisolated synchronous buck converters having switching frequencies of 400 kHz. The input terminals of the converters are provided with an input capacitor preventing accurate measurement of their internal input impedances because of the dominating effect of the input capacitor especially at the higher frequencies. The approximate power-stage-component values, the actual switching frequencies f_s, and the control bandwidths of the voltage-loop gains are also given in Fig. 6.

From the presented system, three different minor-loop gains were measured at the interfaces A_1, A_2, and A_3 as defined in Fig. 6. These measured minor-loop gains are shown in Fig. 7(a) as bode plots and in Fig. 7(b) as polar plots, where the unit circle and MPC circle corresponding to 6-dB peaking are given, respectively. These plots indicate that the system is stable. Even though the PM and GM of the minor-loop gains at A_1 and A_2 are high, implying robust stability, the behavior of the minor-loop gain at the interface A_3 implies that the margins are low in reality.

An extended view of the minor-loop gain at A_3 as Nyquist plot in the original loading condition (solid line) of the POL converters (see Fig. 6) and by interchanging the output currents of the converters (dashed line) are given in Fig. 8. The Nyquist plots confirm the state of the stability but also show that the violation of the ESAC criterion [3] does not lead to instability. The violation of the MPC criterion is also obvious.

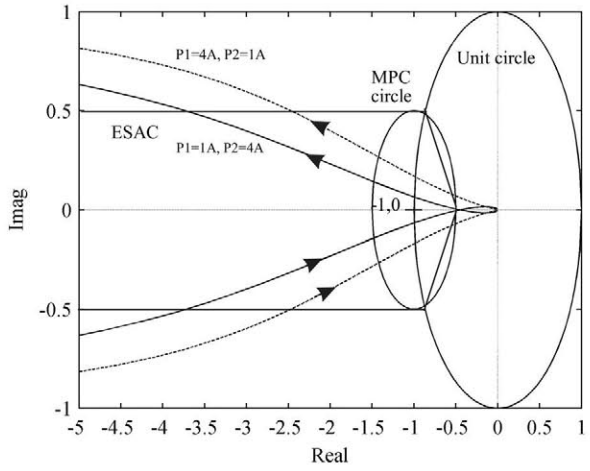


Fig. 8. Measurement-based Nyquist plots of the minor-loop gain measured at interface A_3 with varying output power of POL2 converter (solid line: $I_{\rm out}$ = 4 A, dashed line: $I_{\rm out}$ = 1 A).

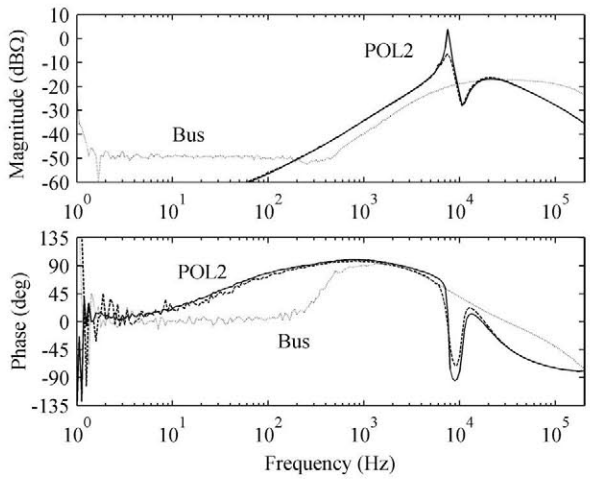
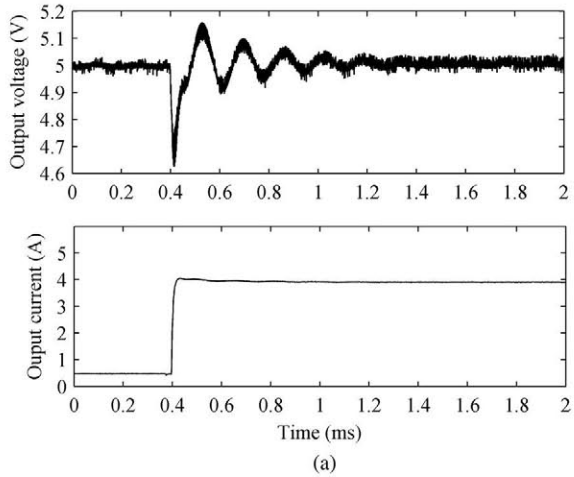


Fig. 9. Measured output impedances of the POL2 (solid line: $I_{\rm out}$ = 4 A, dashed line $I_{\rm out}$ = 1 A) and bus (dotted line) converters.

Based on the minimum distance between the measured minor-loop gain and the point $(-1, 0)$, the amount of peaking of the sensitivity function can be computed to be 23.7 dB, corresponding to PM of 4° and GM of 0.6 dB in the original loading condition. The interchange of the output currents clearly increases the minimum distance defined previously. Fig. 9 shows the measured output impedances of the POL2 converter in both of the loading conditions, where the solid line denotes the original condition and the dashed line the interchanged condition. The peaking of the output impedance in the original condition is approximately 24 dB, which complies with the information given by the minor-loop gain in Fig. 8. The peaking of the output impedance in the interchanged condition is reduced by 10 dB, which corresponds to the information given by the corresponding minor-loop gain in Fig. 8.

Fig. 10 shows the time-domain output-voltage responses of the POL2 and bus converters when a load-current step is applied at the output of the POL2 converter. The decaying oscillatory response of the POL2 converter [see Fig. 10(a)] is caused by the



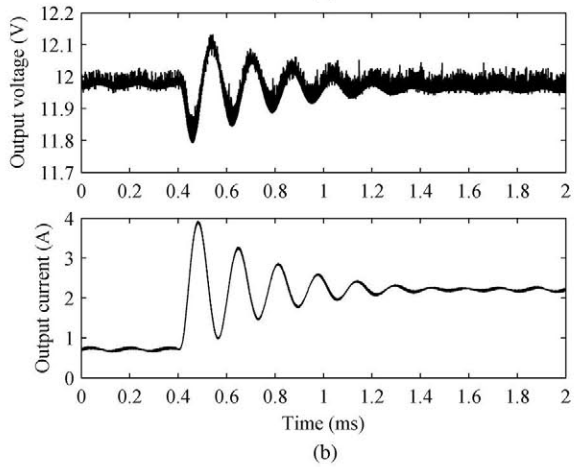


Fig. 10. Measured time-domain behavior of (a) POL2 and (b) bus converters when a step change in load current from 0.5 to 4 A (250 mA/μs) is applied at the output of the POL2 converter.

resonance in its source-affected output impedance, which lies within the bandwidth (100 kHz) of its voltage-loop gain. Therefore, the transient response is not determined by the control system but by the resonant behavior in the output impedance. Fig. 9 shows that the output impedance (dotted line) of the bus converter is well behaving. Therefore, the decaying oscillatory response at the output of the bus converter is caused by the behavior of the input current of the POL2 converter [see Fig. 10(b)] due to its rather high output impedance (≈100 mΩ) at the frequency of the oscillation (see Fig. 9; ≈6 kHz).

The experimental measurements show clearly that the interface, at which the minor-loop gain is measured, affects the validity of the robustness information. The interface closest to the power-stage direct input or output gives only reliable information on the state of the robustness of stability.

V. Conclusion

The stability assessment based on the impedance ratio known as minor-loop gain was addressed in this letter. It was shown that the previously defined forbidden regions are all developed not only to ensure stability but also to maintain the changes in the transient performance acceptable. It was shown that the

robustness of stability (i.e., adequate PM and GM) is mostly determined by the area around the point $(-1, 0)$. As a consequence, the area occupied by these forbidden regions in the complex plane is unnecessary large. This letter shows that the criterion based on the allowed peaking in the associated sensitivity function yielding a circle having the center at the point $(-1, 0)$ and the radius of inverse of the allowed maximum peaking value is sufficient to guarantee robust stability. This forbidden region automatically determines the minimum values for the PM and GM without any need for considering their relations to frequency. Moreover, it was also stated that the well-behaving minor-loop gain alone does not necessarily ensure robust transient performance. This letter shows also explicitly that an arbitrarily measured minor-loop gain within a system does not necessarily contain such information according to which the robustness of stability and the state of transient performance can be determined. In addition, the experiments clearly show that the minor-loop gain should be measured at the interface, which is closest to the internal terminals of the converter for maximizing the value of the measured information. The used value of the peaking in this letter is just an example and it can be freely chosen according to the specifications or needs in the specific system designs.

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