Impedance Circuit Model of Grid-Forming Inverter: Visualizing Control Algorithms as Circuit Elements

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***Abstract*—The impedance model is widely used for analyzing power converters. However, the output impedance is an external representation of a converter system, i.e., it compresses the entire dynamics into a single transfer function with internal details of the interaction between states hidden. As a result, there are no programmatic routines to link each control parameter to the system dynamic modes and to show the interactions among them, which makes the designers rely on their experience and heuristic to interpret the impedance model and its implications. To overcome these obstacles, this paper proposes a new modeling tool named as *impedance circuit model*, visualizing the closed-loop power converter as an impedance circuit with discrete circuit elements rather than an all-in-one impedance transfer function. It can reveal the virtual impedance essence of all control parameters at different impedance locations and/or within different frequency bandwidths, and show their interactions and coupling effects. A grid-forming voltage-source inverter (VSI) is investigated as an example, with considering its voltage controller, current controller, control delay, voltage/current dq-frame cross-decoupling terms, output-voltage/current feedforward control, droop controllers, and three typical virtual impedances. The proposed modeling tool is validated by frequency-domain spectrum measurement and time-domain step response in simulations and experiments.**

***Index Terms*—Output Impedance Shaping, Impedance Circuit Model, Virtual Impedance, Grid-Forming Inverter, Voltage-Source Inverter, Power System Stability.**

I. Introduction

Voltage source inverters (VSIs) are increasing in penetration in the world's major power systems due to the rapid growth of renewable resources on the pathway towards decarbonization [1], [2]. Such a trend gives rise to a structural change as VSIs are starting to take over the dominant role from synchronous generators, which introduces new dynamic behaviour and thereby poses new challenges to power system stability [3], [4]. A framework for modeling and analyzing VSIs in the context of power networks is needed to address this emerging problem.

There are two tools widely used for power system dynamic modeling: (a) state-space method, (b) impedance-based method, each has its advantages and disadvantages. The state-space model preserves a detailed representation of each single state in the model and allows for an insight into the root caused of under-damped or unstable modes via participation and sensitivity analysis [5]–[8]. However, it needs a full knowledge of the hardware and control design of the VSI, which is often very difficult to obtain and validate. Besides, the state-space model takes a very abstract form and is hard to be visualized and interpreted intuitively as required by practical engineers. The impedance-based (or equivalently admittance-based) model, on the other hand, can be directly measured, validated and visualized without a full knowledge of the design details, but lack a systematic insight into the internal root causes of under-damped or unstable modes [9]–[12].

Due to these different characteristics, state-space models and impedance-based models are used complementarily for different conditions. The state-space method is usually used to analyze low-frequency oscillation (e.g. angle swing) in a complex system, where precise models can be readily obtained (since a VSI's behaviour is relatively fixed in the low frequency but can be rather diversified in the high frequency). The impedance-based method is usually used to analyze high-frequency local oscillation (e.g. harmonic oscillation), where the system dynamics is largely reflected by impedance alone [13]–[16]. However, such division may no longer hold with the increasing penetration of VSI's in the grid, as mid-frequency oscillation (e.g. synchronous control interaction) may be induced across a larger range.

To solve this problem, there has been efforts to bridge the gap between the two modelling approaches. Theoretically, the linkage between an impedance-model and state-space model can be established by system identification [17], [18]. In practice, the system identification can be greatly facilitated by the prior knowledge of the model. These considerations lead to the idea of a gray-box model, where the structure of the state-space model is considered known, whereas the parameters are identified from the impedance either measured or disclosed by manufacturers [19]. However, such a gray-box model still needs to be converted to either state-space or impedance (transfer function) format in stability analysis, which means that the model is only gray in the set-up phase, but becomes white or black in the analysis phase.

In this paper, we present a novel gray-box model named *impedance circuit model*. This model expands the conventional impedance model (represented as an all-in-one transfer function or spectrum) into a series of interconnected circuit elements. These elements can be mapped to either physical components or control loops in the VSI. As a result, the abstract control algorithms are visualized as circuit elements, and the role of each control loop can be directly interpreted from the value, the position, and the interconnection of corresponding circuit elements. Such mapping and visualization are generally applicable to inner, outer, feedback and feed-forward control loops, so the impedance circuit model provides a very general yet intuitive modeling framework.

The impedance circuit model is "gray" in its inherent

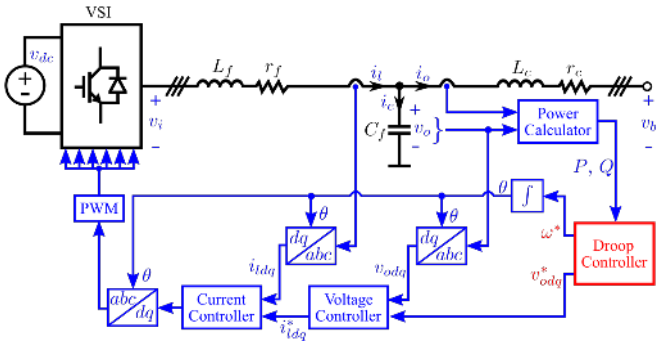


Fig. 1. Droop-controlled grid-forming VSI.

formulation, and serves as a bridge between the white-box and black-box approaches. It preserves part of the internal details of a white-box model in terms of the interconnection structure of the circuit elements, but can be directly interfaced to a black-box model of an unknown system (e.g. a grid with measured impedance but no detailed model).

As an example, the impedance circuit model is applied to grid-forming VSIs. Such a choice is based on the consideration that grid-following VSIs are relatively well-understood whereas grid-forming VSIs are not, especially for impedance modeling. Moreover, grid-forming VSIs often appear in weak or stand-alone grids with no stiff sources to anchor the voltage and frequency [2], [20], so their interaction with loads and other converters/generators is more complicated.

The paper is organized as follows: Section II firstly reviews the modeling, control, and a simplified controller design procedure of grid-forming VSIs. The results are displayed in both transfer matrix form and complex vector form. The impedance circuit model concept is proposed in Section III, with a detailed analysis of each control parameter and its virtual impedance essence. Finally, in Section IV, the proposed model is discussed, and validated by simulations and experiments in frequency-domain spectrum measurement and time-domain step response. The final section summarizes the findings and concludes the paper.

II. Fundamentals of Control

A. Reference Frames

The VSI in Fig. 1 is investigated in this paper with corresponding reference directions of variables. The synchronous dq frame is widely used, which converts the ac time-variant steady-state operating points of a three-phase-balanced system into dc time-invariant steady-state operating points [1], [5], [9], and facilitates the controller design.

The dq frame can be further classified into two forms [12], [21]–[23]: (a) transfer matrix form; and (b) complex vector form. Fig. 2 shows the relationship between these two frames in Laplace s domain. (F1) is a typical dq-frame system. Its transfer function G^m_{dq} has four elements: G_{dd} and G_{qq} are the self transfer functions at d and q axes, respectively; G_{dq} and G_{qd} are the mutual transfer functions (i.e., the coupling effect) between two axes. By using (F8), the transfer matrix form (F1) can be transformed into the complex vector form (F3) [11], [12], [21]. In the complex vector form, the input and output signals are complex vectors, e.g., input $u_{dq+} = u_d + ju_q$ is the forward component and $u_{dq-} = u_d - ju_q$ is the backward component, and they are conjugate. It is worth mentioning that the complex-vector model in this paper is distinguished from the sequence-domain model in [24]. In other words, the forward and backward space vectors are not positive and negative-sequence signals. Instead, the positive and negative frequencies $\pm\omega$ represent the positive- and negative-sequence signals at frequency ω for a complex vector, e.g., $u_{dq+}(+j\omega)$ and $u_{dq+}(-j\omega)$ represent the positive and negative-sequence signals of $u_{dq+}(s)$ at a given frequency point $\omega > 0$, as discussed in [11], [21]. In the complex vector form, the transfer function $G^m_{dq\pm}$ is also a matrix, but consisting of only two independent complex elements G_{dq+} and G_{dq-}. Notably, if symmetric condition (F7) is valid, i.e., two diagonal elements of G^m_{dq} in (F4) are same and two anti-diagonal elements are the negative of each other, in this case, the complex vector form is equivalent to a single-input-single-output (SISO) system because of the equivalence of forward and backward equations in (F6). This considerably simplifies the system analysis.

B. Converter Circuit Modeling

The result of the derivation of the dq frame converter model, as explained in [25], [26], is shown in Fig. 3. Fig. 3(a) and (b) correspond to transfer matrix form and complex vector form, respectively. They are related through transformation (F2) in Fig. 2. Notably, only the forward complex component is shown in Fig. 3(b) due to the system symmetry [i.e., (F7) in Fig. 2 is valid].

C. Control Structure

Fig. 1 shows a widely-used dq-frame control structure of a grid-forming VSI. The droop controller (red block) is applied to generate the frequency and the voltage references ω^* and v^*_{odq}, which achieves the grid synchronization by the power-angle swing when the converter is connected to power grids consisting of stiff voltage sources [5], [27]. Alternatively, in certain stand-alone grids without stiff voltage sources, the droop controller can be removed, and ω^* and v^*_{odq} can be set to required constant values. The droop controller will be discussed in details in Sections III-G to III-I later due to its asymmetry. The inner voltage and current loops (as shown in Fig. 4 in details) are discussed first. It is a general structure, and features multiple loops that have been suggested in literature, noting that some of them may be disabled depending on the applications as discussed next. Fig. 4(a) and (b) correspond to transfer matrix form and complex vector form, respectively. Only the forward component is shown in Fig. 4(b) because the symmetric condition [(F7) in Fig. 2] is still valid for Fig. 4(a). The complex vector form gives a very concise representation and therefore used in later analysis. This control structure is briefly introduced next: i_{ldq} and v_{odq} are the control targets of current and voltage loops, respectively. G_{del} is the control delay, which equals to $e^{-1.5T_s}$ approximately [8]. The output voltage v_{odq} can be fed to v^*_{idq} and the output current i_{odq} can

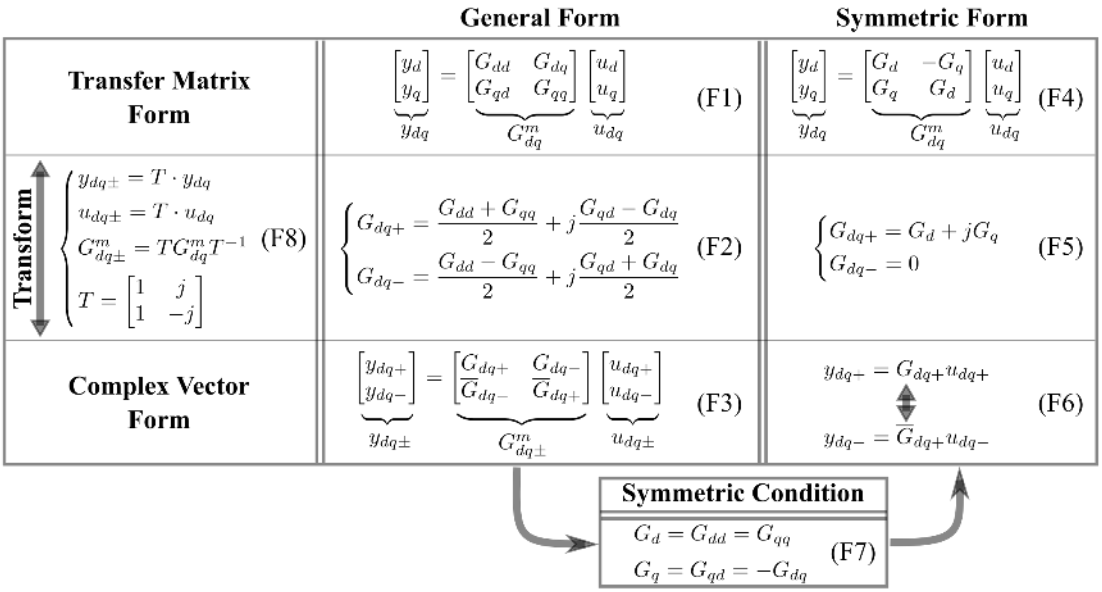


Fig. 2. Relationship of dq-frame transfer functions in transfer matrix frame and complex vector frame. [Remarks: For the sake of brevity, "(s)" is omitted for all transfer functions or impedances in this paper, e.g., G_{dd} in (F1) actually represents $G_{dd}(s)$; Overbar donates the conjugate operation.]

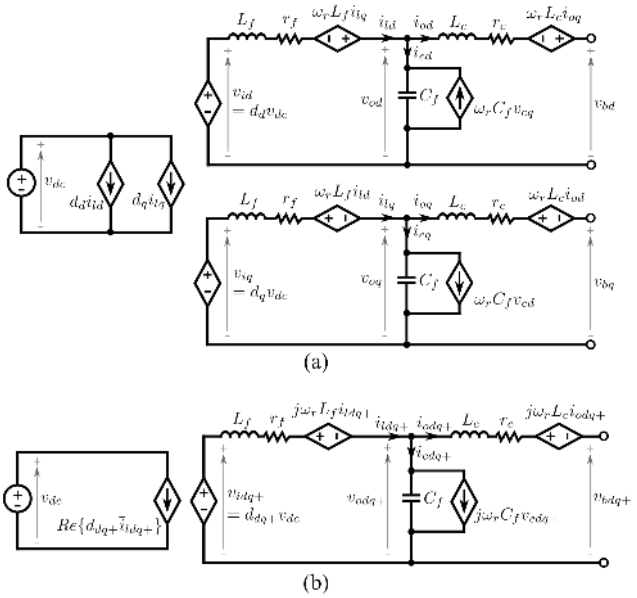


Fig. 3. VSI circuit model in dq frame. (a) Transfer matrix form. (b) Complex vector form.

be fed to i^*_{ldq}, with feedforward gains F_v and F_i, respectively. Three locations are available for adding virtual impedance, as shown in Fig. 4 and Fig. 5. The detailed analysis of this control structure is shown next.

III. Impedance Circuit Model

The impedance circuit model concept is proposed in this section. The parameters in Table II (shown in Section IV later) are used when plotting bode diagrams in this section.

A. Methodology: The Equivalence of Controlled Source and Virtual Impedance

A grid-forming VSI is essentially a controlled voltage source, which reflects the impedance shaping effects of control loops. Hence, we first give a brief discussion, to reveal the virtual impedance essence of a controlled source. As shown in Fig. 6(a) and (b), according to Ohm's law [28], a self-current-controlled voltage source is equivalent to a few virtual impedances in series; and a self-voltage-controlled current source is equivalent to a few virtual impedances in parallel. They are two fundamental cases. Furthermore, Fig. 7 illustrates a more general example: a step-by-step procedure of converting an external-voltage-controlled voltage source to one of these two fundamental cases, by using Thevenin's theorem, Norton's theorem, Ohm's law, superposition theorem, and block diagram algebra [28]. Notably, it is also equivalent to a virtual impedance aligned to its feedback signal v. As derived next, all control loops of the grid-forming VSI could be equivalent to virtual impedances at different impedance locations depending on the feedback signals: (a) in series with L_f with feeding back i_l; (b) in parallel with C_f with feeding back v_o; and (c) in series with L_c with feeding back i_o. (The derived impedance circuit model will be summarized in Fig. 16 and Fig. 17 later.)

B. Current Controller versus Inner Virtual Impedance

As shown in the control structure in Fig. 4(b), the inner virtual impedance is implemented by using the following equation

$$v_{idq+} = [v^*_{idq+} - (R_{iv} + jX_{iv})i_{ldq+}] \times G_{del} \qquad (1)$$

i.e., a virtual impedance $Z_{iv} = (R_{iv} + jX_{iv})G_{del}$ is added in series with L_f, as shown in Fig. 5. $G_{del} \approx 1$ when $f << 1/T_s$, e.g., $f < T_s/5$. Z_{iv} is usually resistive, for damping the LCL

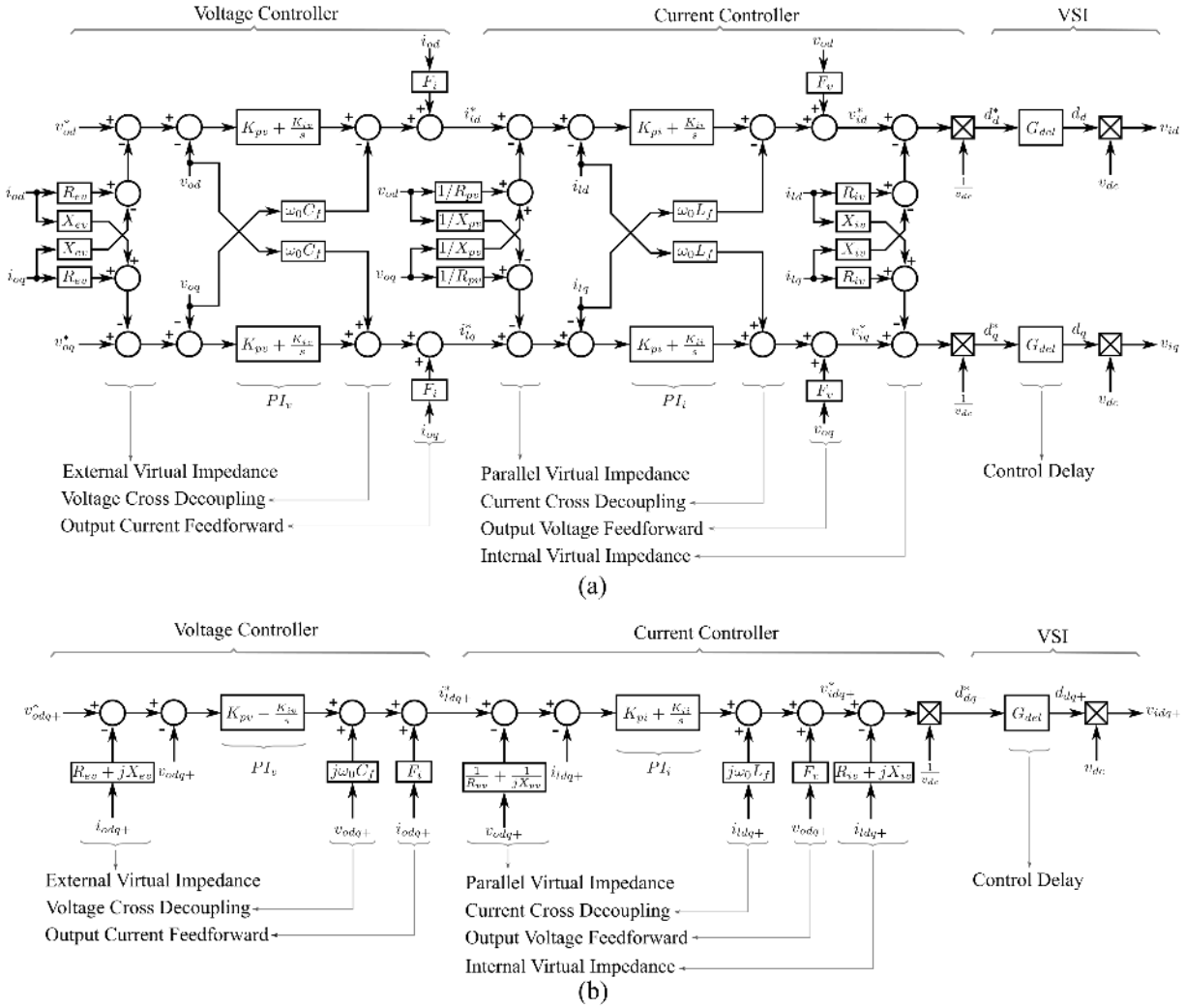


Fig. 4. Control structure in dq frame. (a) Transfer matrix form. (b) Complex vector form.

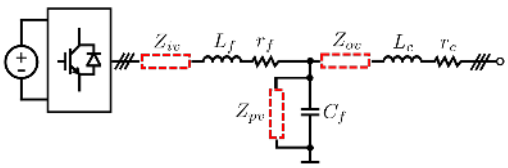


Fig. 5. Equivalent circuit of three virtual impedance locations.

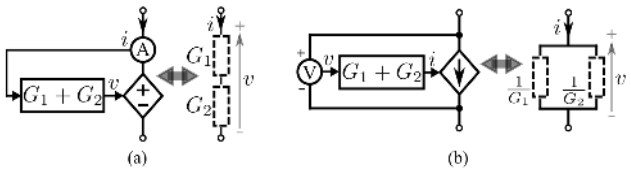


Fig. 6. The equivalence between controlled source and virtual impedance - two fundamental cases: (a) Self-current-controlled voltage source. (b) Self-voltage-controlled current source.

filter resonance [15], [29]. It will be shown next that, the current controller is also equivalent to adding inner virtual impedance in series with L_f.

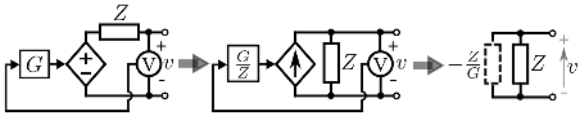


Fig. 7. A general example: an external-voltage-controlled voltage source and its equivalent virtual impedance.

According to the control structure in Fig. 4 and average model in Fig. 3, the current-loop impedance circuit model can be derived, as illustrated in Fig. 8, which represents the current-controlled VSI as a Norton equivalent circuit, i.e., a current source $i^*_{ldq+}G_I$ with an source impedance[1] $Z_{Norton} = Z_{inner}//Z_{Fv}$. The output current i_{ldq+} can be represented by

$$i_{ldq+} = i^*_{ldq+}G_I - v_{odq+}/\underbrace{(Z_{inner}//Z_{Fv})}_{Z_{Norton}} \tag{2}$$

i^*_{ldq+} is the current reference. G_I is the closed-current-loop

[1]We use "//" to represent the parallel connection of impedances in this paper.

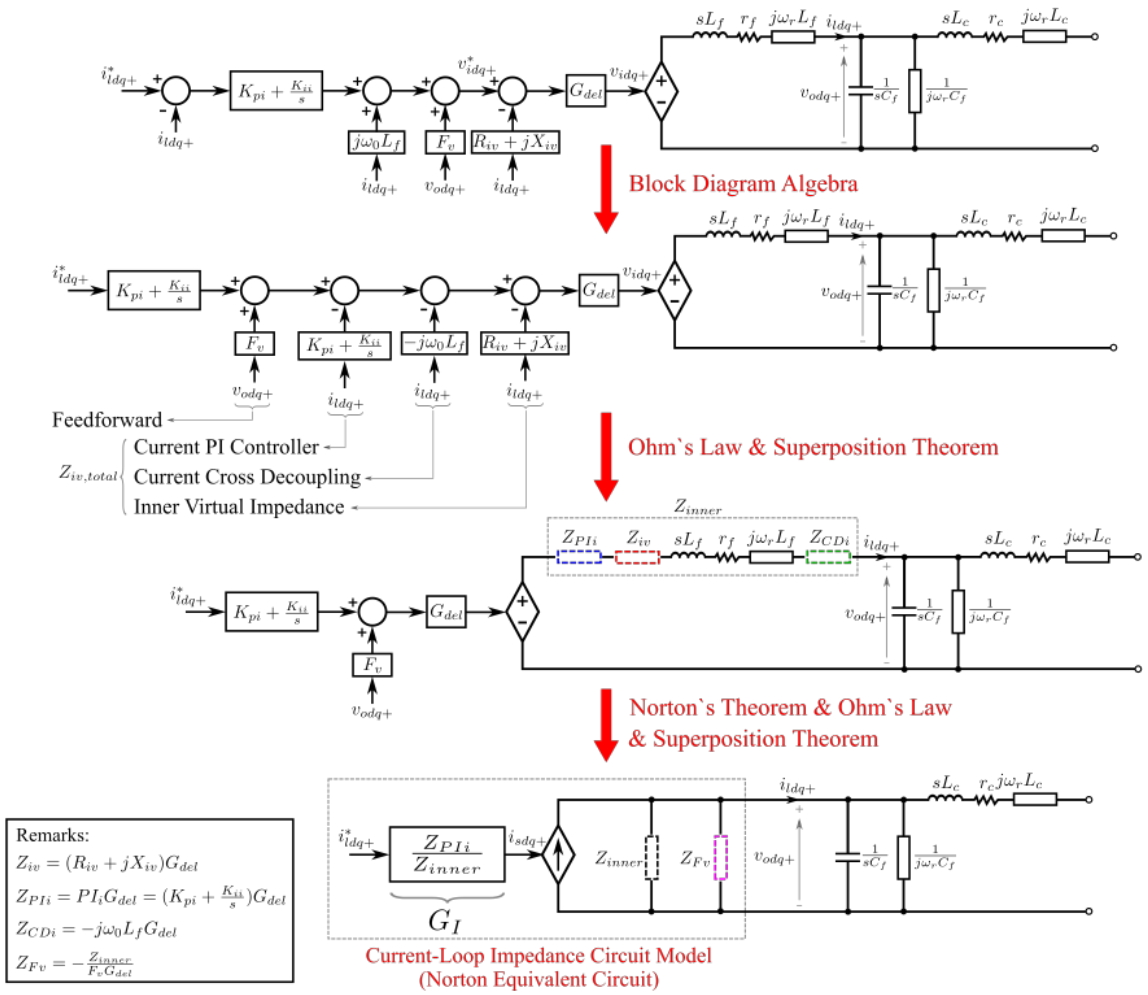


Fig. 8. Derivation of current-loop impedance circuit model. (Remarks: current PI controller - Z_{PIi}; current cross-decoupling - Z_{CDi}; inner virtual impedance - Z_{iv}; output voltage feedforward - Z_{Fv}.)

gain, with considering the control delay and cross decoupling, i.e., no approximations. v_{odq+} introduces the grid influence (grid disturbance) to the current control loop through the source impedance Z_{Norton}. Z_{Fv} is the virtual impedance given by output-voltage feedforward, which will be discussed later in Section III-D and is temporarily ignored here; Z_{inner} includes the filtering inductor L_f only in open-loop but is shaped by the current controller in closed-loop, as discussed next.

Current cross decoupling - Z_{CDi}: In Fig. 3(b), the dq-frame coupling of L_f is represented by a voltage source $j\omega_r L_f i_{ldq+}$, which is also equivalent to an impedance $j\omega_r L_f$ in Fig. 8. As for the cross decoupling, it is equivalent to a negative virtual inductor $Z_{CDi} = -j\omega_0 L_f G_{del}$ in series with $j\omega_r L_f$, and therefore can compensate the coupling impedance if $\omega_r = \omega_0$ and $G_{del} \approx 1$.

Current PI controller - Z_{PIi}: As displayed in Fig. 8, the PI controller introduces a virtual impedance $Z_{PIi} = PI_i G_{del} = (K_{pi} + K_{ii}/s)G_{del}$ in series with L_f, i.e., a virtual resistor K_{pi} given by the proportional part and a virtual capacitor K_{ii}/s given by the integral part. Fig. 9 shows the Bode diagrams of the closed-loop gain G_{Icl} and Norton source impedance Z_{Icl} with different controller settings. Notably, compared with the inner virtual resistance R_{iv}, K_{pi} holds an exactly same impedance shaping effect, i.e., shaping the low-frequency impedance to resistive and damping the $L_f C_f$ resonance. But K_{pi} also increases the loop gain G_I for speeding up the system dynamics and reducing the steady-state error. Adding K_{ii} shapes Z_{Icl} to be capacitive at low-frequency range, which means infinite current source impedance at dc (i.e., no steady-state error in the closed-loop gain). It is worth mentioning that Z_{PIi} is also influenced by $G_{del} = e^{-1.5T_s}$ (i.e., a phase shift). This means $K_{pi}G_{del}$ would become a negative virtual resistor (i.e., negative damping) with the increase of frequency and control delay. Hence, the ratio of $K_{pi}/(sL_f)$ must be limited, specially at high frequency range. This can be ensured by selecting $K_{pi} = w_i L_f$ with $w_i \ll 1/(1.5T_s)$. Notably, w_i is also the bandwidth index of inner current loop according to the conventional design criterion [15], [29], [30], which implies the coincidence between the proposed impedance model with conventional design tool.

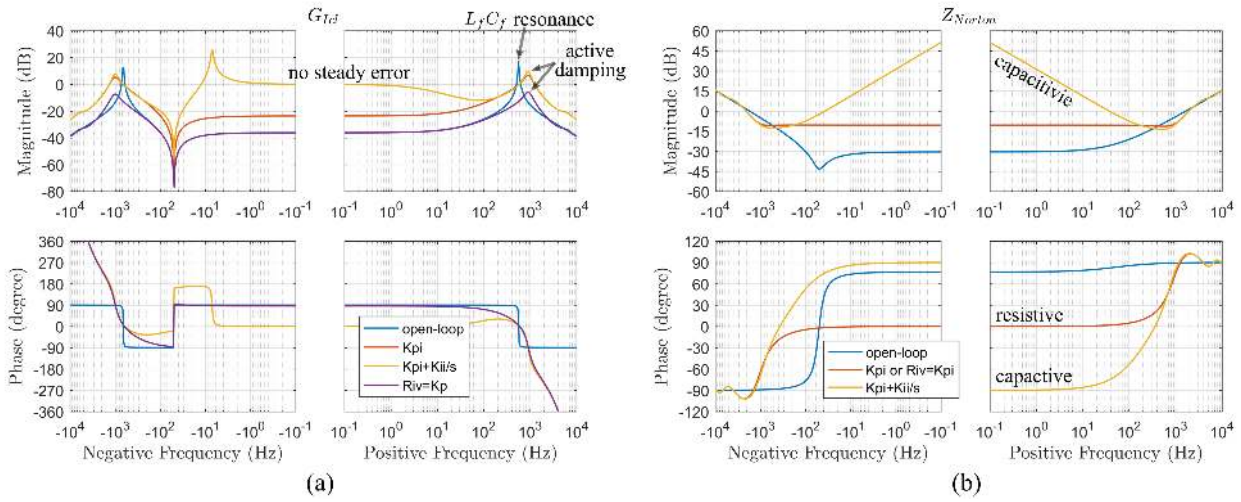


Fig. 9. Bode diagram for analyzing current loop. (a) Closed-loop gain $G_{Icl} = i_{ldq+}/i^*_{ldq+}$. (b) Norton source impedance Z_{Norton}, which equals to Z_{inner} if ignoring Z_{Fv}.

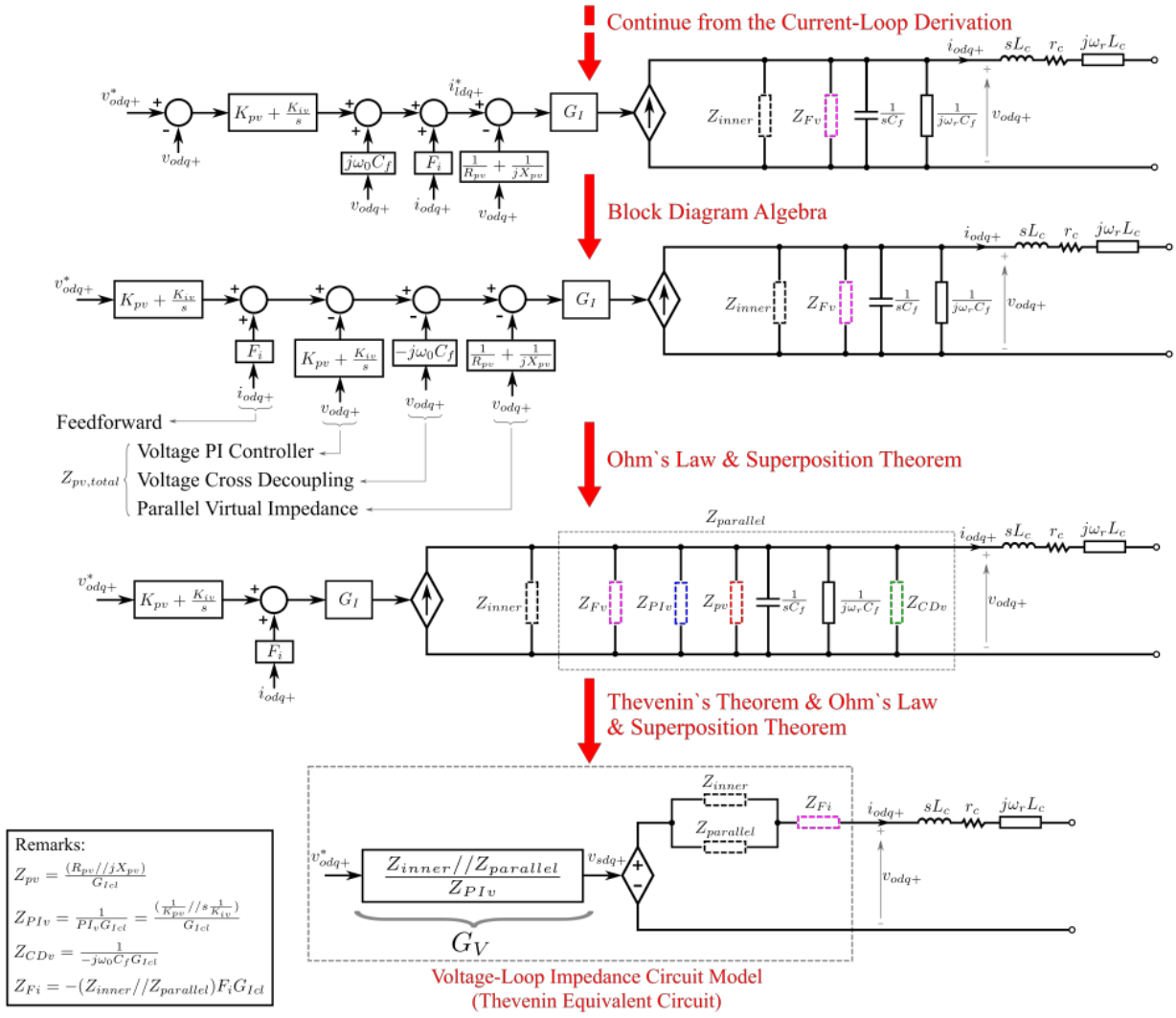


Fig. 10. Derivation of voltage-loop impedance circuit model. (Remarks: voltage PI controller - Z_{PIv}; voltage cross-decoupling - Z_{CDv}; parallel virtual impedance - Z_{pv}; output current feedforward - Z_{Fi}.)

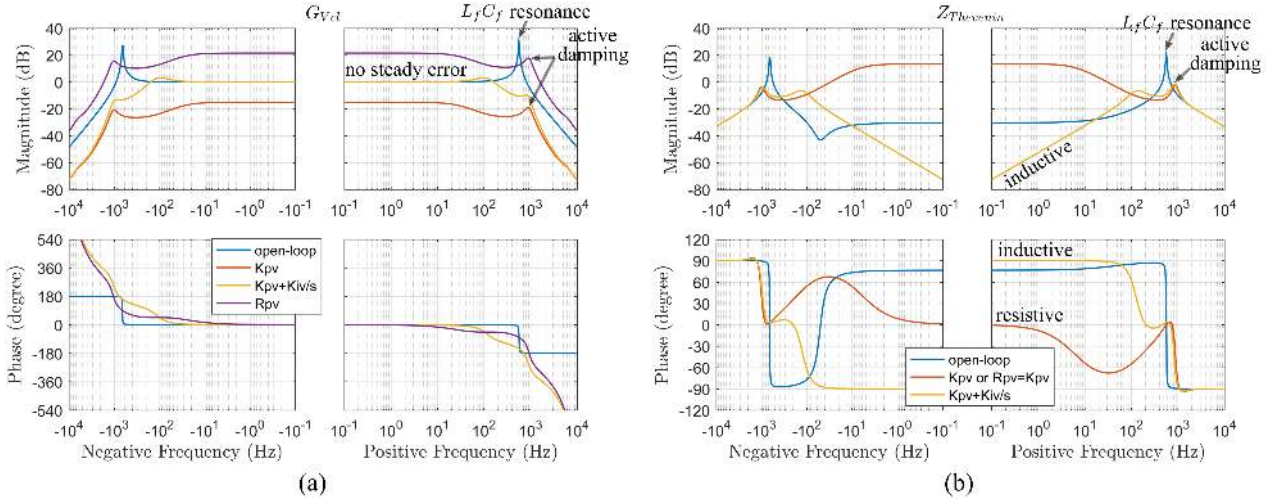


Fig. 11. Bode diagram for analyzing voltage loop. (a) Closed-loop gain $G_{Vcl} = v_{odq+}/v^*_{odq+}$. (b) Thevenin source impedance $Z_{Thevenin}$, which equals to $Z_{inner}//Z_{parallel}$ if ignoring Z_{Fi}.

C. Voltage Controller versus Parallel Virtual Impedance

As shown in the control structure in Fig. 4(b), the parallel virtual impedance is implemented by

$$i_{idq+} = [i^*_{ldq+} - v_{odq+}(\frac{1}{R_{pv}} + \frac{1}{jX_{pv}})] \times G_I \qquad (3)$$

A virtual impedance $Z_{pv} = (R_{pv}//jX_{pv})/G_I$ (i.e., admittance $Y_{pv} = (G_{pv} + jB_{pv})G_I$) is added in parallel with C_f, as shown in Fig. 5. G_I is the current-loop gain in Fig. 8. Within the bandwidth of the current loop, $G_I \approx 1$. Z_{pv} is usually resistive in conventional cases for damping the LCL filter resonance [29]. It will be shown next that, the voltage controller is also equivalent to adding parallel virtual impedances in parallel with C_f.

As shown in Fig. 10, the voltage controller can also be rearranged into an impedance circuit model, which represents the voltage-controlled VSI as a Thevenin equivalent circuit, i.e., a voltage source $v^*_{odq}G_V$ with a source impedance $Z_{Thevenin} = Z_{inner}//Z_{parallel} + Z_{Fi}$. The source output voltage v_{odq+} can be represented by

$$v_{odq+} = v^*_{odq+}G_V - i_{odq+}\underbrace{(Z_{inner}//Z_{parallel} + Z_{Fi})}_{Z_{Thevenin}} \qquad (4)$$

v^*_{odq+} is the voltage reference. G_V is the voltage-loop gain with considering the inner current-loop delay and the voltage cross-decoupling, i.e., no approximations. i_{odq+} introduces the grid influence (grid disturbance) to the voltage loop through the source impedance $Z_{Thevenin}$. Z_{Fi} is the virtual impedance effect of output-current feedforward, which will be discussed later in Section III-D and is temporarily ignored here. Z_{inner} shows the inner-current-loop impedance shaping effect. $Z_{parallel}$ includes C_f in open-loop but is shaped by the voltage controller in closed-loop, as discussed next.

Voltage cross decoupling - Z_{CDv}: As displayed in the average model in Fig. 3(b), the cross coupling of C_f in complex dq frame is represented by a current source $j\omega_r C_f v_{odq+}$, which is also equivalent to an virtual capacitor $\frac{1}{j\omega_r C_f}$. By contrast, the voltage cross-decoupling term is equivalent to a negative virtual capacitor, i.e., $Z_{CDv} = \frac{1}{-j\omega_0 C_f G_I}$ in Fig. 10, and hence, can compensate the coupling effect if $\omega_0 \approx \omega_r$ and $G_I \approx 1$.

Voltage PI controller - Z_{PIv}: As displayed in Fig. 10, the voltage PI controller introduces a virtual impedance $Z_{PIv} = 1/(PI_vG_I) = (\frac{1}{K_{pv}}//\frac{s}{K_{iv}})/G_I$ in parallel with C_f, i.e., a virtual resistor $1/K_{pv}$ given by the proportional controller and a virtual inductor s/K_{iv} given by the integral controller. The Bode diagrams with different controller settings are shown in Fig. 11. Notably, K_{pv} illustrates same impedance shaping effect as the parallel virtual resistor R_{pv}, except that their effects on loop gain G_V are different. Adding K_{iv} can shape the Thevenin voltage source impedance Z_{Vcl} to inductive at low-frequency, which implies the zero impedance at dc and coincides with the zero steady-state error. It is also worth mentioning that Z_{PIv} is proportional to $1/G_I$, i.e., limited by the bandwidth of inner-current-loop.

D. Output Feedforward

In this subsection, it will be shown that both output-current and -voltage feedforward can also be equivalent to virtual impedances.

1) Output-voltage feedforward - Z_{Fv}: As derived in the current-loop impedance circuit model in Fig. 8, the output-voltage feedforward is equivalent to adding a virtual impedance Z_{Fv} in parallel with the source impedance Z_{inner} and the filtering capacitor C_f, with

$$Z_{Fv} = -\frac{Z_{inner}}{F_v G_{del}} \qquad (5)$$

With considering Z_{Fv}, the inner impedance of the Norton current source is $Z_{Norton} = Z_{inner}//Z_{Fv}$. When the feedforward gain is zero ($F_v = 0$), $Z_{Fv} \to \infty$ and $Z_{Norton} \to Z_{inner}$, so that Z_{Fv} can be ignored. By contrast, when the feedforward gain is unity ($F_v = 1$) and if the delay is ignored ($G_{del} \approx 1$), we get $Z_{Fv} \approx -Z_{inner}$ and $Z_{Norton} \to \infty$. In this case,

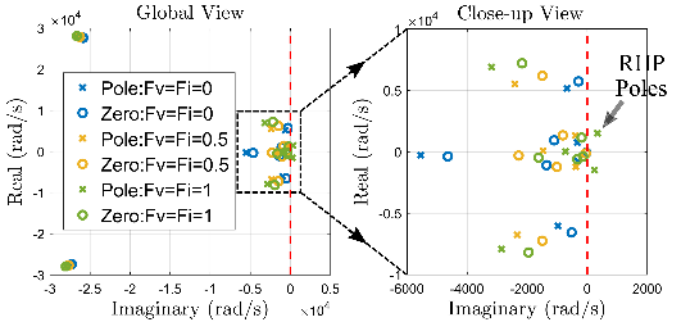


Fig. 12. Pole/zero map of the VSI output impedance with different feedforward gains.

the feedforward leads to an zero admittance for the Norton source not only at steady state but also during system transients [(2) can be rewritten as $i_{ldq+} = i^*_{ldq+}G_I$], which means an ideally-stiff Norton current source not being affected by the grid disturbance v_{odq+}. In other words, the output-voltage feedforward mitigates the output admittance of a current-loop-controlled VSI and helps the current controller to reject the grid disturbance. However, Z_{Fv} is a negative impedance (possible negative damping) and influenced by G_{del}, which would introduce right-half-plane (RHP) poles/zeros to the output impedance when the feedforward gain F_v is too large, as shown in Fig. 12.

2) Output-current feedforward - Z_{Fi}: As derived in the voltage-loop impedance circuit model in Fig. 10, the output-current feedforward is also equivalent to a virtual impedance Z_{Fi} in series with the source impedance $Z_{inner}//Z_{parallel}$ and the coupling inductor L_c, with

$$Z_{Fi} = -(Z_{inner}//Z_{parallel})F_iG_I \tag{6}$$

With considering Z_{Fi}, the inner impedance of the Thevenin voltage source is $Z_{Thevenin} = Z_{inner}//Z_{parallel}+Z_{Fi}$. When the feedforward gain is zero ($F_i = 0$), $Z_{Fi} = 0$ and can be ignored. By contrast, when the feedforward gain is unity ($F_i = 1$) and if the current-loop delay is ignored ($G_I \approx 1$), we get $Z_{Fi} \approx -(Z_{inner}//Z_{parallel})$ and $Z_{Thevenin} \approx 0$. In this case, the feedforward leads to a zero impedance for the Thevenin source not only at steady state but also during system transients [(4) can be re-written as $v_{odq+} = v^*_{odq+}G_V$], which means an ideally-stiff Thevenin voltage source not being affected by the grid disturbance i_{odq+}. In other words, the output-current feedforward mitigates the output impedance of a voltage-loop-controlled VSI and helps the voltage controller to reject the grid disturbance. However, Z_{Fi} is also a negative impedance (possible negative damping) and influenced by G_I. It would introduce RHP poles/zeros to the output impedance when F_i is too large, as shown in Fig. 12.

Above analysis also explains the oscillations caused by the feedforward from the perspective of impedance. Hence, feedforward gains are usually limited less than 1 in practice. $F_v = F_i = 0.5$ is used in this paper for later analysis. It is worth mentioning that voltage and current feedforward gains (F_v and F_i) do not need to be the same. In certain applications, a relatively-large voltage feedforward gain is required due to

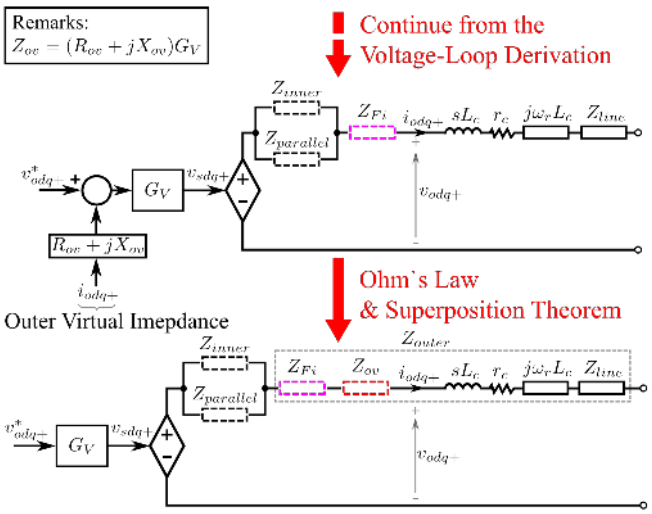


Fig. 13. Derivation of impedance shaping effect of outer virtual impedance Z_{ov}.

not only the rejection of grid-voltage disturbance, but also the limitation of transient-surge current during the start-up procedure of the VSI. (The transient-surge current is also limited by properly initializing the integrator of the inner current loop in practice.) However, damping for the LCL filter or careful adjustment of voltage feedforward gain is required at the same time [31]–[33]. This is out of the scope of this paper and omitted here.

E. Outer Virtual Impedance versus Line Impedance

The impedance shaping effect of the outer virtual impedance is shown in Fig. 13, which is implemented by

$$v_{sdq+} = [v^*_{odq+} - (R_{ov} + jX_{ov})i_{odq+}] \times G_V \tag{7}$$

where $Z_{ov} = (R_{ov} + jX_{ov})G_V$ is added in series with L_c. G_V is the closed-loop gain of the voltage loop, and $G_V \approx 1$ within the bandwidth of the voltage loop. Outer virtual reactance jX_{ov} is usually used to increase the X/R ratio of the grid line impedance, to decouple the active- and reactive-power flows and increase the accuracy of power sharing of droop controllers [34]–[36]. Outer virtual resistance R_{ov} is usually used to damp the subsynchronous oscillations, mitigate the low-frequency voltage harmonics and imbalance, improve the power sharing of nonlinear loads, and limit fault currents [37]–[39]. The impedance shaping effect of outer virtual impedance ($R_{ov} = 0.01$p.u. and $X_{ov} = 0.05$p.u.) is compared with real line impedance ($R_{line} = 0.01$p.u. and $X_{line} = 0.05$p.u.) in Fig. 14. Notably, at low-frequency, the outer virtual impedance has a same impedance effect as the line impedance, but can not damp the high-frequency L_cC_f resonance because of the bandwidth limitation of G_V.

Flux dynamics can also be observed in the figure, which are caused by the compensation of the steady inductance and s-domain inductance: e.g., $\min\{|j\omega_0L_1 + sL_2|\} = 0$ when $s = -j\omega_{res} = -j\omega_0\frac{L_1}{L_2}$. A practical inductor in complex dq frame is simply $(s + jw_0)L$ [21], which indicates the flux resonance at $s = -j\omega_0$. ($-j\omega_0$ in dq frame corresponds to

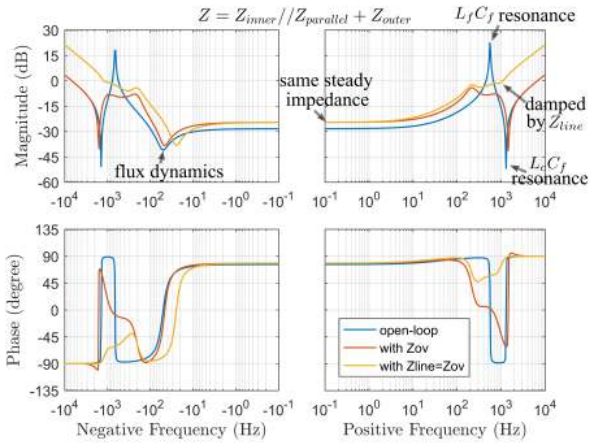


Fig. 14. Impedance shaping effect of outer virtual impedance versus line impedance.

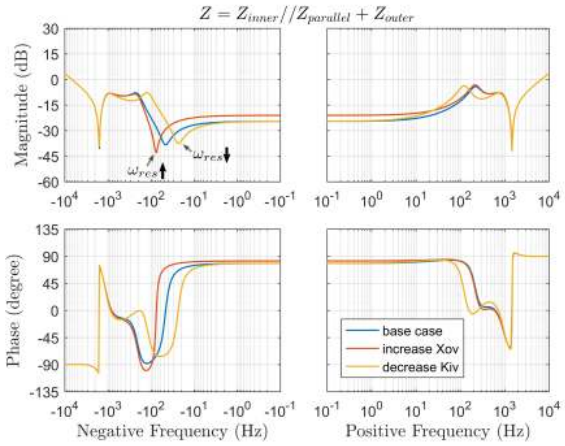


Fig. 15. Shifting the resonant frequency of flux dynamics by changing X_{ov} or K_{iv}.

0Hz in stationary frame, i.e., this resonant impedance valley is simply caused by the low-impedance nature of an inductor at dc.) By contrast, adding virtual inductor would shift this resonant frequency: (a) Adding steady virtual inductor (e.g., X_{ov} in Z_{ov} discussed in last paragraph) makes $L_1 > L_2$ and therefore increases the resonant frequency ω_{res}; (b) Adding s-domain virtual inductor (e.g., $\frac{s}{K_{iv}}$ in Z_{PIv} given by the voltage PI controller) makes $L_2 > L_1$ and therefore reduces the resonant frequency ω_{res}. These effects are shown in Fig. 15. The flux resonant frequency ω_{res} is also related to the system stability, as discussed in Section IV-D later.

F. Summary of Current and Voltage Loops

Fig. 16 summarizes the findings in Sections III-B to III-E. The output impedance of a grid-forming VSI (without droop control) can simply be represented by

$$\begin{aligned} Z_{b\pm}^{m} &= \begin{bmatrix} Z_{b+} & Z_{b-} \\ \overline{Z}_{b-} & \overline{Z}_{b+} \end{bmatrix} \\ &\text{with} \\ Z_{b+} &= Z_{inner}//Z_{parallel} + Z_{outer} \\ Z_{b-} &= 0 \end{aligned} \tag{8}$$

$Z_{b-} = 0$ thanks to the symmetry of current and voltage loops, which also implies that a grid-forming VSI (without droop control) is a SISO system in complex vector dq frame. But as discussed next, the droop-control virtual impedance is asymmetrical, i.e., $Z_{droop-} \neq 0$.

G. Impedance Shaping of Droop Controllers: Preparatory Work

The widely used P-F and Q-V droop controllers are [34]–[36],

$$\begin{cases} \omega_r^* = W_{r0} + m_p(P_0 - P \times \text{LPF}) \\ v_{od}^* = V_{od0} + n_q(Q_0 - Q \times \text{LPF}) \\ v_{oq}^* = 0 \end{cases} \tag{9}$$

P_0 and Q_0 are the setting points of active and reative power values, which are chosen as 0 in this paper. W_{r0} and V_{od0} are the setting points of angular frequency and d-axis voltage, which are chose as their base values W_{base} and V_{base}. P and Q are the measured active and reactive power, which can be calculated by

$$\begin{aligned} P &= v_{od}i_{od} + v_{oq}i_{oq} \\ &= \frac{1}{2}(v_{odq+}i_{odq-} + v_{odq-}i_{odq+}) \\ Q &= -v_{od}i_{oq} + v_{oq}i_{od} \\ &= \frac{1}{2j}(v_{odq+}i_{odq-} - v_{odq-}i_{odq+}) \end{aligned} \tag{10}$$

m_p and n_q are frequency and voltage droop gains, respectively. They can be set based on the required variation ranges of frequency and voltage according to grid codes [40], [41],

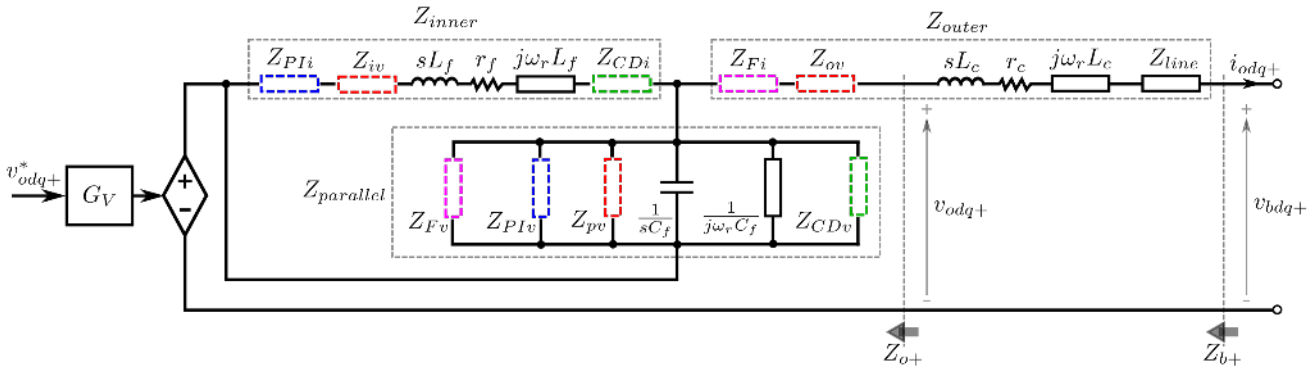
$$\begin{cases} m_p = \Delta\omega\% \frac{W_{base}}{S_{base}} \\ n_q = \Delta V\% \frac{V_{base}}{S_{base}} \end{cases} \tag{11}$$

where S_{base} is the base power. LPF in droop equations indicates the low-pass filter,

$$\text{LPF} = \frac{1}{1 + T_f s} \tag{12}$$

It is used to avoid the interaction between droop controller and inner control loops and provide virtual inertia for system stability [20], [27], [42]. This effect will also be revealed in the virtual impedance later.

As discussed in next two subsections, the droop controller also introduces virtual impedance in series with L_c. This can be intuitively explained that a stable power system holds a relatively constant voltage in dq frame, so that P and Q are approximately proportional to VSI output currents i_{odq+} and i_{odq-} and fed back to the control loop, just like adding the outer virtual impedance Z_{ov} in Section III-E. But droop



Virtual Impedance	$Z_{iv} = (R_{iv} + jX_{iv})G_{del}$ $Z_{pv} = \frac{(R_{pv}//jX_{pv})}{G_I}$ $Z_{ov} = (R_{ev} + jX_{ev})G_V$
PI Controller	$Z_{PIi} = PI_iG_{del} = (K_{pi} + \frac{K_{ii}}{s})G_{del} = (K_{pi} + \frac{1}{s\frac{1}{K_{ii}}})G_{del}$ $Z_{PIv} = \frac{1}{PI_vG_I} = \frac{1}{(K_{pi}+\frac{K_{iv}}{s})G_I} = \frac{(\frac{1}{K_{pv}}//s\frac{1}{K_{iv}})}{G_I}$
Cross Decoupling	$Z_{CDi} = -j\omega_0 L_f G_{del}$ $Z_{CDv} = \frac{1}{-j\omega_0 C_f G_I}$
Feedforward	$Z_{Fv} = -\frac{Z_{inner}}{F_vG_{del}}$ $Z_{Fi} = -(Z_{inner}//Z_{parallel})F_iG_I$
Loop Gain & Delay	$G_{del} = e^{-1.5T_s s}$ $G_I = \frac{Z_{PIi}}{Z_{inner}}$ $G_V = \frac{Z_{inner}//Z_{parallel}}{Z_{PIv}}$

Fig. 16. Impedance circuit model of a grid-forming VSI with constant voltage and frequency reference signals (i.e., a symmetric system) in complex dq frame.

control makes the VSI output impedance asymmetric, i.e., (8) should be changed to

$$Z^m_{tot\pm} = Z^m_{b\pm} + Z^m_{QV\pm} + Z^m_{PF\pm} = \begin{bmatrix} Z_{tot+} & Z_{tot-} \\ \overline{Z}_{tot-} & \overline{Z}_{tot+} \end{bmatrix}$$

with (13)

$$Z_{tot+} = Z_{inner}//Z_{parallel} + Z_{outer} + Z_{QV+} + Z_{PF+}$$
$$Z_{tot-} = Z_{QV-} + Z_{PF-}$$

where $Z^m_{QV\pm}$ and $Z^m_{PF\pm}$ are virtual impedances given by Q-V and P-F droop control, respectively. The corresponding impedance circuit model is shown in Fig. 17. In this model, voltage and current are vectors including both forward and backward components (e.g., $i_{odq\pm} = [i_{odq+}, i_{odq-}]^T$); transfer functions and impedances are matrices (e.g., $Z^m_{inner} = \text{diag}[Z_{inner}, \overline{Z}_{inner}]$ where the overbar indicates the conjugate operation as discussed in Fig. 2). Detailed expressions of $Z^m_{QV\pm}$ and $Z^m_{PF\pm}$ are analyzed next.

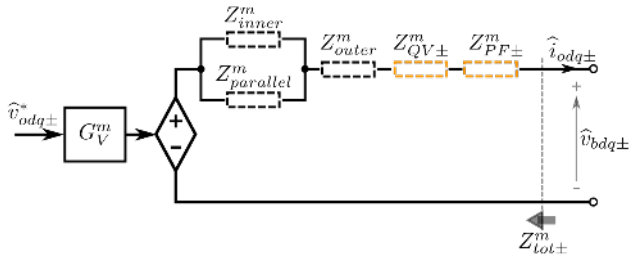


Fig. 17. Small-signal impedance circuit model of a droop-controlled grid-forming VSI (i.e., an asymmetric system) in complex dq frame. [Remarks: Voltage and current signals are two-dimension vectors, e.g., $\hat{v}^*_{odq\pm} = [\hat{v}^*_{odq+}; \hat{v}^*_{odq-}]$; Impedances are 2-by-2 matrices, e.g., $Z^m_{PF\pm} = [Z_{PF+}, Z_{PF-}; \overline{Z}_{PF-}, \overline{Z}_{PF+}]$.]

H. Q-V Droop Controller versus Outer Virtual Reactance

As shown in detail in Appendix A, the small-signal Q-V droop virtual impedance gives

$$Z^m_{QV\pm} = n_q \text{LPF} \frac{1}{2} V_o \begin{bmatrix} je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \\ je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \end{bmatrix} \quad (14)$$

V_o and ϕ_{V_o} are the magnitude and phase angle of v_{odq} at the linearized steady-state operating point.

Simplifications are conducted next to reveal the essence of the impedance more clearly. Because $v_{oq}^* = 0$, $\phi_{V_o} \approx 0$ should be valid at steady state. In this case, $Z_{QV\pm}^m$ can be further simplified to

$$Z_{QV\pm}^m \approx j \underbrace{n_q \text{LPF} \frac{1}{2} V_o}_{X_{QV}} \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} \tag{15}$$

i.e., a positive reactance in forward frame and a negative reactance in backward frame. The reactance value is

$$\begin{aligned} X_{QV} &= n_q \text{LPF} \frac{1}{2} V_o = \Delta V\% \frac{V_{base}}{S_{base}} \text{LPF} \frac{1}{2} V_o \\ &\approx \Delta V\% Z_{base} \frac{1}{2} \text{LPF} \end{aligned} \tag{16}$$

This reveals the equivalence of $Z_{QV\pm}^m$ and outer virtual reactance X_{ov}, except that $Z_{QV\pm}^m$ is asymmetric. Additionally, it also implies that using X_{ov} only should also be able to achieve similar reactive-power-sharing and voltage-supporting capabilities as the Q-V droop control, which fortunately has already been validated in [34]–[36], [43]. Hence, for simplicity, the virtual reactance of $X_{ov} = 0.05$p.u. is used in later analysis, which corresponds to 5% voltage variation when generating/absorbing 1p.u. reactive power and achieves a similar effect of using $n_q = 5\% \frac{V_{base}}{S_{base}}$ in Q-V droop control.

I. P-F Droop Controller versus Virtual Synchronous Generator

As shown in detail in Appendix B, the small-signal P-F droop virtual impedance gives

$$Z_{PF\pm}^m = \frac{V_o^2}{2Z_{PF,D}} \begin{bmatrix} j & je^{j2\phi_{V_o}} \\ -je^{-j2\phi_{V_o}} & -j \end{bmatrix} \tag{17}$$

with

$$Z_{PF,D} = s^2 \frac{T_f}{m_p} + s \frac{1}{m_p} + V_o I_o \text{sin}(\phi_{I_o} - \phi_{V_o}) \tag{18}$$

The total output impedance can be obtained as

$$Z_{tot\pm}^m = Z_{b\pm}^m + Z_{QV\pm}^m + Z_{PF\pm}^m \tag{19}$$

where $Z_{b\pm}^m$ represents the inner-loop dynamics can be calculated by the impedance circuit model in Fig. 16, $Z_{PF\pm}^m$ illustrates the frame dynamics (i.e., the grid synchronization) and can be calculated by (17) and (18), and $Z_{QV\pm}^m = 0$ here because the virtual reactance X_{ov} (which is included in $Z_{b\pm}^m$) rather than the Q-V droop is used. The total output admittance can also be obtained as

$$\begin{aligned} &Y_{tot\pm}^m = Z_{tot\pm}^{-1} \\ &= \frac{1}{Y_{tot,D1} Y_{tot,D2}} \begin{bmatrix} Z_{PF,D} \overline{Z}_{b+} - j\frac{V_o^2}{2} & -j\frac{V_o^2}{2} e^{j2\phi_{V_o}} \\ j\frac{V_o^2}{2} e^{-j2\phi_{V_o}} & Z_{PF,D} Z_{b+} + j\frac{V_o^2}{2} \end{bmatrix} \end{aligned} \tag{20}$$

with denominators

$$\begin{aligned} Y_{tot,D1} &= s^2 \frac{T_f}{m_p} + s \frac{1}{m_p} + Re\Big\{ j \frac{V_b V_o}{Z_{b+}} e^{j(\phi_{V_b} - \phi_{V_o})} \Big\} \\ Y_{tot,D2} &= Z_{b+} \overline{Z}_{b+} \end{aligned} \tag{21}$$

If assuming Z_{b+} is constant (i.e., ignoring the dynamics of inner loops) and is pure inductive (i.e., $Z_{b+} = jX_{b+}$), $Y_{tot,D1}$ can be re-written as

$$Y_{tot,D1} = s^2 \frac{T_f}{m_p} + s \frac{1}{m_p} + \frac{V_b V_o}{X_{b+}} \text{cos}(\phi_{V_b} - \phi_{V_o}) \tag{22}$$

which is exactly same to the swing equation of a synchronous generator [5], [12]: $\frac{T_f}{m_p}$ is the rotor inertia J; $\frac{1}{m_p}$ is the damping torque coefficient K_D; and $\frac{V_b V_o}{X_{b+}} \text{cos}(\phi_{V_b} - \phi_{V_o})$ is the synchronizing torque coefficient K_S. The roots of $Y_{tot,D1}$ are the poles of $Y_{tot\pm}^m$ and influence the VSI dynamics. In other words, the P-F droop adds synchronous-generator-like properties into the VSI and achieves the grid synchronization. This reveals the equivalence of frequency droop and virtual synchronous generator, and also coincides with the findings in [27], [42]. It is also worth mentioning that, the impedance shaping effect of this synchronization loop is obviously influenced by steady-state operating points of the VSI [especially, the power factor angle of the converter and the angle difference between the converter and external grid according to (18) and (22), respectively].

The bode diagrams of output impedance/admittance of the VSI are shown in Fig. 18, to compare the VSI dynamics with and without P-F droop. Notably, the frequency integral effect at low-frequency range (caused by $Z_{PF,D}$) and the swing dynamics at around $\pm$5Hz (caused by $Y_{tot,D1}$) can be observed only when the P-F droop is added. Flux dynamics can also be observed at around -50Hz, which are resulted by the system inductance and are discussed in Section III-E earlier. The impedance measured by simulation is also included in Fig. 18(b) for validating the proposed impedance circuit model, as discussed in next section.

IV. Model Discussion and Validation

The impedance circuit model of a grid-forming inverter is derived in last section. In this section, the advantages and constraints of the proposed model will be discussed, followed by conducting simulations and experiments to validate the model.

A. Model Discussion

The proposed impedance circuit model is shown in Fig. 16 and Fig. 17, and summarized in Table I. This modeling tool has the following characteristics:

(a) It simplifies the output impedance calculation from a multi-loop-coupled block-diagram-algebra problem (conventional approach) to a series/parallel impedance-circuit problem, and therefore gives a more visualized and straightforward impedance shaping procedure.

(b) The model breaks the conventional all-in-one impedance into discrete circuit elements, as summarized in Fig. 16 and Fig. 17. Specifically, it can clearly show the virtual impedance essence (e.g., resistance, inductance, capacitance, etc) of different control parameters at different impedance locations (e.g., Z_{inner}, $Z_{parallel}$, or Z_{outer}) and within different frequency bandwidths (e.g., near switching/sampling frequency

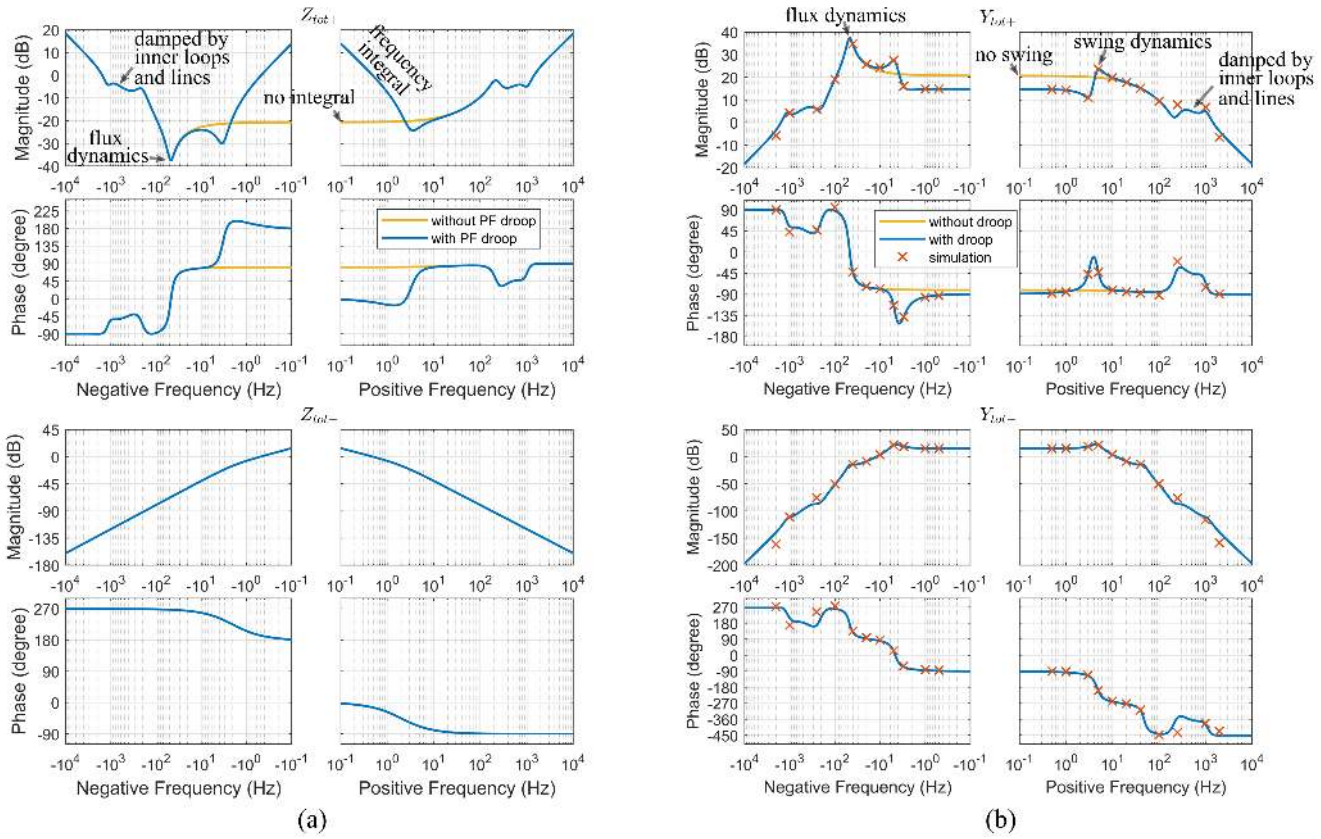


Fig. 18. Bode diagrams of the output impedance/admittance of the droop-controlled grid-forming VSI. (a) Impedance. (b) Admittance.

by multiplying G_{del}, within current-loop bandwidth by multiplying G_I, within voltage-loop bandwidth by multiplying G_V, within droop-loop bandwidth by multiplying LPF). In addition, the positive/negative damping effects (i.e., passivity [44]) of each controller parameters can also be evaluated directly from the corresponding virtual impedance, which can straightforwardly guide the controller design and parameter tuning in practice.

(c) When deriving the impedance circuit model, linearization is applied, but for droop control only, i.e., the values of $Z^m_{PF\pm}$ and $Z^m_{QV\pm}$ are influenced by the steady-state operating points of the system. But for inner voltage and current loops, linearization is not required, i.e., the values of Z_{inner}, $Z_{parallel}$, and Z_{outer} depend on controller and LCL filter parameters only. The non-linearity of inner loops (e.g., the saturation of current reference for protection) is not considered in this paper. When reaching these saturation limits under certain grid scenarios, the impedance circuit model of the converter should be degraded with setting certain impedances to zero or infinite, which is expected to be investigated in the future to generalize the proposed model.

(d) This paper uses the moving average operator in each switching period to model a three-phase balanced VSI [26]. The PWM and converter switching are simply neglected by averaging all system variables over one switching period. If it is required to analyze the high-frequency harmonic stability (e.g., the sideband oscillations caused by the converter switching and PWM) or to analyze the three-phase imbalance, advanced modeling methods have to be used, such as generalized averaging (also known as dynamic phasor), harmonic state space (HSS), etc [45].

In the following subsections, a droop-controlled grid-forming VSI connected to a infinite bus (as shown in Fig. 19) is tested to validate the proposed impedance circuit model in both frequency- and time-domain through simulations and experiments. The system parameters are organized in Table II. The droop-controlled grid-forming VSI can operate in both grid-connected mode and stand-alone mode, but is more likely to become unstable when connecting to external grid because of the swing interaction between the converter and external grid, which therefore is focused in this paper.

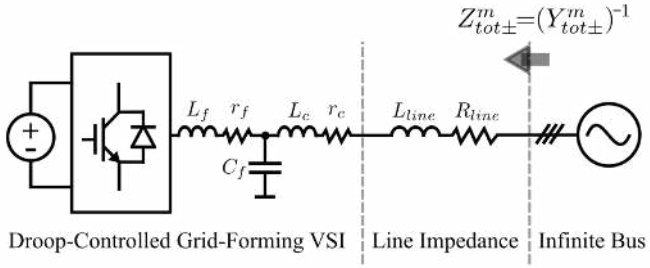


Fig. 19. Configuration of the tested system consisting of a droop-controlled grid-forming VSI, an infinite bus, and transmission/distribution lines.

TABLE I
SUMMARY OF ELEMENTS IN THE IMPEDANCE CIRCUIT MODEL

Controller	Symbol	Physical Interpretation	Remarks
Current PI_i	Z_{PIi}	A virtual resistor and a virtual capaitor in series with converter-side inductor L_f.	a) Influenced by the control delay G_{del}. b) Damping for LCL resonance. c) Possible negative damping effect at high frequency range.
Voltage PI_v	Z_{PIv}	A virtual resistor and a virtual inductor in parallel with C_f.	a) Influenced by the current-loop gain G_I. b) Shifting the resonant frequency point of flux dynamics, which may lead to the interaction with outer droop controller and the instability when K_{iv} is too small.
Output Voltage Feedforward	Z_{Fv}	Negative virtual admittance compensating the current-loop Norton source admittance.	a) Influenced by the control delay G_{del}. b) Rejection of grid voltage disturbance. c) Possible instability with large feedforward gain F_v. d) Help on the limitation of start-up transient-surge current.
Output Current Feedforward	Z_{Fi}	Negative virtual impedance compensating the voltage-loop source impedance.	a) Influenced by the current-loop gain G_I. b) Rejection of grid current disturbance. c) Possible instability with large feedforward gain F_i.
Cross Decoupling	Z_{CDi} Z_{CDv}	Negative virtual impedance compensating the coupling effect between dq axes.	N/A
Q-V Droop	$Z^m_{QV\pm}$	Asymmetric virtual reactance in series with grid-side inductor L_c.	a) Influenced by the voltage-loop gain G_V. b) Reactive power sharing and voltage support.
P-F Droop	$Z^m_{PF\pm}$	Asymmetric virtual impedance in series with grid-side inductor L_c.	a) Active power sharing and frequency support. b) Virtual synchronous generator.
Inner virtual impedance	Z_{iv}	Normally a virtual resistor in series with converter-side inductor L_f	a) Influenced by the control delay G_{del}. b) Damping LCL resonance (similarly to K_{pi} of PI_i).
Parallel virtual impedance	Z_{pv}	Normally a virtual resistor in parallel with C_f	a) Influenced by the current-loop gain G_I b) Damping LCL resonance (similarly to K_{pv} of PI_v).
Outer virtual impedance	Z_{ov}	Normally a virtual resistor and a virtual inductor in series with grid-side inductor L_c	a) Influenced by the voltage-loop gain G_V. b) Virtual resistor: b.1) Damping low-frequency range oscillations. b.2) Dealing with low-frequency harmonics, imbalance, and non-linearity. c) Virtual inductor: c.1) Decoupling the active and reactive power flow. c.2) Reactive power sharing and voltage supporting (similarly to the Q-V droop).

B. Frequency-Domain Validation: Spectrum Measurement

The $Y^m_{tot\pm}$ spectrum of the tested system can be measured similarly to [9], [12], [18], [19], [46]. The simulated results are shown in Fig. 18(b). Noticeably, the measured admittance agrees with the theoretical results and shows similar dynamics: swing dynamics at around $\pm$5Hz, flux dynamics at around $-$50Hz, and damping effects at mid-high frequency range.

C. Time-Domain Validation: System Step Response

Experiments are conducted to show the time-domain transients of the system. Fig. 20 shows the VSI dynamics responding to a step frequency change of the infinite bus. At 0.1s, the infinite-bus frequency is set from 49.75Hz (99.5%p.u.) to 49.7Hz (99.4%p.u.). Then, the VSI's power and frequency suffer short-term swing oscillations and settles down to their new steady states. The swing dynamics in Fig. 20 (inside the dashed circle) can be clearly shown during the transient, with a oscillation frequency of around 5Hz, which coincides with the frequency of swing dynamics in the admittance spectrum Fig. 18(b).

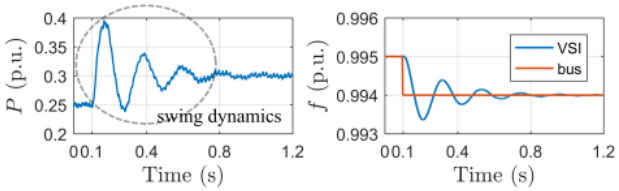


Fig. 20. Experiment: VSI dynamic performance with $m_p = 2\%\frac{W_{base}}{S_{base}}$ under a step frequency change of the infinite bus.

D. Example: Droop-Related Stability and Loop Interaction

The sub-impedances in Z_{inner}, $Z_{parallel}$, and Z_{outer} in Fig. 16 can clearly show the damping effects of different parameters of current and voltage loops and reveal their interactions through bandwidths, as discussed in Section III. As for the frequency droop impedance, its effect on the system stability and its interaction with inner loops is not that straightforward, even though some discussions have already been given in Sections III-G to III-I earlier. So, this topic is

TABLE II
PARAMETERS OF THE TESTED SYSTEM

Base Values		
Power	S_{base}	10kVA
Voltage	V_{base}	380V
Frequency	F_{base}	50Hz
Angular Frequency	W_{base}	$2\pi F_{base}$
Current	I_{base}	S_{base}/V_{base}
Impedance	Z_{base}	V_{base}/I_{base}
LCL Filter and Grid Line Impedance		
Filtering Inductor	L_f	0.0294p.u.
Inner Resistance of L_f	r_f	0.0069p.u.
Filtering Capacitor	C_f	0.2268p.u.
Coupling Inductor	L_c	0.0076p.u.
Inner Resistance of L_c	r_c	0.0021p.u.
Line Inductance	L_{line}	0.0338p.u.
Line Resistance	R_{line}	0.0124p.u.
Controller Parameters		
Bandwidth Index	w_i	10p.u.
Current PI	K_{pi} K_{ii}	$w_i L_f$ $w_i^2 L_f/4$
Voltage PI	K_{pv} K_{iv}	$1/(16 w_i L_f)$ $1/(4L_f)$
Feedforward Gain	$F_i = F_v$	0.5
P-F Droop Gain	m_p	$2\% \frac{W_{base}}{S_{base}}$
LPF Time Constant	T_f	$1/(2\text{Hz} \times 2\pi)$
Outer Virtual Reactance (For Q-V droop)	X_{ov}	0.05p.u.
Steady-State Operating Points		
Capacitor Voltage	$V_o \angle \phi_{V_o}$	1p.u.$\angle -0.86°$
Infinite Bus Voltage	$V_b \angle \phi_{V_b}$	1p.u.$\angle -1.60°$
Output Current	$I_o \angle \phi_{I_o}$	0.3031p.u.$\angle 8.21°$
Operating Frequency	W_r	0.994p.u.

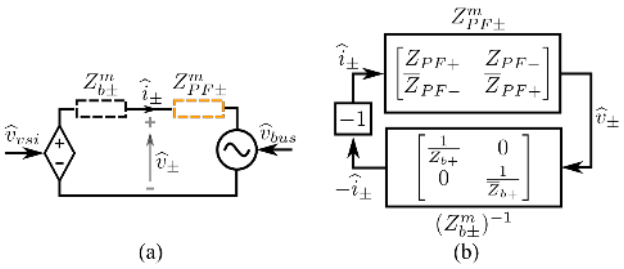


Fig. 21. Small-signal equivalent system for analyzing the interaction between the frequency droop with the rest system. (a) Equivalent circuit. (b) Block diagram.

discussed next, in order to further highlight the potential of the proposed impedance circuit model.

The equivalent circuit for the tested system is displayed in Fig. 21(a) with separating $Z^m_{PF\pm}$ from the rest system. As the infinite bus voltage is stable, the stability of the whole system is determined by:

$$\hat{i}_\pm = \underbrace{(Z^m_{b\pm} + Z^m_{PF\pm})^{-1}}_{Y^m_{tot\pm}}(\hat{v}_{vsi} - \hat{v}_{bus}) \tag{23}$$

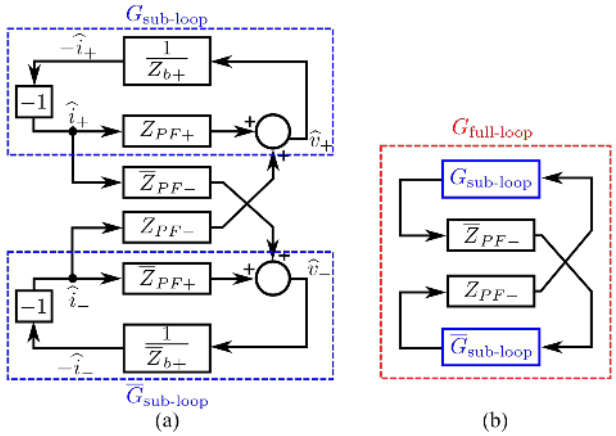


Fig. 22. Scalar block diagram of the investigated system. (a) Sub-loop. (b) Full-loop.

which is equivalently to

$$\hat{i}_\pm = \underbrace{\left((Z^m_{b\pm})(1 + (Z^m_{b\pm})^{-1} Z^m_{PF\pm})\right)^{-1}}_{Y^m_{tot\pm}} (\underbrace{G^m_V \hat{v}^*_{vsi}}_{\hat{v}_{vsi}} - \hat{v}_{bus}) \tag{24}$$

Hence, the system stability is equivalent to the stability of two terms: $\hat{v}_{vsi}$ and $Y^m_{tot\pm}$. Furthermore, the stability of $\hat{v}_{vsi}$ is equivalent to the stability of G^m_V; and the stability of $Y^m_{tot\pm}$ is equivalent to the stability of both $Z^m_{b\pm}$ and $(1 + (Z^m_{b\pm})^{-1} Z^m_{PF\pm})$. G^m_V is the voltage-loop gain and $Z^m_{b\pm}$ is the impedance effect of filter and inner loops. The stability of G^m_V and $Z^m_{b\pm}$ has already been ensured when designing the inner voltage and current loops in practice. Therefore, we can focus on the third term "$(1 + (Z^m_{b\pm})^{-1} Z^m_{PF\pm})$" only, which is equivalent to the stability of the feedback system in Fig. 21(b). Tranditional approach for stability analysis needs to calculate the eigenvalues of the return ratio $(Z^m_{b\pm})^{-1} Z^m_{PF\pm}$ and apply the generalized Nyquist stability criterion, for example in [9], [11], [47], which however obviously requires tedious calculations, especially when an analytical solution is required. Additionally, it is also challenging to link the eigenvalues back to the orignal elements of $Z^m_{b\pm}$ and $Z^m_{PF\pm}$, which increase the difficulty when locating the origin of the system instability. Hence, in this paper, the loop analysis method proposed in [48] is used to solve these problems, as discussed next. This feedback system can be equivalently transformed to a scalar block diagram Fig. 22, where the system stability depends on the stability of sub-loop in (a) and full-loop in (b). The Bode diagrams are shown in Fig. 23. Notably, the full-loop is always stable with changing the droop gain m_p, hence we can focus on the sub-loop only. The upper sub-loop in Fig. 22(a) is analyzed because two sub-loops are complex conjugate and hold the same property of stability. Instead of plotting the open-loop gain (i.e., the return ratio Z_{PF+}/Z_{b+}), we plot Z_{PF+} and Z_{b+} in Fig. 23(a) respectively to preserve the features of the original elements of impedance matrices, which helps to analyze the origin of the instability. The phase margin can be checked by investigating the phase difference where their magnitudes intersect [11], [49]. Notably, the positive-frequency intersection points always satisfy the sta-

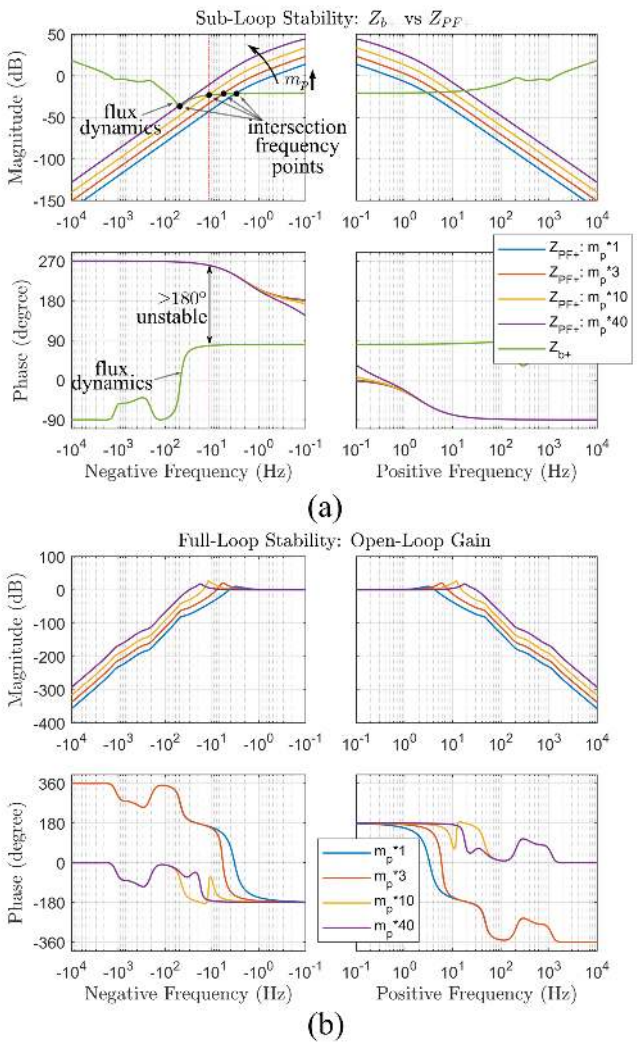


Fig. 23. Bode diagrams with increasing the droop gain m_p. (a) Sub-loop stability: Z_{b+} vs Z_{PF+}. (b) Full-loop stability: open-loop gain $G_{op} = G_{\text{sub-loop}}\overline{G}_{\text{sub-loop}}Z_{PF-}\overline{Z}_{PF-}$.

bility criterion. But with the increase of the droop gain m_p, the absolute value of negative intersection frequency increases, and the phase difference also increases (implying smaller phase margin) until it is out of $180°$ (implying the unstable system). Fig. 24 displays the unstable case by experiment test. The derived swing equation in (22) also implies same system dynamics because $\frac{1}{m_p}$ is the damping coefficient: the larger of m_p, the smaller of system damping, the more chances of system instability. It is worth mentioning that discussions given in this paragraph coincide the state-space-based analysis in [6].

We can get deeper insights about the interaction between the frequency droop and inner loops by investigating Fig. 23 further. We also can focus on the sub-loop in (a) only. Notably, with the increase of the absolute value of the negative intersection frequency, the phase of Z_{PF+} increases caused by the Laplace operator s in the denominator $Z_{PF,D}$ in (18), and the phase of Z_{b+} decreases nearing -50Hz caused by the flux dynamics (inductance dynamics) discussed in Section III-E

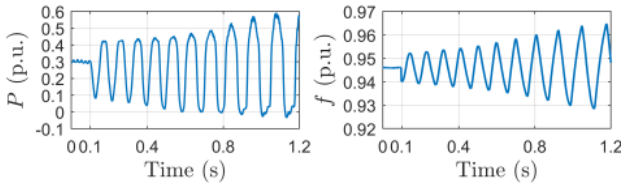


Fig. 24. Experiment: Unstable test with $m_p = 10 \times m_{p,rated}$.

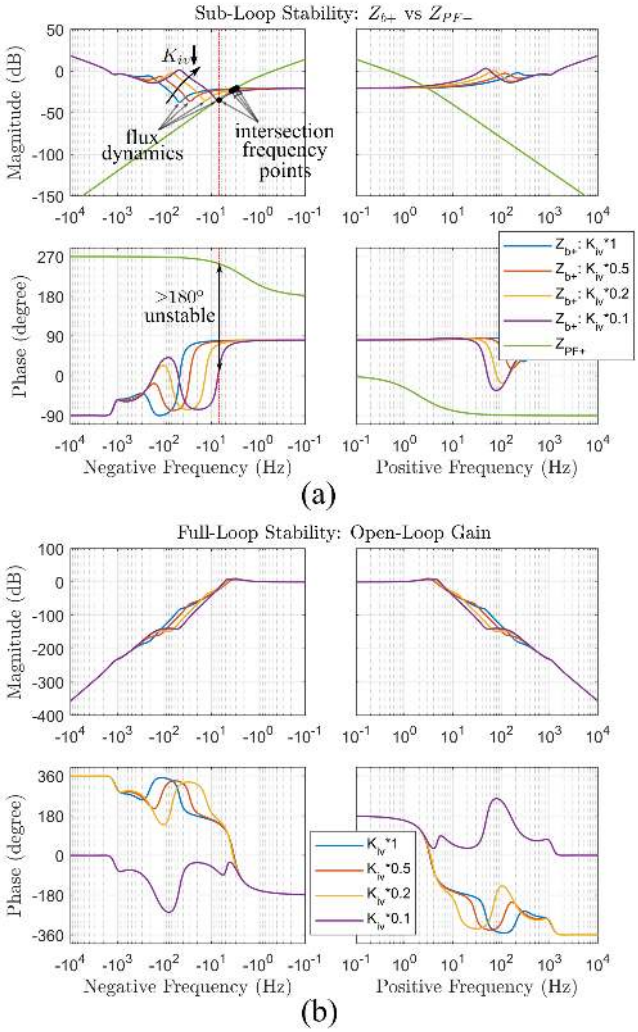


Fig. 25. Bode diagrams with decreasing the integral gain K_{iv} of voltage PI controller. (a) Sub-loop stability: Z_{b+} vs Z_{PF+}. (b) Full-loop stability: open-loop gain $G_{op} = G_{\text{sub-loop}}\overline{G}_{\text{sub-loop}}Z_{PF-}\overline{Z}_{PF-}$.

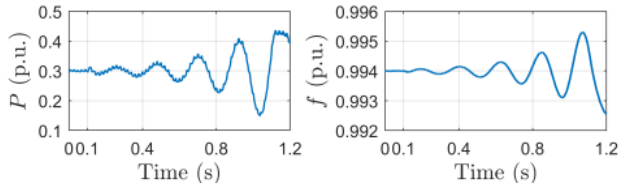


Fig. 26. Experiment: Unstable test with $K_{iv} = 0.1 \times K_{iv,rated}$.

earlier. This inductance includes both the real inductor (given by VSI's filter and system lines) and the virtual inductor (given

by $\frac{s}{K_{iv}}$ of voltage PI controller and X_{ov} of the outer virtual impedance Z_{ov}). Fig. 25 shows the Bode diagram with fixing m_p but reducing K_{iv} gradually. Notably, the smaller of K_{iv}, the smaller of the resonance frequency of the flux dynamics, and the larger of phase difference between two impedances (smaller phase margin). The system becomes unstable when K_{iv} is too small. The unstable experiment test is shown in Fig. 26, validating the analysis. It is worth highlighting that, while the system stability can also be evaluated by using the conventional all-in-one impedance, however the interaction between the voltage and droop loops can be clearly shown only by investigating the corresponding impedance elements in the impedance circuit model, i.e., Z_{PF+} and Z_{PIv} in this example. Hence the proposed model obviously gives more insights about the system stability and can guide the controller design in practice. Discussions given in this paragraph also coincide with the state-space-based analysis of loop interaction in [7].

V. Conclusions

The concept of *impedance circuit model* was proposed, which visualizes control loops of power converters as discrete circuit elements in an impedance circuit, and therefore provides an intuitive impedance modeling framework for power converters. The proposed tool was applied to a droop-controlled grid-forming VSI as the example, with analyzing the droop-related stability in details. It has been proved by simulation and experiment that the large droop gain of P-F droop controller or the small integral gain of voltage PI controller would lead to the system instability.

Appendix A
Impedance Shaping Effect of Q-V Droop

The Q-V droop virtual impedance is derived here. By linearizing (10) and combining the results with (9), we can get the small-signal voltage references as

$$\widehat{v}^*_{odq+} = \widehat{v}^*_{odq-} = -n_q \cdot \text{LPF} \cdot \frac{1}{2j} \times \left(\begin{bmatrix} -V_{odq-} & V_{odq+} \end{bmatrix} \begin{bmatrix} \widehat{i}_{odq+} \\ \widehat{i}_{odq-} \end{bmatrix} + \begin{bmatrix} I_{odq-} & -I_{odq+} \end{bmatrix} \begin{bmatrix} \widehat{v}_{odq+} \\ \widehat{v}_{odq-} \end{bmatrix} \right) \tag{25}$$

with steady-state operating points of

$$\begin{cases} V_{odq+} = V_o \angle \phi_{V_o} \\ V_{odq-} = V_o \angle -\phi_{V_o} \end{cases} ; \quad \begin{cases} I_{odq+} = I_o \angle \phi_{I_o} \\ I_{odq-} = I_o \angle -\phi_{I_o} \end{cases} \tag{26}$$

(25) can be re-written as

$$\begin{aligned} \begin{bmatrix} \widehat{v}^*_{odq+} \\ \widehat{v}^*_{odq-} \end{bmatrix} = & - n_q \cdot \text{LPF} \cdot \frac{1}{2j} \times \\ & \left(V_o \begin{bmatrix} je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \\ je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \end{bmatrix} \begin{bmatrix} \widehat{i}_{odq+} \\ \widehat{i}_{odq-} \end{bmatrix} \right. \\ & \left. + I_o \begin{bmatrix} -je^{-\phi_{I_o}} & je^{\phi_{I_o}} \\ -je^{-\phi_{I_o}} & je^{\phi_{I_o}} \end{bmatrix} \begin{bmatrix} \widehat{v}_{odq+} \\ \widehat{v}_{odq-} \end{bmatrix} \right) \end{aligned} \tag{27}$$

Within the bandwidth of LPF, $\widehat{v}_{odq+} \approx \widehat{v}^*_{odq+}$ and $\widehat{v}_{odq-} \approx \widehat{v}^*_{odq-}$. Hence, the impedance shaping effect of the Q-V droop can be derived as

$$\begin{aligned} Z^m_{QV\pm} = & \left(I + n_q \text{LPF} \frac{1}{2} I_o \begin{bmatrix} je^{-\phi_{I_o}} & -je^{\phi_{I_o}} \\ je^{-\phi_{I_o}} & -je^{\phi_{I_o}} \end{bmatrix} \right)^{-1} \\ & \times \left(n_q \text{LPF} \frac{1}{2} V_o \begin{bmatrix} je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \\ je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \end{bmatrix} \right) \end{aligned} \tag{28}$$

Noticing that

$$|n_q \text{LPF} \frac{1}{2} I_o| = |\Delta V\% \frac{V_{base} I_o}{S_{base}} \text{LPF} \frac{1}{2}| \ll 1 \tag{29}$$

i.e.,

$$\left(I + n_q \text{LPF} \frac{1}{2} I_o \begin{bmatrix} je^{-\phi_{I_o}} & -je^{\phi_{I_o}} \\ je^{-\phi_{I_o}} & -je^{\phi_{I_o}} \end{bmatrix} \right)^{-1} \approx I^{-1} = I \tag{30}$$

We get

$$Z^m_{QV\pm} \approx n_q \text{LPF} \frac{1}{2} V_o \begin{bmatrix} je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \\ je^{-\phi_{V_o}} & -je^{\phi_{V_o}} \end{bmatrix} \tag{31}$$

Appendix B
Impedance Shaping Effect of P-F Droop

The P-F droop virtual impedance is derived here. By linearizing (10) and combining the results with (9), we can get the small-signal frequency reference as

$$\widehat{\omega}^*_r = -m_p \cdot \text{LPF} \cdot \frac{1}{2} \times \left(\begin{bmatrix} V_{odq-} & V_{odq+} \end{bmatrix} \begin{bmatrix} \widehat{i}_{odq+} \\ \widehat{i}_{odq-} \end{bmatrix} + \begin{bmatrix} I_{odq-} & I_{odq+} \end{bmatrix} \begin{bmatrix} \widehat{v}_{odq+} \\ \widehat{v}_{odq-} \end{bmatrix} \right) \tag{32}$$

at steady-state operating points in (26). Within the bandwidth of LPF, $\widehat{w}_r \approx \widehat{w}^*_r$. According to [12], the droop effect will be reflected in two different ways in (a) swing-rotating frame; and (b) steady-rotating frame.

Swing-rotating frame: This frame is aligned to the VSI's dq axes. As discussed in [12], the P-F droop in this frame only introduces a small perturbation to the impedance of passive components, e.g., changing jW_rL_f to $j(W_r + \widehat{w}_r)L_f$, which can be ignored because $\widehat{w}_r \ll W_r$.

Steady-rotating frame: This frame rotates with a constant angular frequency. Therefore, the angle and frequency oscillations of the VSI's dq axes can be observed. The impedance shaping effect in this frame can be derived following a analogous way as in [12], as shown next:

According to (32), the small-signal angle difference between the swing frame and steady frame can be calculated by

$$\widehat{\epsilon} = \frac{\widehat{\omega}_r}{s} = K' \begin{bmatrix} \widehat{i}_{odq+} \\ \widehat{i}_{odq-} \end{bmatrix} \tag{33}$$

with

$$\begin{aligned} K' = & - m_p \cdot \text{LPF} \cdot \frac{1}{s} \cdot \frac{1}{2} \\ & \times \left(\begin{bmatrix} V_{odq-} & V_{odq+} \end{bmatrix} + \begin{bmatrix} I_{odq-} & I_{odq+} \end{bmatrix} Z^m_{o\pm} \right) \end{aligned} \tag{34}$$

where $Z^m_{o\pm}$ is the VSI output impedance without considering the coupling inductor L_c, as shown in the impedance circuit model in Fig. 16. Noticing that within the bandwidth of LPF, $Z_{o-,p.u.} = 0$ and $Z_{o+,p.u.} \approx Z_{ov,p.u.} \ll 1$p.u. (i.e., $I_o Z_{o+} \ll V_o$). Hence, K' can be simplified to

$$K' \approx -m_p \cdot \text{LPF} \cdot \frac{1}{s} \cdot \frac{1}{2} \times \begin{bmatrix} V_{odq-} & V_{odq+} \end{bmatrix} \tag{35}$$

K' indicates the transfer function from the converter output current i_{odq} to the angle difference $\widehat{\epsilon}$, and can be used to calculate the impedance shaping effect of frequency droop as [12],

$$Z^m_{PF\pm} = \left((Z^m_{b\pm} + Z^m_{QV\pm}) + \begin{bmatrix} jV_{bdq+} \\ -jV_{bdq-} \end{bmatrix} K' \right) \left(I + \begin{bmatrix} jI_{odq+} \\ -jI_{odq-} \end{bmatrix} K' \right)^{-1} - (Z^m_{b\pm} + Z^m_{QV\pm}) \tag{36}$$

where $Z^m_{b\pm}$ is the VSI output impedance at the bus terminal, as shown in the impedance circuit model in Fig. 16 as well. Combing (34) and (36), we get

$$Z^m_{PF\pm} = \frac{V_o^2}{2Z_{PF,D}} \begin{bmatrix} j & je^{j2\phi_{V_o}} \\ -je^{-j2\phi_{V_o}} & -j \end{bmatrix} \tag{37}$$

with

$$Z_{PF,D} = s^2 \frac{T_f}{m_p} + s\frac{1}{m_p} + V_o I_o \text{sin}(\phi_{I_o} - \phi_{V_o}) \tag{38}$$

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