Impedance Modeling and Analysis of Multi-stacked On-chip Power Distribution Network in 3D ICs

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Impedance Modeling and Analysis of Multi-stacked On-chip Power Distribution Network in 3D ICs

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Abstract

An accurate impedance modeling of a multi-stacked on-chip power distributed network (PDN) based on through-silicon-vias (TSVs) is vitally important to estimate the electrical performance in three-dimensional integrated circuits (3D ICs). This paper proposed a method for calculating the impedance matrix of the multi-stacked on-chip PDN, which mainly consists of arbitrarily distributed TSVs and grid-type on-chip PDNs. First, a real stack-up structure of a multi-stacked on-chip PDN is separated into discrete components intentionally. Then the equivalent lumped circuit models of all discrete components are assembled into a whole to build the transmission matrix of the multi-stacked on-chip PDN through the relationship between the nodal voltage and the nodal current. Finally, the impedance matrix can be derived through the transmission matrix . In this paper, the coupling of the arbitrarily distributed TSVs and the distributional effect of the on-chip PDN are considered in the impedance matrix through the transmission matrix method (TMM). The proposed method replaces the simulation of the complex equivalent circuit model with the matrix calculation. It can accurately and quickly calculate the impedance of the multi-stacked on-chip PDN.

Keywords: Multi-stacked on-chip PDN, TSV array, Coupling, Transmission matrix method

1 Introduction

In recent years, with the rapid development of electronic terminals, electronic systems have developed towards higher speed, higher bandwidth, lower power consumption, and so on. Three-dimensional integrated circuits (3D ICs) are widely used for some unique advantages, such as shorter interconnection and heterogeneous integration[1]. But the problems such as signal integrity (SI), power integrity (PI), and electromagnetic interference (EMI) become more and more serious in the higher frequency systems. Simultaneous switching noise (SSN) often leads to unwanted noise in power distribution networks (PDNs), then the induced power supply fluctuation will cause problems with signal integrity in the system. A major challenge faced by 3D ICs is how to deliver clean power to the active circuits, especially on the topmost chip [2]. Fundamentally, PDN systems have a low value of the impedance in the frequency range of interest to effectively reduce noise. The low-frequency impedance is principally determined by off-chip components in 3D ICs, while the high-frequency impedance is determined by the multi-stacked on-chip structure concerned in this paper[3–5]. Through-silicon-vias (TSVs) penetrating the stacked chips act as key interconnect channels to connect stacked chips, and thus realize the circuit conduction as shown

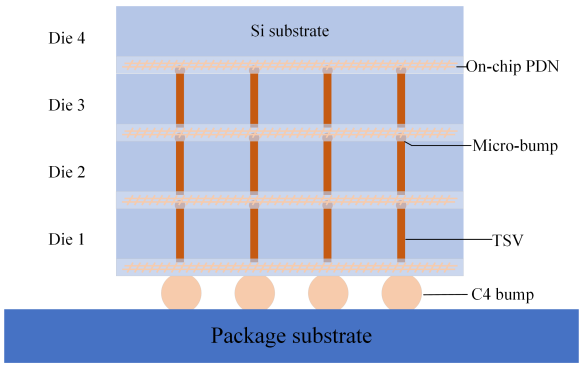


Fig. 1 A simple illustration of a stacked 3D IC including TSVs.

in figure 1 (Fig. 1). These chips may have different functions to implement a heterogeneous system. The power and ground TSVs respectively connect on-chip PDNs that consist of the multilayer power and ground grid metal into a whole as the important electrical pathways to supply the power source for active circuits.

A compact and accurate impedance modeling can help optimize power distribution networks during the early stages of design. The primary objective is to develop an accurate and quick model to predict the PDN impedance. On-chip PDN conditions such as the effective inductance and capacitance at the active circuit affected by the size of the PDN and the number and position of TSVs are very important to precisely evaluate the impedance of 3D stacked on-chip PDNs. As the frequency is closing to a higher value (GHz), even a small TSV inductance can produce several numbers of high impedance peaks induced by the parallel resonances of the TSV and on-chip PDN inductances and capacitances [6]. It will induce a larger noise near the frequency point of the peak impedance. The coupling between TSVs cannot be ignored which is affected by the number and distribution of TSVs. In 3D PDNs, a large number of TSVs are placed in the Si substrate. Multiple and randomly located ground TSVs may be shared by multiple power TSVs in the TSV array. In the previous analysis, a uniform distribution of power/ground TSVS (P/G TSVs) was assumed frequently. Although a uniform distribution was preferable to suppress the worst voltage drop in 3D PDNs, it may not be a practical design choice due to the area constraint. In some designs, TSVs are only assigned in the whitespace around circuit modules [7, 8]. Too many TSVs in the whitespace will increase the size of the die and may cancel out their benefits. So minimizing the number of TSVs is an important goal for the optimization of PDNs during the design flow. It brings difficulties to obtain and analyze 3D PDN impedance because there exists complicated electromagnetic coupling among TSVs. Knowing the effect of the number and assignment of P/G TSVs on the impedance in advance is helpful to minimize the number of TSVs at the beginning of the design.

A considerable CPU run time is required to analyze the complex multi-stacked on-chip PDN through finite element simulation software such as ANSYS HFSS. Many published studies have reported the impedance models of PDN systems rather than finite element simulation. For the plate-shaped PDN, the analytical methods are used to calculate the impedance such as the resonant cavity method [9], the imaging method [10], the transfer matrix method [11, 12], and so on. With the development of IC technology, a grid-type PDN is usually designed since the plate-shaped PDN is easy to peel off during the fabrication process. The segmentation method is the basic method to analyze complex PDN structures. Some researchers have built the equivalent circuit models for the 3D PDNs using the lumped circuit models of on-chip PDNs and TSVs to analyze the impedance of the PDNs by SPICE simulations[13–15] . There are many studies on the influence of the regular TSV array on the PDN impedance. In[14] , the proposed model of the P/G TSV array has a limitation in the assumption of uniform current magnitude distributions across all power and ground TSVs in the uniform distributed TSVs during the extraction of the partial TSV inductances. It leads to the inaccurate partial TSV inductances in a real multiply stacked PDN which has an uneven power distribution. In [16, 17], it uses a segmentation method to model the PDNs with multiply pairs of P/G TSVs. It considers the effects of P/G TSV pairs to estimate the impedance of the 3D stacked PDN. It no longer applied if TSV pairs are close to each other because there is greater coupling between them. And it is unsuitable for the arbitrarily distributed TSVs. There are two TSV design schemes namely the irregular TSV placement and the regular TSV placement for the design of 3D ICs [18]. For the

irregular TSV placement, the matrix-based calculation using a segmentation method can accelerate the calculation speed for the PDN impedance estimation and solve the complexity problem of building a SPICE circuit due to the coupling. In this paper, a matrix calculation method is proposed to solve the PDN impedance of multi-stacked chips based on TMM rather than SPICE simulation. The P/G TSVs in the TSV array can be uniformly distributed or arbitrarily distributed. The test ports of the model can be TSV connection ports or ports of any interested nodes on the on-chip PDN of every tier. The multi-stacked on-chip PDN impedance is calculated quickly and accurately by the proposed method . It shows the advantages of large savings in computer run time and flexibility and versatility in applications.

The paper is organized as follows. In Section 2, a typical multi-stacked on-chip PDN structure based on TSVs is given and a detailed derivation of the impedance matrix is presented. In Section 3, The impedance obtained by the proposed method for different TSV distributions is compared. The accuracy of the proposed method is verified with the results obtained from HFSS. Compared with the results of HFFS and other methods, it concludes that the proposed method is accurate and effective. The influence of several arbitrarily distributed TSVs on the multi-stacked on-chip PDN impedance is also compared and analyzed. Finally, there is a conclusion drawn in Section 4.

2 Modeling and analysis of the multi-stacked on-chip PDN impedance

A locally simplified multi-stacked on-chip PDN in stacked 3D ICs is shown in Fig. 2, where active layers are face-to-back (F2B) stacked. The grid-type PDN is usually used for the on-chip PDN because it is efficient when it comes to design with a limited area and it is not easy to peel off. The grid-type on-chip PDN is composed of orthogonal metal wires in two interconnection layers, where power wires and ground wires are routed alternately in the same interconnection layer with an identical pitch and connected to corresponding wires in the next interconnection layer by a large of micro-vias. The P/G TSV array in silicon substrate connects adjacent on-chip PDNs to achieve

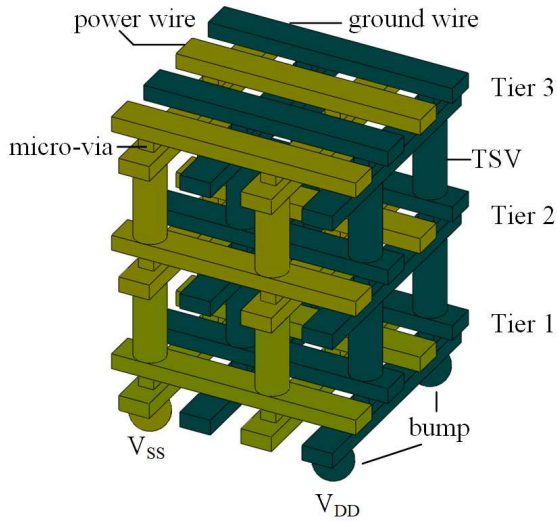


Fig. 2 A diagram of a locally simplified multi-stacked on-chip PDN

power delivery. In this paper, bumps are simplified as an extension of the TSV metal. The impedance matrix of the multi-stacked on-chip PDN can be derived by using separated P/G TSV array and on-chip PDN models through TMM.

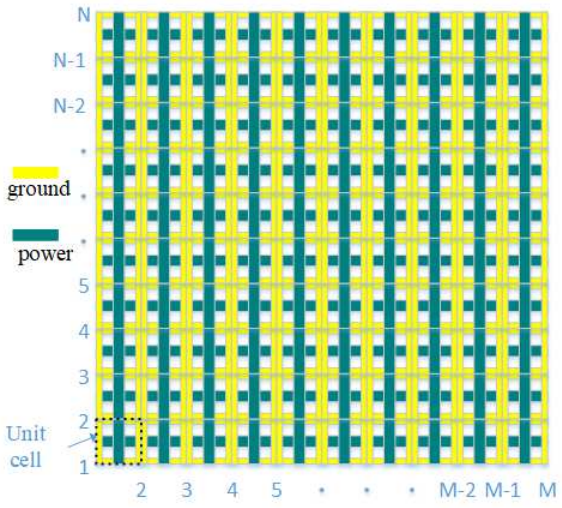
For an on-chip PDN model, a quasi-static solver can be applied if the dimension of a network is much less than one-tenth of the wavelength of interest (0.1λ). The grid-type on-chip PDN can be divided into a lot of periodic unit cells with a lumped element model for each cell. As shown in Fig. 3, the P/G grid is divided into $(N-1)\times(M-1)$ unit cells modeled with a distributed network of RLCG elements. The equivalent circuit of each grid unit cell consists of the resistance (R_u), inductance (L_u), conductance (G_u), and capacitance (C_u) which can be accurately calculated as (1), where L_p and L_w are the pitch and width of the metal line of the mesh grid. Parameters with subscripts of CMS and Micro represent parameters per unit length in the coplanar multistrip type transmission line and the conductor-backed coplanar multistrip type transmission line, respectively. More details of the calculating procedure are presented in[19].

$$R_u = (2L_p - L_w)R_{CMS} + L_w R_{Micro} \tag{1a}$$

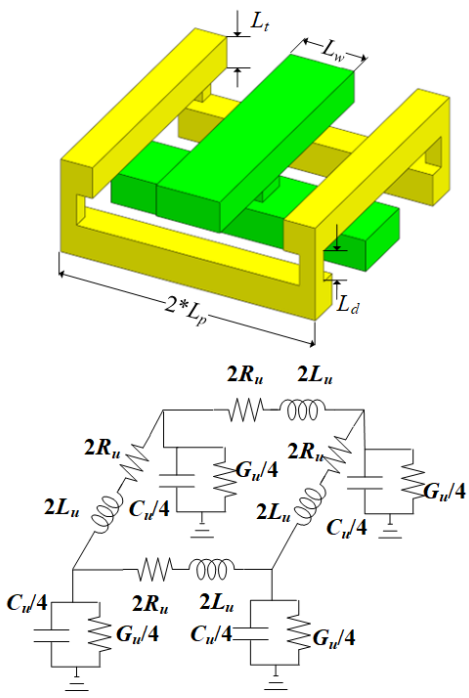
$$L_u = (2L_p - L_w)L_{CMS} + L_w L_{Micro} \tag{1b}$$

$$C_u = 2(2L_p - L_w)R_{CMS} + 2L_w R_{Micro} \tag{1c}$$

$$G_u = 2\pi f C_u \tan(\delta) \tag{1d}$$



(a)



(b)

Fig. 3 (a)The segmentation of a P/G grid (b)The unit cell with its equivalent circuit model

According to the relationship between the nodal voltage and the nodal current, the admittance matrix of the P/G grid ($Y_{P/Ggrid}$) in $N \times M$ nodes can be expressed as:

$$Y_{P/Ggrid} = \begin{bmatrix} Y_{11} & -Y_{12} & 0 & 0 & \cdots \\ -Y_{12} & Y_{22} & -Y_{23} & 0 & \cdots \\ 0 & -Y_{23} & Y_{33} & -Y_{34} & \cdots \\ \vdots & \vdots & \vdots & \ddots & \cdots \\ 0 & 0 & 0 & \cdots & Y_{MM} \end{bmatrix} \tag{2a}$$

$$Y_{11} = Y_{MM} = \frac{1}{2}Y_{22} = \cdots = \frac{1}{2}Y_{(M-1)(M-1)} = \begin{bmatrix} \frac{Y_P}{4} + \frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \cdots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_P}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} & \cdots & 0 & 0 \\ \vdots & \vdots & & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & -\frac{1}{2Z_s} & \frac{Y_P}{2} + \frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \cdots & 0 & -\frac{1}{2Z_s} & \frac{Y_P}{4} + \frac{1}{Z_s} \end{bmatrix} \tag{2b}$$

$$Y_{12} = Y_{23} = \cdots = Y_{(M-1)M} = \begin{bmatrix} \frac{1}{2Z_s} & & & & 0 \\ & \frac{1}{Z_s} & & & \\ & & \ddots & & \\ & & & \frac{1}{Z_s} & \\ 0 & & & & \frac{1}{2Z_s} \end{bmatrix} \tag{2c}$$

$$Z_s = R_u + j\omega L_u \tag{2d}$$

$$Y_P = j\omega C_u + G_u \tag{2e}$$

where Y_{ii} is the $N \times N$ self-admittance matrix of unit cells in the ith column and Y_{ij} is the $N \times N$ mutual-admittance matrix of unit cells between the ith column and the jth column. Z_S and Y_P are the impedance and admittance of a unit cell respectively. ω is the angular frequency.

As the size of the P/G grid increases, the number of the unit cells is increasing rapidly and the size of the admittance matrix of the P/G grid is bigger. The matrix calculation will become more complex and time-consuming. In the impedance calculation of a multi-port network, the input impedance of one port is obtained under the condition that the input currents of other uninterested ports are zero. To simplify the matrix and speed up the calculation, the matrix transformations are as follows. The relationship between voltages and currents in nodes of the grid metal is rewritten as:

$$\begin{bmatrix} I_a \\ I_b \end{bmatrix} = \begin{bmatrix} Y_{aa} & Y_{ab} \\ Y_{ba} & Y_{bb} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} \tag{3}$$

where I_a and V_a are the current and voltage vector in the interested nodes, I_b and V_b are the current

and voltage vector in the neglected nodes. For simplifying the admittance matrix of the P/G grid, the neglected nodes can be seen as open circuits and these nodal currents are limited to zero as (4). Then these nodes are deleted from the grid nodes, only remaining the interested nodes.

$$\begin{cases} I_a = (Y_{aa} - Y_{ab}{Y_{bb}}^{-1}Y_{ba})V_a \\ I_b = 0 \end{cases} \tag{4}$$

So the simplified admittance matric (Y_{sim}) in only interested nodes can be derived as:

$$Y_{sim} = Y_{aa} - Y_{ab}{Y_{bb}}^{-1}Y_{ba} \tag{5}$$

For a multi-stacked on-chip PDN, the P/G TSVs connecting adjacent on-chip PDNs can be randomly distributed. The nodes with power TSVs connecting are regarded as the nodes of interest to reduce the admittance matrix. The transmission matrix for a multi-port network can be derived in terms of the concerned nodal voltages and nodal currents and can be represented to relate the voltages and currents as:

$$\begin{bmatrix} V_{\text{in}} \\ I_{in} \end{bmatrix} = \begin{bmatrix} T_a & T_b \\ T_c & T_d \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{\text{out}} \end{bmatrix} \tag{6}$$

So the transmission matrix of a single on-chip PDN in the vertical direction (T_{PDN}) can be written in a simpler form as:

$$T_{PDN} = \begin{bmatrix} 1 & 0 \\ Y_{sim} & 1 \end{bmatrix} \tag{7}$$

It is not ignored that the electromagnetic coupling exists among the P/G TSV array as the frequency increases. To simplify the analysis of the coupling, the TSV array is considered as the multi-conductor interconnection and established the T-shaped network topology of the equivalent circuit model. Without a doubt, the equivalent circuit model becomes extremely complicated as the number of TSVs increases. This paper replaces the simulation of the complex equivalent circuit with using the matrix computation . All the values of lumped elements in the model of TSVs as depicted in Fig. 4 are given in the closed-form formulas as [20]. A ground TSV is arbitrarily set as the reference marked with *0* . The values of the self-inductance (L_{ii}) and mutual inductance (L_{ij})

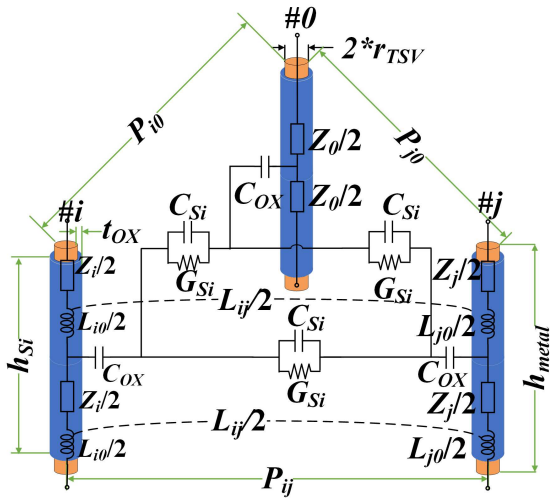


Fig. 4 The partial equivalent circuit model of a TSV array

of other TSV metals can be calculated as:

$$L_{ii} = \frac{\mu_0 h_{metal}}{\pi} \ln \frac{P_{i0}}{r_{TSV}} \tag{8a}$$

$$L_{ij} = \frac{\mu_0 h_{metal}}{2\pi} \ln \frac{P_{i0}P_{j0}}{P_{ij}r_{TSV}} \tag{8b}$$

where μ_0 is the permeability of the vacuum, P_{ij} is the distance between TSVs marked with i and TSV marked with j, h_{metal} is the length of the TSV metal, and r_{TSV} is the radius of the TSV. Considering N TSVs in which there are m power TSVs and n ground TSVs, all ground TSVs which are shorted represent the current return path. Based on the definition of the loop inductance with the size of m×m, it is rewritten as [21] :

$$\begin{cases} V_p = j\omega L_{eq} I_p \\ V_g = 0 \end{cases} \tag{9}$$

where V_p and I_p are the $m \times 1$ voltage and current vectors of m power TSVs respectively, V_g is the $n \times 1$ voltage vector of n ground TSVs. Then the effective loop inductance (L_{eq}) of the TSV array is yielded. When regarding each outer edge of the TSV as an equipotential surface, the equivalent inductance of Si substrate (L_{Si_eq}) in a homogeneous medium can be calculated as derived in (8) and (9). Next, simplify calculate the effective capacitance (C_{Si_eq}) and conductance (G_{Si_eq}) matrix of the silicon substrate as [22] :

$$C_{Si\_eq} = \mu_0 \varepsilon_0 \varepsilon_{Si} h_{Si}^2 {L_{\text{Si\_eq}}}^{-1} \tag{10a}$$

$$G_{Si\_eq} = \frac{\sigma_{Si}}{\varepsilon_0 \varepsilon_{Si}} C_{Si\_eq} \tag{10b}$$

The internal impedance (Z_{in}) for a TSV metal can be expressed as:

$$Z_{in} = \frac{h_{metal}\sqrt{j\omega\mu_0/\sigma_{TSV}}}{2\pi r_{TSV}} \frac{I_0(r_{TSV}\sqrt{j\omega\mu_0\sigma_{TSV}})}{I_1(r_{TSV}\sqrt{j\omega\mu_0\sigma_{TSV}})} \tag{11}$$

where I_0 and I_1 are the modified Bessel functions of order zero and one, respectively. The effective internal impedance matrix (Z_{in_eq}) of the TSV array can be obtained in the similar way to (9). The liner capacitance of a TSV can be expressed as:

$$C_{\mathrm{OX}} = \frac{2\pi\varepsilon_0\varepsilon_{Si}h_{Si}}{\ln\left(\frac{r_{TSV}+\mathrm{r}_{OX}}{r_{TSV}}\right)} \tag{12}$$

Next, Z_{in} is given by $1/j\omega C_{OX}$ to calculate the effective linear capacitance matrix (C_{OX_eq}) as also similar way to (9). The effective linear capacitance matrix of the TSV array is extracted from $Z_{in\_eq} = (j\omega C_{OX\_eq})^{-1}$. The impedance and admittance of the P/G TSV array can be expressed as:

$$Z_{TSV} = Z_{in\_eq} + j\omega L_{eq} \tag{13a}$$

$$Y_{TSV} = \left(\frac{1}{j\omega C_{OX\_eq}} + \frac{1}{G_{Si\_eq} + j\omega C_{Si\_eq}}\right)^{-1} \tag{13b}$$

The transmission matrix of the TSV array (T_{TSV}) can be derived as:

$$T_{TSV} = \begin{bmatrix} 1 & \frac{Z_{TSV}}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{TSV} & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{Z_{TSV}}{2} \\ 0 & 1 \end{bmatrix} \tag{14}$$

Finally, the separated on-chip PDNs and TSV arrays are assembled into a whole. According to the cascade of the multi-port network as shown in Fig. 5, the transmission matrix of the multi-stacked on-chip PDN combining multiple on-chip PDNs and TSV arrays (T_{total_n}) can be expressed as:

$$\begin{aligned} T_{total\_n} =& T_{PDN\_n} \cdot T_{TSV\_n,n-1} \cdot \cdots \\ & \cdot T_{PDN\_2} \cdot T_{TSV\_2,1} \cdot T_{PDN\_1} \end{aligned} \tag{15}$$

where T_{PDN_n} is the transmission matrix of the on-chip PDN of tier n, $T_{TSV\_n,n-1}$ is the transmission matrix of the TSV array between tier n and tier n-1. The impedance matrix of the multi-stacked on-chip PDN (Z_{total_n}) can be derived from T_{total_n} as:

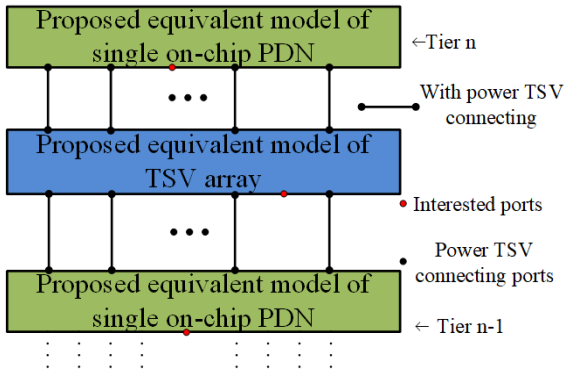


Fig. 5 The configuration of a multi-stacked on-chip PDN transmission modeling

$$Z_{total\_n} = \begin{bmatrix} T_{total\_n,a}T_{total\_n,c}^{-1} & T_{total\_n,c}^{-1} \\ T_{total\_n,c}^{-1} & T_{total\_n,c}^{-1}T_{total\_n,d} \end{bmatrix} \tag{16}$$

The impedance matrix describes the voltage-current correlation over the connection ports of the PDN at different frequencies. The coupling effect between TSVs through matrix calculation is considered in the arbitrary distributed P/G TSVs. For the impedance of the ports of any interested nodes on the on-chip PDN of every tier, it can be derived from the Z-matrix transformation of the black box model as shown in Fig. 6. α segment is expressed as a single on-chip PDN where interested ports (p) are. β segment is expressed as the remaining part of the multi-stacked on-chip PDN. The interconnection between them is replaced by

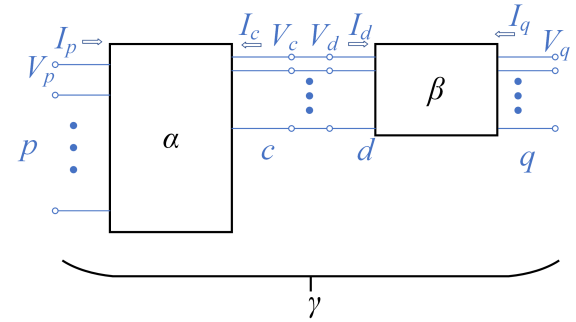


Fig. 6 The illustration of a black box model

the interconnected ports denoted c-ports on the α segment and d-ports on the β segment. p and q ports are the concerned ports of the α and β segments. The Z-matrices of α, β, and γ segments are respectively partitioned into submatrices corresponding to the interested and connected ports as:

$$Z_\alpha = \begin{bmatrix} Z_{pp\alpha} & Z_{pc} \\ Z_{cp} & Z_{cc} \end{bmatrix} \tag{17a}$$

$$Z_\beta = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq\beta} \end{bmatrix} \tag{17b}$$

$$Z_\gamma = \begin{bmatrix} Z_{pp\gamma} & Z_{pq} \\ Z_{qp} & Z_{qq\gamma} \end{bmatrix} \tag{17c}$$

Z_α and Z_β can be replaced respectively by different Z_{total_n} due to different segments. According to the continuity of the voltage and current on ports c and d, Z_γ can be calculated as:

$$Z_\gamma = \begin{bmatrix} Z_{pp\alpha} - Z_{pc}Z'_{dp} & Z_{pc}Z'_{dq} \\ Z_{qd}Z'_{dp} & Z_{qq\beta} - Z_{qd}Z'_{dq} \end{bmatrix} \tag{18}$$

where $Z'_{dp} = [Z_{cc} + Z_{dd}]^{-1} Z_{cp}$ and $Z'_{dq} = [Z_{cc} + Z_{dd}]^{-1} Z_{dq}$.

3 Validation and analysis of the proposed method

To verify the accuracy of the proposed method of the impedance estimation in the TSV-based multi-stacked on-chip PDN structure, a double-stacked grid-type on-chip PDN is constructed and its parameter description is listed in table 1. It has a horizontal size of 1 mm× 1 mm. The ordinary cylindrical TSVs filled with copper are applied in the TSV array. Designers need to arrange these TSVs properly to meet signal integrity, power integrity, and heat dissipation requirement. Fig. 7 shows two different TSV assignments. For a regular TSV distribution, P/G TSVs are uniformly distributed on the nodes with an identical pitch. For an arbitrary TSV distribution, P/G TSVs are only assigned in the whitespace around the circuit modules. Therefore P/G TSVs can be arranged in any position of the substrate that is dependent on the distribution of the circuit modules. Multiple and randomly located ground TSVs can be shared by multiple power TSVs. Without good planning and optimization, the over-design P/G network may create congestion problems for the later signal routing resources that are over-used. In the constructed structures, the regular TSV distributions are shown in Fig. 8, which includes the different number of TSV pairs and the uniform TSV distributions with the different scales of the TSV array. The proposed model is used to calculate the impedance of which the result is compared with the full-wave method and previous models. Due to the difficulty in the fabrication of complete multi-stacked on-chip PDNs, A frequency-domain simulation to extract Z-parameters is conducted ranging from 0.1GHz to 40 GHz with a 3D electromagnetic (EM) solver, ANSYS HFSS to verify the accuracy of the proposed method. Lumped ports

Table 1 The model parameters and its values

Symbol	Parameter description	Value
L_w	Width of the metal line	10 μm
L_p	Pitch of the metal line	50 μm
L_t	Thickness of the metal line	1 μm
L_d	Vertical distance between the metal layers	0.6 μm
r_{TSV}	Radius of the TSV metal	5 μm
h_{Si}	Height of the Si substrate	50 μm
h_{metal}	Length of the TSV metal	60 μm
t_{OX}	Thickness of the oxide liner	0.2 μm
p_{TSV}	Pitch between power and ground TSVs	-
σ_{TSV}	Conductivity of the TSV metal	$5.8\times10^7 S/m$
σ_{Si}	Conductivity of silicon	10 S/m
ϵ_0	Permittivity of vacuum	$8.85 \times 10^{-12} F/m$
ϵ_{Si}	Permittivity of silicon	11.9
ϵ_{OX}	Permittivity of the oxide liner	4
μ_0	permeability of vacuum	$4\pi \times 10^{-7}$ m

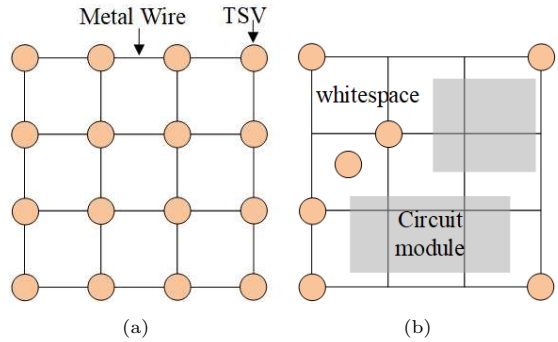


Fig. 7 The configurations of two different TSV assignments. (a) A regular distribution: TSVs are placed on each node (b) An arbitrary distribution: TSVs are only placed in the whitespace

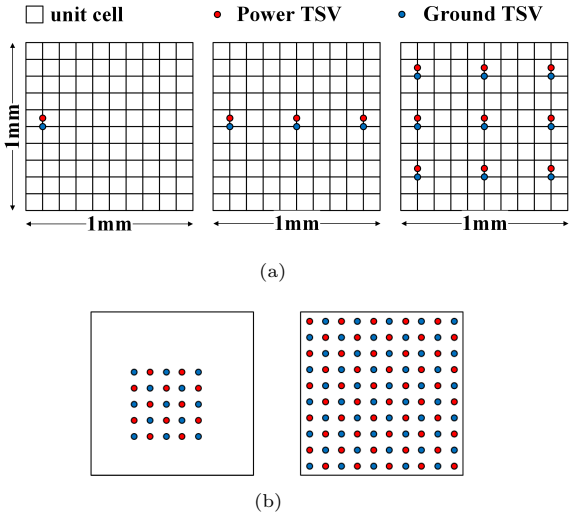


Fig. 8 PDNs with several different TSV distributions in the benchmark model. (a) One, three, and nine pairs of P/G TSVs (b) The uniform distributed TSVs in the arrays with 25 TSVs and 100 TSVs

for the analysis of the PDN input impedance are located on the topmost on-chip PDN.

As seen in Fig. 9, the PDN impedance curves have similar characteristics which mainly have three resonant frequencies (f_1, f_2, and f_3) below 20GHz. These frequencies are caused by the series and parallel resonances of the equivalent capacitance of the P/G grid ($C_{P/Ggrid}$), the equivalent inductance of the P/G grid ($L_{P/Ggrid}$), and the equivalent inductance of the TSV array (L_{TSV}). As the number of TSVs increases, f_2 moves to a higher frequency and it is eliminated if the number of TSVs is large enough. In this situation, f_3 is equal to f_1. So the deviation from the resonance frequency of the HFSS model such as f_1 is compared to verify the accuracy of the proposed method. The results of the proposed method show good agreement with the results of the HFSS. Not only the PDN impedance but also the simulation time for the three methods are compared as shown in table 2. The simulation is performed on a computer with 16 cores (at 3.0 GHz) and 256 GB of RAM. The proposed model leads to a larger saving in CPU run time than using HFSS simulation. It only takes a tiny computing time compared with the full-wave method. Therefore, it is concluded that the proposed model is accurate and efficient to estimate the impedance of the multi-stacked on-chip PDN with the regular TSVs connecting. Comparatively, the benefit of

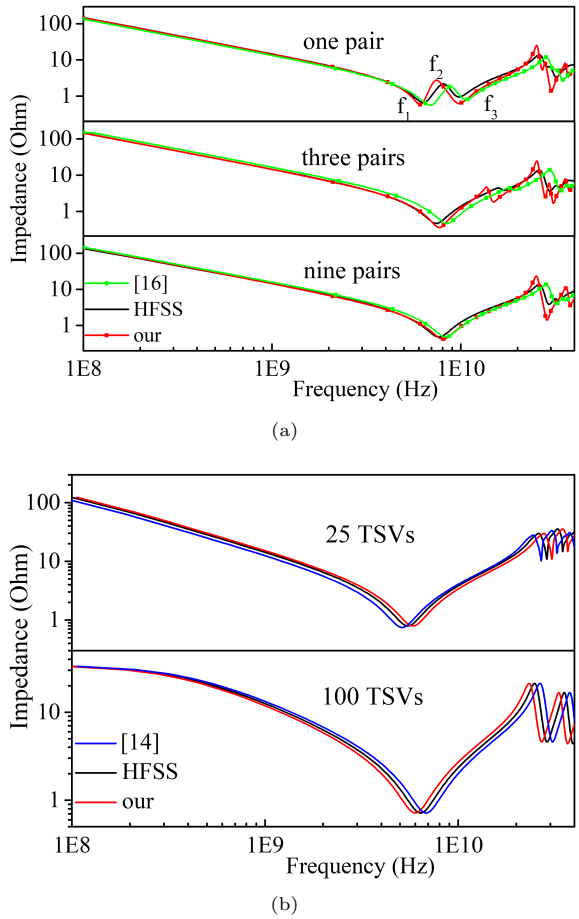


Fig. 9 The comparison of three methods for PDN impedances with regular TSV distributions. (a) PDNs with different pairs of P/G TSVs (b) PDNs with different scales of the TSV array

the proposed method is that it can deal with the complicated TSV array including not only the regularly distributed TSVs but also the arbitrarily distributed TSVs in 3D PDNs. The arbitrarily distributions of TSVs are constructed as shown in Fig. 10. The whitespace around the circuit models are respectively across, peripheral, and combined distribution in the substrate, and TSVs are only assigned in the whitespace. To enable power TSVs to be connected directly to the power wires without the need for the extra redistribution layer, power TSVs are placed designedly at the location of the intersection of the two-layer of the power metal wires so that it can reduce the wiring area. Ground TSVs are placed designedly at the location of the intersection of the two-layer of the ground metal wires. The impedances of three test

Table 2 Comparison of results with several kinds of different methods

Cases in Fig. 8		Methods	Deviation of f_1	CPU run time
a	1	HFSS model	-	1h23min30s
	2			1h57min01s
	3			2h29min35s
	1	The proposed model	4.2%	3.03s
	2		6.5%	8.57s
	3		5.9%	10.06s
	1	Model in [16]	11.1%	1min12s
	2		13.8%	1min18s
	3		12.6%	2min05s
b	1	HFSS model	-	2h39min47s
	2			2h51min36s
	1	The proposed model	6.2%	13.47s
	2		5.9%	15.91s
	1	Model in [14]	10.9%	40.96s
	2		9.5%	2min13s

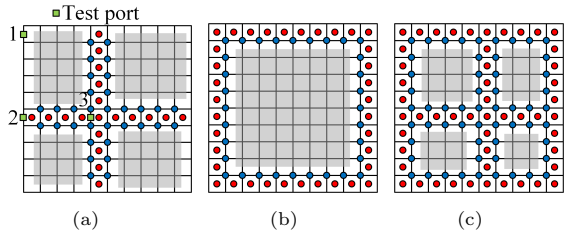


Fig. 10 Three kinds of arbitrary distributions of P/G TSVs. (a) cross (b) peripheral (c) combined

ports marked with port *1*, *2*, and *3* are calculated and qualitatively analyzed. The results are shown in Fig. 11. In the range of the lower frequency, the impedance shows capacitive which is determined by the $C_{P/G}$ grid and the equivalent capacitance of the TSV array (C_{TSV}). As the number of TSVs increases, the total capacitance is increasing so that impedance is decreasing. As the frequency goes up, the impedance shows inductive which is determined by the $L_{P/Ggrid}$ since the L_{TSV} decreases to a very small value that can be neglected if the number of TSVs is large enough.

The impedance of the PDN should stay at a low level to ensure power integrity. Aspects that the influence of the impedance for the multi-stacked on-chip PDN and methods to decrease the impedance are studied. Fig. 12 shows several kinds of low density and arbitrary P/G TSVs connecting between tier n and n-1. The impacts of the number of TSVs on the impedance of the

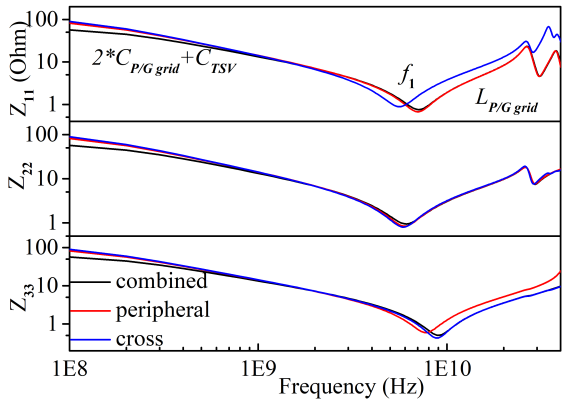


Fig. 11 The comparison of three kinds of arbitrary distributions of P/G TSVs for the PDN impedance

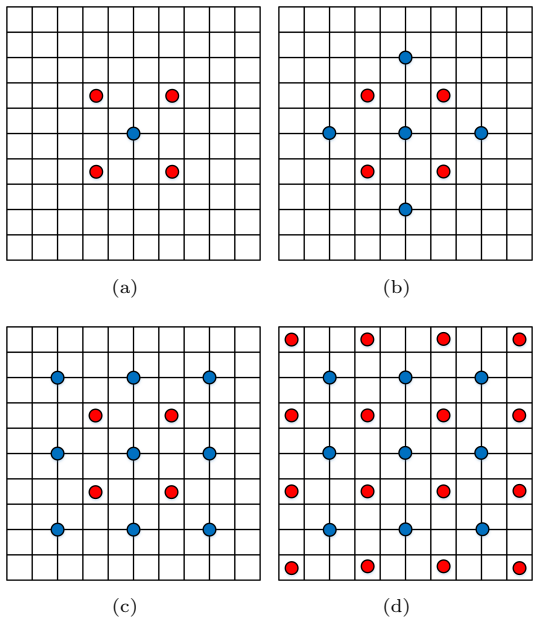


Fig. 12 Different number of TSVs connecting between tier n and n-1. (a) 4P1G (b) 4P5G (c) 4P9G (d) 9P16G

multi-stacked on-chip PDN are explored. Fig. 13 compares four input impedances at the center of the toper tier for the double-stacked on-chip PDNs with four kinds of arbitrary TSV array connecting as shown in Fig. 12. Four PDN impedance curves have similar characteristics. Careful observation reveals that the difference in the input impedance of the lower frequency range is slight. The reason is that the impedance of the lower frequency range is caused by the total capacitance which consists of C_{TSV} and two times $C_{P/Ggrid}$. As the number of TSVs increases, the capacitance of TSVs

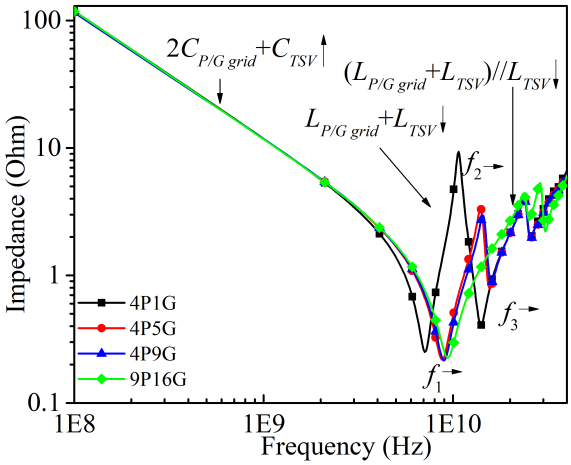


Fig. 13 The comparison of the input impedance at the center of the toper tier for the double-stacked on-chip PNDs with four kinds of TSV arrays connecting respectively as shown in Fig. 12

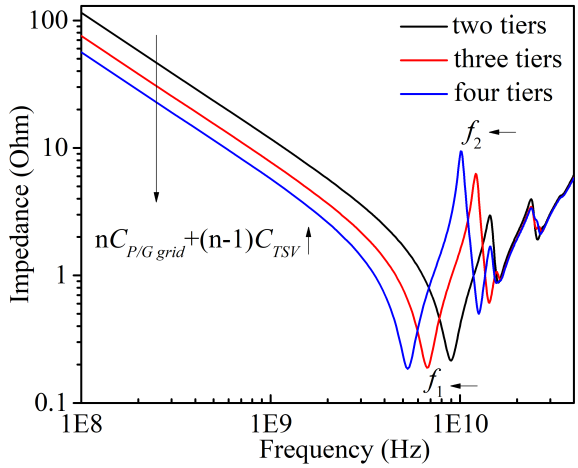


Fig. 14 The comparison of the input PDN impedance at the center of the topmost layer depended on the different number of the tiers

is gradually larger and the total capacitance is only larger slightly but the effective inductance of the power TSVs is smaller. The resonance frequency f_1 goes to the higher frequency range with an increased ground TSV number compared to case a with b and c, which can affect the relative distance between the frequency of the impedance peak and the clock frequency, but the impact is getting smaller with more ground TSVs compared case b with c as it is shown that the impedance curves tend to be approximately the same. Therefore, it needs to add more power TSVs as shown in case d if higher f_1 and f_2 are wanted, and f_2 will be eliminated because of the enough TSVs.

To determine the effects of the number of stacked tiers on the impedance , it varies from two to four. Fig. 14 shows the comparison of three input impedances at the center of the topmost tier for the multi-stacked on-chip PDNs with the TSV array connecting as shown in case c in Fig. 12. The P/G grid and TSV capacitances increase with the number of stacked tiers increasing so that the impedance below the series resonant frequency (f_1) is decreased. f_1 moves to a lower frequency range, but the lowest parallel resonance frequency (f_2) of them moves to the lower frequency range with the higher PDN impedance peak. As a result, it needs to pay more attention to designing the future heterogeneous 3D IC because a higher-stacked on-chip PDN is more difficult to keep minimizing the low PDN impedance.

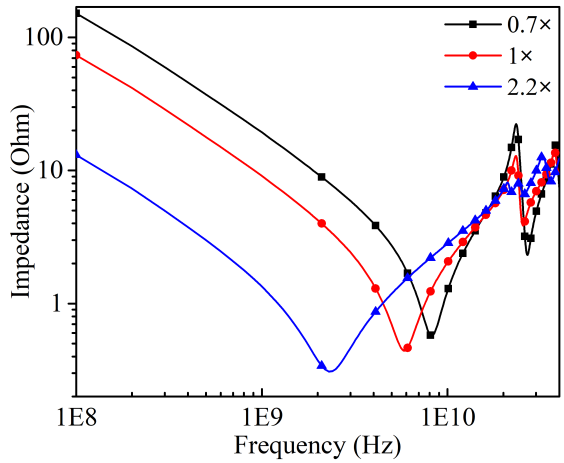


Fig. 15 The comparison of the input PDN impedance at the center of the topmost layer depended on the different size of the four-stacked on-chip PDN

To determine the effect of the size of the stacked on-chip PDN on the impedance, the scales of the sizes of four-stacked on-chip PDNs are varied from 0.7 to 2.2. The uniform density distribution of TSVs is adopted. Fig. 15 shows the comparison of three input impedances at the center of the topmost tier for the four-stacked on-chip PDNs with the TSV array connecting as shown in case d in Fig. 12. When the scale of the stacked on-chip PDN is increased, the impedance below series resonant frequency (f_1) is decreased because the P/G grid and TSV capacitances increase. f_1

moves to the lower frequency range. The parallel resonance becomes less and less obvious in the high-frequency range.

4 Conclusion

The proposed model can reflect the various arrangements of the P/G TSVs for estimating the multi-stacked on-chip PDN impedance in 3D ICs. The separated power/ground grid units of the on-chip PDN are modeled as the transmission line using the frequency-dependent RLGC parameters and the TSV array is modeled using the theory of multiconductor transmission lines. Then the impedance of the multi-stacked on-chip PDN is derived by the transmission matrix method through the cascade. It replaces the simulation of the complex SPICE circuit in which there exits lots of coupling with the matrix calculation method. It is computationally efficient and leads to a large saving in CPU run time. For the complicated structure, it is also accurate and scalable to analyze the impedance in the pre-design stage and help designers achieve a 3D PDN quickly and reliably.

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References

[1] Lau, J.H.: Overview and Outlook of Three-Dimensional Integrated Circuit Packaging, Three-Dimensional Si Integration, and Three-Dimensional Integrated Circuit Integration. Journal of Electronic Packaging **136**(4) (2014). https://doi.org/10.1115/1.4028629

[2] Swaminathan, M., Engin, A.E.: Power integrity modeling and design for semiconductors and systems. Pearson Schweiz Ag (2008)

[3] Swaminathan, M., Kim, J., Novak, I., Libous, J.P.: Power distribution networks for system-on-package: status and challenges. IEEE Transactions on Advanced Packaging **27**(2), 286–300 (2004). https://doi.org/10.1109/TADVP.2004.831897

[4] Xu, J., Bai, S., Nalla, K., Sapozhnikov, M., Drewniak, J.L., Hwang, C., Fan, J.: Power delivery network optimization approach using an innovative hybrid target impedance. In: 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal Power Integrity (EMC+SIPI), pp. 211–216 (2019). https://doi.org/10.1109/ISEMC.2019.8825309

[5] Kim, J., Lee, W., Shim, Y., Shim, J., Kim, K., Pak, J.S., Kim, J.: Chip-package hierarchical power distribution network modeling and analysis based on a segmentation method. IEEE Transactions on Advanced Packaging **33**(3), 647–659 (2010). https://doi.org/10.1109/TADVP.2010.2043673

[6] Pak, J.S., Kim, J., Cho, J., Lee, J., Lee, H., Park, K., Kim, J.: On-chip pdn design effects on 3d stacked on-chip pdn impedance based on tsv interconnection. In: 2010 IEEE Electrical Design of Advanced Package Systems Symposium, pp. 1–4 (2010). https://doi.org/10.1109/EDAPS.2010.5682994

[7] Knechtel, J., Markov, I.L., Lienig, J., Thiele, M.: Multiobjective optimization of deadspace, a critical resource for 3d-ic integration. In: 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 705–712 (2012)

[8] Wu, Q., Zhang, T.: Design techniques to facilitate processor power delivery in 3-d processor-dram integrated systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems **19**(9), 1655–1666 (2011). https://doi.org/10.1109/TVLSI.2010.2053565

[9] Na, N., Swaminathan, M.: Modeling and transient simulation of planes in electronic packages for ghz systems. In: IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No.99TH8412), pp. 149–152 (1999). https://doi.org/10.1109/EPEP.1999.819214

[10] Yang, D.-C., Wei, X.-C.: Impedance calculation of power and ground planes by using

imaging methods. In: 2012 Asia-Pacific Symposium on Electromagnetic Compatibility, pp. 37–40 (2012). https://doi.org/10.1109/APEMC.2012.6237851

[11] Kim, J.-H., Swaminathan, M.: Modeling of irregular shaped power distribution planes using transmission matrix method. IEEE Transactions on Advanced Packaging **24**(3), 334–346 (2001). https://doi.org/10.1109/6040.938301

[12] Kim, J.-H., Matoglu, E., Choi, J., Swaminathan, M.: Modeling of multi-layered power distribution planes including via effects using transmission matrix method. In: Proceedings of ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15h International Conference on VLSI Design, pp. 59–64 (2002). https://doi.org/10.1109/ASPDAC.2002.994886

[13] He, H., Lu, J.J.-Q.: Modeling and analysis of pdn impedance and switching noise in tsv-based 3-d integration. IEEE Transactions on Electron Devices **62**(4), 1241–1247 (2015). https://doi.org/10.1109/TED.2015.2396914

[14] Pak, J.S., Kim, J., Cho, J., Kim, K., Song, T., Ahn, S., Lee, J., Lee, H., Park, K., Kim, J.: Pdn impedance modeling and analysis of 3d tsv ic by using proposed p/g tsv array model based on separated p/g tsv and chip-pdn models. IEEE Transactions on Components, Packaging and Manufacturing Technology **1**(2), 208–219 (2011). https://doi.org/10.1109/TCPMT.2010.2101771

[15] Kim, K., Lee, W., Kim, J., Song, T., Kim, J., Pak, J.S., Kim, J., Lee, H., Kwon, Y., Park, K.: Analysis of power distribution network in tsv-based 3d-ic. In: 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems, pp. 177–180 (2010). https://doi.org/10.1109/EPEPS.2010.5642575

[16] Kim, K., Yook, J.M., Kim, J., Kim, H., Lee, J., Park, K., Kim, J.: Interposer power distribution network (pdn) modeling using a segmentation method for 3-d ics with tsvs. IEEE Transactions on Components, Packaging and Manufacturing Technology **3**(11), 1891–1906 (2013). https://doi.org/10.1109/TCPMT.2013.2276050

[17] Kim, K., Hwang, C., Koo, K., Cho, J., Kim, H., Kim, J., Lee, J., Lee, H.-D., Park, K.-W., Pak, J.S.: Modeling and analysis of a power distribution network in tsv-based 3-d memory ic including p/g tsvs, on-chip decoupling capacitors, and silicon substrate effects. IEEE Transactions on Components, Packaging and Manufacturing Technology **2**(12), 2057–2070 (2012). https://doi.org/10.1109/TCPMT.2012.2214482

[18] SungKyuLim, SungKyuLim, SungKyuLim, SungKyuLim: Regular versus irregular tsv placement for 3d ic. Springer New York (2013). https://doi.org/10.1007/978-1-4419-9542-1$_$1

[19] Hwang, C.S., Kim, K.Y., Pak, J.S., Kim, J.H.: Modeling of an on-chip power/ground meshed plane using frequency dependent parameters. Journal of Electromagnetic Engineering & Science **11**(11), 192–200 (2011). https://doi.org/10.5515/JKIEES.2011.11.3.192

[20] Qu, C., Ding, R., Liu, X., Zhu, Z.: Modeling and optimization of multiground tsvs for signals shield in 3-d ics. IEEE Transactions on Electromagnetic Compatibility **59**(2), 461–467 (2017). https://doi.org/10.1109/TEMC.2016.2608981

[21] Paul, C.R.: Analysis of Multiconductor Transmission Lines. John Wiley & Sons, New York (2007)

[22] Engin, A.E., Narasimhan, S.R.: Modeling of crosstalk in through silicon vias. IEEE Transactions on Electromagnetic Compatibility **55**(1), 149–158 (2013). https://doi.org/10.1109/TEMC.2012.2206816