# Impedance spectroscopy of thin-film CdTe/CdS solar cells under varied illumination

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The electrical properties of CdTe/CdS solar cells grown by metal organic chemical vapor deposition were investigated by a technique of impedance measurements under varied intensity of AM1.5 illumination. A generalized impedance model was developed and applied to a series of CdTe/CdS cells with variations in structure and doping. The light measurements were compared to the conventional ac measurements in dark under varied dc bias, using the same methodology for equivalent circuit analysis in both cases. Detailed information on the properties of the device structure was obtained, including the properties of the main *p*-*n* junction under light, minority carrier lifetime, back contact, as well as the effect of the blocking ZnO layer incorporated between the transparent conductor and CdS layers. In particular, the comparison between samples with different chemical concentrations of As has shown that the total device impedance and the series resistance are strongly increased at lower As densities, resulting in the lower collection current and efficiencies. At the same time the minority carrier lifetime was found to be one order of magnitude larger for the lowest value of As density, when compared to the optimized devices. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3204484]

## I. INTRODUCTION

It has been recognized recently that impedance spectroscopy methods (used for analysis of electrical properties of a wide range of physical systems), are particularly suitable for in-depth studies of thin-film polycrystalline solar cells.[1] The power of impedance analysis in this case lies in its ability to separate contributions from different layers or regions of a solar cell structure.[2] The method was shown to provide detailed assessment of the device properties, as well as of the possible impact on the overall performance, from each of the device regions individually.

Impedance measurements of thin-film solid state solar cells is an increasingly popular technique, however, the majority of such experiments to date have been carried out almost exclusively under dark conditions.[3–6] On one hand this makes the measurements and interpretation of the spectra easier in some cases. Yet on the other, it also has a strong disadvantage of not providing the direct information on a solar cell under its operating condition. In particular, under illumination the distribution of electric fields, as well as the electrical states of defects and impurities (affecting the carrier transport and recombination) is significantly different from those in the dark.

In this work we apply a recently refined technique of impedance spectroscopy carried out under varied intensity of illumination, and compare it with the dark impedance measurements for the case of polycrystalline thin-film solar cells. The light technique was successfully applied before to dye-sensitized solar cell systems,[7] and more recently to the cells based on microcrystalline and amorphous silicon.[2] Here a series of thin-film devices based on the CdTe/CdS *p*-*n* junction and grown by metal organic chemical vapor deposition[8,9] (MOCVD) is being investigated. The study is focused on the critical aspects of device structure, such as (i) the effect from incorporation of a thin barrier layer on device electrical properties and performance; (ii) the change in properties induced by a variation of the doping level in the *p*-type CdTe absorber; (iii) the comparison of impedance characteristics between the samples with and without an extra highly doped CdTe:As layer next to the metal back contact.

Undoped, low conductivity barrier layers—positioned between the transparent conducting oxide (TCO) and window layers—have been recognized over the recent years as an important element of a thin-film cell, contributing to high device efficiencies.[10] The exact effects of such a layer on the internal electrical properties of a solar cell, however, have not yet been fully understood. In this work we carried out the comparison of impedance characteristics from samples with and without a ZnO barrier layer. Also, the comparative approach has been taken for the study of devices *p*-doped by arsenic at different levels, both in the absorber and contact regions.

## II. SAMPLES AND EXPERIMENTAL TECHNIQUE

Four CdTe/CdS samples grown and processed by a MOCVD method have been investigated in this work.

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TABLE I. Device parameters for the four studied solar cells. $N_{As}$ is the chemical concentration of As in the CdTe layer, $\eta$—cell efficiency, $V_{oc}$—open circuit voltage, $J_{sc}$—short circuit current, and FF—fill factor.

| Samples | $N_{As}$ ($cm^{-3}$) | ZnO | Back contact | $\eta$ (%) | $V_{oc}$ (V) | $J_{sc}$ ($mA/cm^{-2}$) | FF (%) |
|---|---|---|---|---|---|---|---|
| I | $2\times10^{18}$ | Yes | Au/CdTe | 8 | 0.6 | 20.5 | 61 |
| II | $2\times10^{18}$ | No | Au/CdTe | 6.5 | 0.58 | 18.3 | 57 |
| III | $1\times10^{17}$ | No | Au/CdTe | 1.5 | 0.5 | 4.4 | 65 |
| IV | $2\times10^{18}$ | Yes | Au/As$^+$doped/CdTe | 10.5 | 0.72 | 21.3 | 70 |

Samples I and II have an identical and optimized level of doping by As, while differ in structure due to the presence of a ZnO barrier layer in sample I. Sample III has the structure identical to that of sample II, but the level of As doping is considerably smaller, resulting in lower efficiency.[8,9] Sample IV has the same structure and doping as sample I, but it also contains an extra layer of highly doped CdTe:As at the back contact, which allows for a considerable improvement in efficiency. The details of the employed MOCVD growth procedure can be found in Refs. 8 and 9.

The devices consist of commercial indium tin oxide glass, 60 nm of ZnO (for samples I and IV), followed by 240 nm of CdS, and further by 4 $\mu$m of CdTe doped with As. The MOCVD process was concluded by the growth of a 600 nm thick $CdCl_2$ layer, followed by a 10 min anneal at 400 °C under hydrogen.[11] To create a Te-rich layer at the back surface a conventional bromine-methanol etching step (Br–MeOH, with 0.1% Br) was applied to the CdTe surface for 10 s prior to the evaporation of gold electrodes (samples I–III). In case of sample IV no back-surface etching was applied. However, the concentration of As was raised to $2\times10^{19}$ $cm^{-3}$ for the last stage of the CdTe growth, thus forming a highly doped $p$-layer of $\sim$250 nm.

The solar cell parameters obtained by the standard current-voltage measurements under AM1.5 illumination, as well as the parameters of the structure for each device, are summarized in Table I.

The impedance measurements were carried out on Solartron 1260 impedance analyzer, in the frequency range from 0.1 Hz to 300 kHz. Each measurement was done applying a 10 mV ac sinusoidal signal over the constant applied bias. The light source was a 300 W Oriel 81160 solar simulator, with the illumination intensity being varied using neutral density filters. All light measurements have been carried out applying a bias equal to the $V_{oc}$ obtained at each illumination, i.e., under zero current condition. The dark measurements were carried out at a constant dc bias in the range of voltages similar to that for $V_{oc}$.

## III. EXPERIMENTAL RESULTS AND ANALYSIS

### A. Impedance spectra and equivalent circuit

Impedance characteristics under light conditions are studied first for the samples with optimized doping level and a basic Au/CdTe back-contact structure. Figure 1 shows examples of impedance spectra of sample I, and Fig. 2—spectra of sample II, measured at the light intensities from 1 sun (100 $mW/cm^2$) to $10^{-4}$ sun, at the room temperature. The complex spectra are qualitatively similar for both samples, consisting of more than one arc, as seen on the $Z''$-$Z'$ plots in Figs. 1(a)–1(d) and Figs. 2(a) and 2(b).

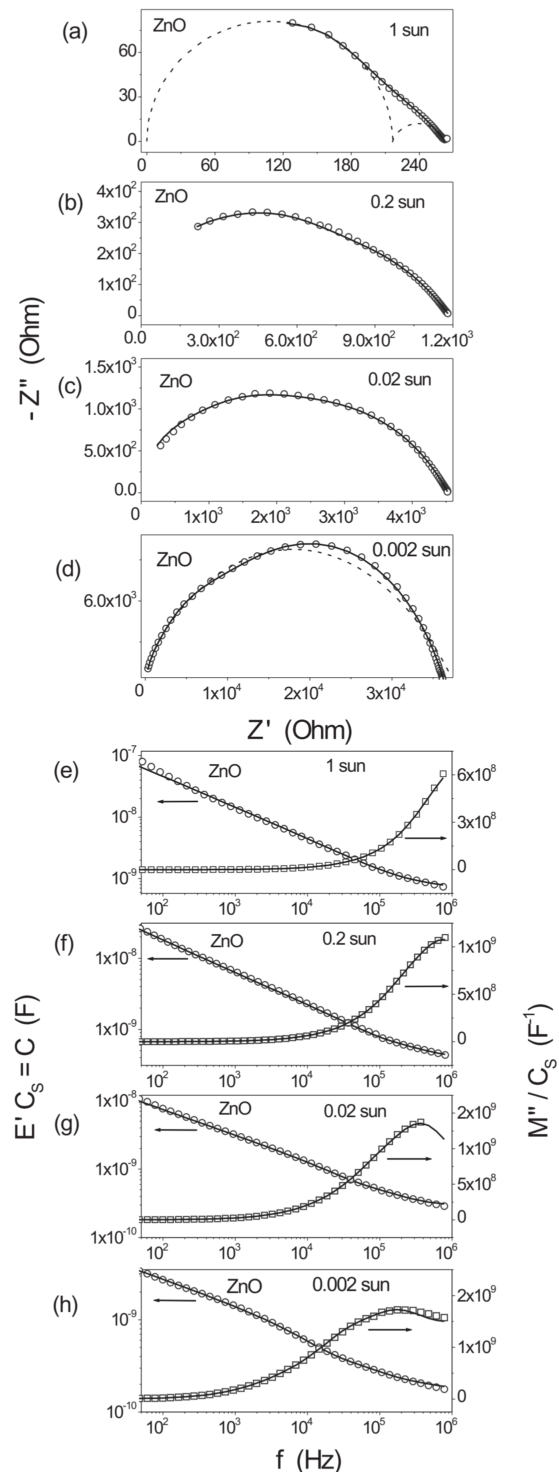


FIG. 1. [(a)–(d)] Impedance spectra on a $Z''$-$Z'$ plot for sample I under varied light intensity in the range from 1 to 0.002 sun. [(e)–(h)] The same impedance data represented as real part of dielectric permittivity $E'$ and imaginary part of electric modulus $M''$ vs frequency. In all plots: solid lines—fit to the model in Fig. 3(b). Dashed lines in (a) depict spectrum from the two-section circuit of Fig. 3(a). The dashed line in (d) represents the fit done with the CPE, but without the third section of the circuit in Fig. 3(b).

The right-hand side cutoff of the spectrum on $Z'$ axis corresponds to the total resistance (low frequency impedance) of a device, $R_t$. Surprisingly, comparison shows that at

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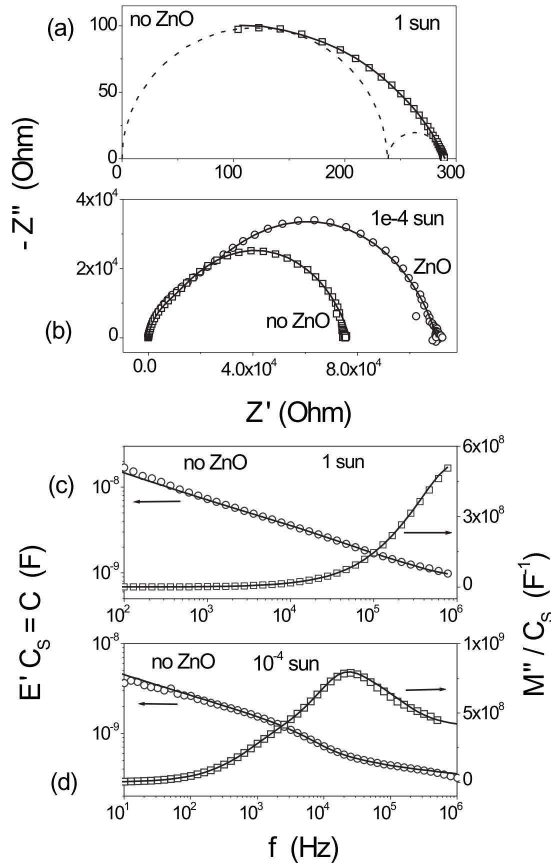


FIG. 2. (a) Impedance spectra on a $Z''$-$Z'$ plot for sample II under light intensity of 1 sun. (b) $Z''$-$Z'$ data in near-dark condition for sample I and II (light intensity of $10^{-4}$ sun). The spectra coincide in the high frequency part (at low $Z'$). [(c) and (d)] The same impedance data for sample II as in (a) and (b), represented as $E'(f)$ and $M''(f)$. In all plots: solid lines—fit to the model in Fig. 3(b). Dashed lines in (a) depict spectrum from two-section circuit of Fig. 3(a).

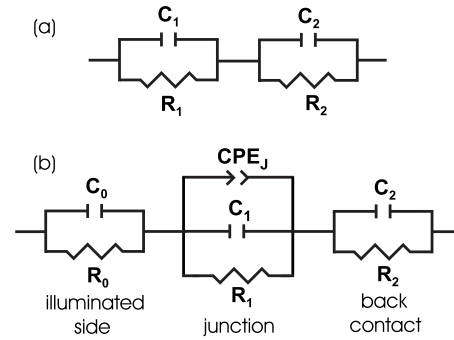


FIG. 3. (a) Basic equivalent circuit of a *p*-*n* type solar cell with a Schottky barrier at the back contact. (b) Refined equivalent circuit which was found to describe impedance data of the studied CdTe/CdS samples under various illumination conditions.

larger light intensities the $R_t$ values are very close for both of the samples [see Figs. 1(a) and 2(a)], despite the incorporation of resistive ZnO barrier in sample I. At low light intensities ($<10^{-3}$ sun), the situation changes and $R_t$ becomes significantly larger, as one could expect, for sample I [by a factor of ~1.5, Fig. 2(b)].

To assess the exact contributions of the circuit elements into spectra at different light intensities, a number of equivalent circuits have been studied according to the procedure outlined in Ref. 1. The simplest consists of two parallel assemblies of *R*-*C* elements, and is shown in Fig. 3(a). It produces two adjacent semiarcs on $Z''$-$Z'$ plot—see dashed lines in Figs. 1(a) and 2(a). This circuit represents the most simple model of a CdTe/CdS *p*-*n* junction ($R_1$-$C_1$) in series with a Schottky junction formed at the back contact ($R_2$-$C_2$).[6] From our analysis it has been found, however, that a circuit of two sections only is incapable of self-consistently describing the entire data sets. Also, a spatial inhomogeneity, probably originating from the grain boundaries in the absorber layer, made it necessary to introduce a CPE (constant phase elements) in parallel with the capacitance of the *p*-*n* junction[12] (CPEs are used to represent a distribution of circuit element values in an equivalent circuit). The final circuit consisting of three sections is shown in Fig. 3(b). To illustrate the necessity of a third section, the example of a fit by a two-section model, and including a CPE, is shown in Fig. 1(d).

Reference 1 explains how, for the case of CdTe/CdS solar cells, certain plots of admittance data are more sensitive to the variations in the equivalent circuit parameters than others. The coordinates best used for fitting of models to experimental data in this case are known to be (i) the $Z''$-$Z'$ plot, (ii) the frequency dependence of capacitance $C$ (i.e., $E'$, the real part of the dielectric permittivity), and (iii) the frequency dependence of the imaginary part of the electric modulus $M''$.[1]

In Figs. 1(e)–1(h) and Figs. 2(c) and 2(d) the same data that has been shown on $Z''$-$Z'$ plots [Figs. 1(a)–1(d) and Figs. 2(a) and 2(b)], are plotted as the frequency dependences of $E'C_S=C$ (left axis) and $M''/C_S$ (right axis), where $C_S$ is the capacitance of the sample holder. The solid lines in Figs. 1 and 2 are the fits to the equivalent circuit shown in Fig. 3(b). A good agreement is obtained for entire data sets in the range of light intensities from 1 to $10^{-4}$ sun.

## B. Analysis of extracted parameters

The extracted values of the equivalent circuit parameters are plotted in Fig. 4 as the functions of the open circuit voltage $V_{oc}$ [measured at each given light intensity $I$, $V_{oc} \propto \ln(I/I_0)$, where $I_0$ is a constant]. It is seen that the elements corresponding to the second and third sections of the circuit, Figs. 4(c)–4(h), are quite close for both samples I and II. This clear correlation supports the validity of the fitting procedure. The distinct difference between the parameters for the first section of the two samples [see Figs. 4(a) and 4(b)] is explained in Sec. III B 1 below.

Figure 4(i) shows the plots of the characteristic times for the first and third sections $\tau_0=R_0C_0$ and $\tau_2=R_2C_2$. Both $\tau_0$ and $\tau_2$ behave similarly in samples I and II. However, the two time constants differ from one another by a factor of 5. This difference can be expected since the two represent the charging/discharging events in deferent areas of a device.

### *1. First section of equivalent circuit, $R_0$-$C_0$*

The difference in the behavior of the parameters $C_0(V_{oc})$ and $R_0(V_{oc})$ for samples I and II [see Figs. 4(a) and 4(b)], is clearly related to the influence of the incorporation of the

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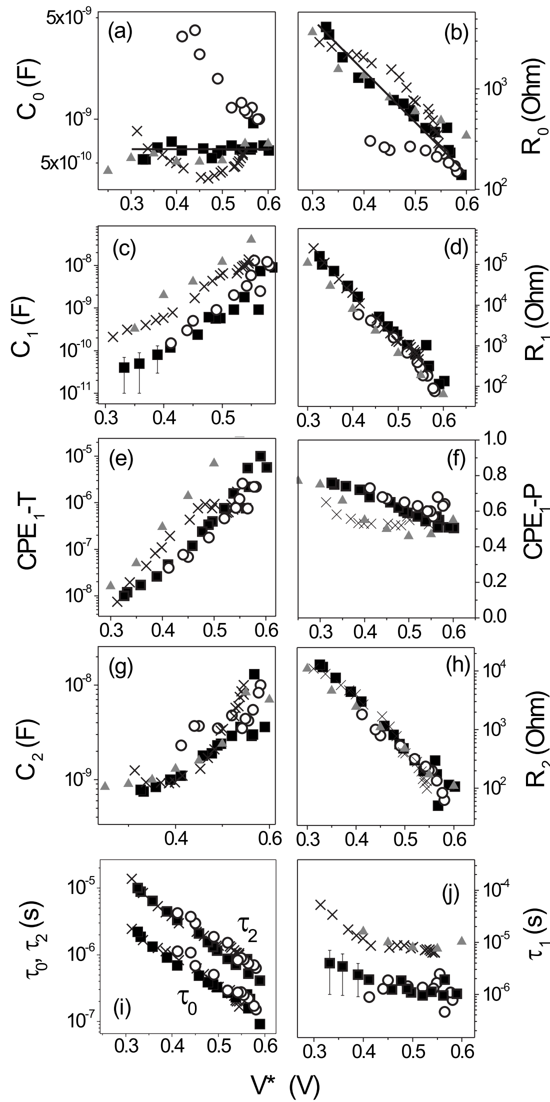


FIG. 4. [(a)–(h)] Equivalent circuit parameters obtained using the model in Fig. 3(b), plotted as functions of the open circuit voltage ($V^*=V_{oc}$ for light data, $V^*=V_{dc}$ for dark data). (i) Characteristic times $\tau_0$ and $\tau_2$ for the first and third sections of the equivalent circuit. (j) Minority carrier lifetime obtained as $\tau_1=R_1C_1$, using data in (c) and (d). Solid squares—values obtained for sample I (with ZnO), open circles—for sample II (no ZnO), crosses—sample III (all three plotted against $V_{oc}$); gray symbols—dark values for sample I (plotted against $V_{dc}$). The lines are a guide for the eye. Note that $V_{oc}$ approximately follows the log($I$) dependence, where $I$ is the light intensity.

ZnO layer, as the devices are otherwise similar. This suggestion is verified by the observed behavior of the resistance $R_0$: its values are significantly lower for sample II than for sample I over the large part of the $V_{oc}$ range, Fig. 4(b). It has been shown in Fig. 2(b) that near dark the total device resistance ($R_t$) is larger for sample I containing ZnO, which also correlates with the results of Fig. 4(b). Interestingly, the values of $R_0$ at intensities ~1 sun are very close for the two devices, indicating that the blocking effect of ZnO layer is negligible under these conditions. The latter corresponds to the general observation of increased efficiency in devices containing a barrier layer. The origin of the apparent drop of ZnO resistivity under 1 sun is not clear at this stage, but it can be suggested that it is caused by the injection of photogenerated electrons into ZnO from the main junction.

The magnitude of capacitance $C_0$ for sample I does not change significantly in the studied $V_{oc}$ range. It corresponds to a characteristic length $d\sim 400$ nm, obtained using the flat plate capacitance relation, and taking standard values for the dielectric permittivity of ZnO and CdS as ~10. This value is comparable to the sum of thicknesses of ZnO (60 nm) and CdS layers (240 nm), implying that it can be associated with the geometrical capacitance. On the other hand, the variation of $C_0$ with $V_{oc}$ in sample II shows that in this case the associated device region is electrically active. The origin of this variation can be interface states (between TCO and CdS) which are discharged under illumination, and thus resulting in the decrease of $C_0$ toward the geometrical value. It is possible to suggest in this scenario, that ZnO layer plays a passivating role—suppressing the effects of interface states.

### 2. Second section of equivalent circuit, $R_1$-$C_1$

In Fig. 4(j) the characteristic time for the second section, $\tau_1(V_{oc})=R_1C_1$, is plotted. It is seen that $\tau_1$ is almost constant at $V_{oc}>0.4$ V and of approximately the same value for both samples. For linear recombination, a diffusion capacitance and a recombination resistance have opposite (linear and reciprocal) dependence on the carrier density, due to the accumulation of carriers in the absorber layer. Thus their product, which is equivalent to a minority carrier lifetime, is expected to be rather independent of the degree of illumination and $V_{oc}$.[13] From plots in Fig. 4(j) it is seen that such a description is well applicable, hence we can attribute $C_1$ to the diffusion capacitance,[14] and $R_1$ to the recombination resistance of the absorber layer under illumination. The magnitude of the minority carrier lifetime ($\tau_1\sim 1$ $\mu$s) agrees with the value expected for a highly doped CdTe solar cell.[15]

The role of $CPE_J$ element of the second section of the equivalent circuit will be discussed in detail in Sec. III E.

### 3. Third section of equivalent circuit, $R_2$-$C_2$

The third section of equivalent circuit can be attributed to the back contact. This is supported by the fact that the structure of this region of a device is expected to be the same for samples I and II, while results in Figs. 4(g) and 4(h) show that the respective parameters are indeed very similar in the two samples. Figure 4(g) shows that the value of $C_2$ at low light or dark is ~0.8 nF, that corresponds to the depletion length of 365 nm, and is comparable to the previously reported value (~0.5 $\mu$m) for a Au/CdTe back contact.[1] Under 1 sun the depletion length decreases to ~30 nm, while $R_2$ decreases by two orders of magnitude, Fig. 4(h).

At the region adjacent to the back contact it is the number of majority carriers only that is increased under illumination, as all electrons are expelled toward the front contact by the charge separation. It is essential to point out, that in the present situation the back-contact region is under zero dc bias, as zero current condition is maintained. At the same time the Schottky diode at the back surface does not generate any photovoltage by itself, as all the light is absorbed at the front. Therefore the only possibility in which light absorbed

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in the main junction can exert the influence on the back-contact parameters is via an increase in the majority carrier density in that region by diffusion.[16]

### C. Comparison with dark measurements

There is a common notion regarding impedance properties of solid state solar cells, which the measurements in light and dark are in many respects equivalent, as in being able to provide the dc bias characteristics of the same magnitude in both cases. This largely stems from the classical studies on properties of silicon solar cells. In particular, the dc bias characteristics extracted from impedance measurements, either in light or dark, are usually expected to provide similar values of minority carrier lifetime.[17]

On the other hand, in the area of polycrystalline thin-film devices based on CdTe or $CuInGaSe_2$ materials, the main focus to date has been on the impedance studies in the dark only, while no investigations under varied illumination have been carried out. In order to make the comparison with the data obtained under illumination as described in Secs. III A and III B, impedance measurements under varied dc bias in the dark are now considered.

The obtained dark impedance spectra for samples I and II (not shown) have been found to be qualitatively similar to those in the light, Figs. 1 and 2. The equivalent circuit of Fig. 3(b) has been also found to describe the dark data very well. In Fig. 4 the parameters extracted for sample I are plotted as the functions of the applied dc bias (gray triangles). It is seen, that the dark parameters overall show similar characteristics (compare with light values for sample I, shown by black squares), however, the significant deviations occur in resistance $R_0$ (at $V_{dc} \gtrsim 0.5$ V), and in $C_1$ and $CPE_1$ values. The dark values of $C_2$ and $R_2$ appear to coincide with the light values in the entire voltage range. At the same time the obtained values of dark minority carrier lifetime, Fig. 4(j), are approximately an order of magnitude larger than the light values. It is logical to suggest that this difference originates from the change in the population of the charged defect states caused by illumination. This can also be the reason for the difference between light and dark values of parameters $C_1$ and $CPE_1$.

In terms of analysis, the main difference between the setups for light and dark measurements is that in the latter case a potential divider relation should be applied, due to the nonzero current condition. (That is, in this case a series assembly of resistances $R_0$, $R_1$, and $R_2$ forms a load for the applied dc bias. The total dc voltage applied is then divided into three potential drops across the respective regions of the device.) At the same time, in light the main junction (Sec. II of the equivalent circuit) can be considered as a voltage source $V_{oc}$, while resistors $R_0$ and $R_2$ have zero voltage drops across them, as there is no current.

Using potential divider for the dark measurements, based on the obtained values of the resistances $R_i$ $(i=0,1,2)$, it was found that the voltage across $R_0$ provides a significant contribution into $V_{dc}$ at $V_{dc} \gtrsim 0.5$ V. This can explain the observed difference in $R_0$ mentioned above. There is no substantial difference between the compared values of $C_0$, as

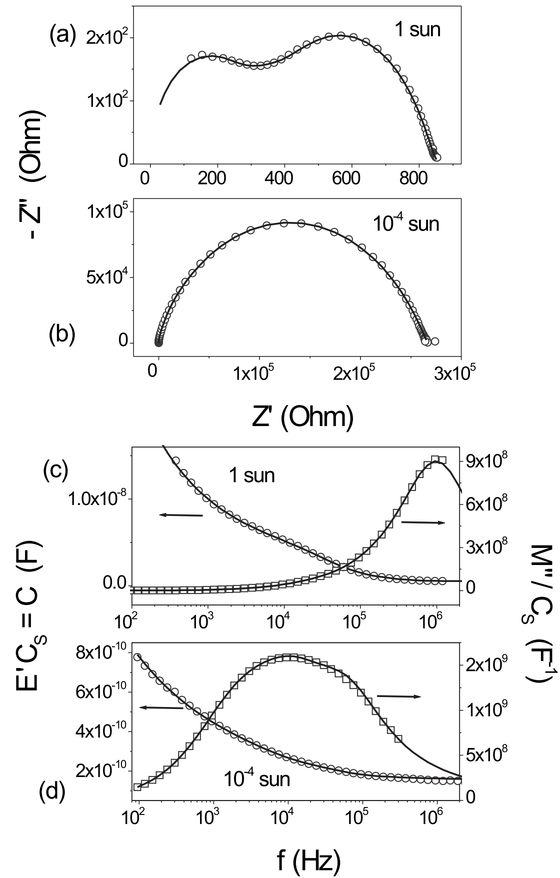


FIG. 5. Examples of impedance spectra on a $Z''$-$Z'$ plot for sample III under illumination; at 1 sun—in (a), and at $10^{-4}$ sun—in (b). [(c) and (d)] Real part of dielectric permittivity $E'$ and imaginary part of electric modulus $M''$ vs frequency at the same light intensities. Solid lines are fit to the model in Fig. 3(b).

this parameter shows only a small variation with the voltage either in light or dark. The voltage across $R_1$ $(V_1)$ provides a significant contribution into $V_{dc}$, while overall the dark characteristic $\tau_1(V_1)$ is similar to that shown in Fig. 4(j).

The voltage drop across $R_2$ has only a weak variation with $V_{dc}$ and remains smaller than 0.12 V. Thus, for section $R_2$-$C_2$ the situation in dark resembles that of the open circuit condition in the light measurements (no bias across $R_2$), which explains the similarity in both cases, Figs. 4(g) and 4(h).

### D. Impedance data for sample III (reduced absorber doping)

The examples of the impedance spectra for sample III are shown in Fig. 5. The $Z''$-$Z'$ spectra differ in the shape from those of samples I and II, while the total resistance $R_t$ is overall much larger than that in the previous cases. However, because sample III has exactly the same structure and the growth parameters as sample II (apart from $N_{As}$), the equivalent circuit shown in Fig. 3(b) is a valid candidate in this case also. Solid lines in Fig. 5 represent the best fit obtained using this model, and the obtained fitting parameters are shown by crosses in Fig. 4. It can be concluded, both from the quality

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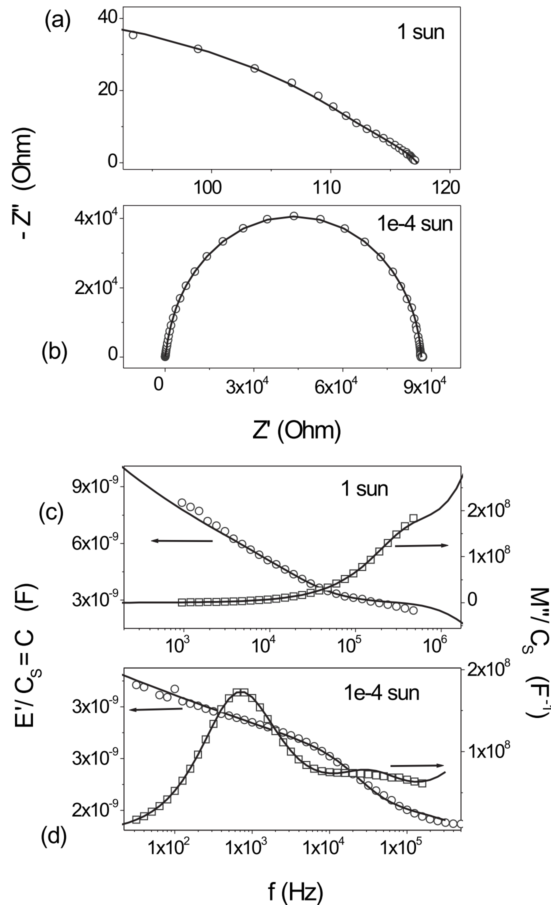


FIG. 6. [(a)–(d)] Examples of impedance spectra on a $Z''$-$Z'$ plot for sample IV at 1 sun and $10^{-4}$ sun. [(c) and (d)] Real part of dielectric permittivity $E'$ and imaginary part of electric modulus $M''$ vs frequency for the same data. Solid lines are fit to the model in Fig. 7(a).

of the fit as well as from the good correlation of the extracted parameters with those of samples I and II, that this model is indeed valid.

The values of parameters $R_2$ and $C_2$, corresponding to the back contact are very close to the values obtained in all of the cases considered so far [Figs. 4(g) and 4(h)]. This supports the interpretation of the third section in the studied equivalent circuit, given that the structure of the back contact is identical to that in samples I and II. The overall behavior of $R_0$ and $C_0$ follows that of sample I with the ZnO layer, despite the fact that sample III does not contain ZnO. This can indicate that decreased As doping can lead to a passivating effect on charged states similar to that of a ZnO layer. $R_1$ in sample III is very close to that in other samples, while $C_1$ is considerably larger, Figs. 4(c) and 4(d). This results in the minority carrier lifetime ($\tau_1 = R_1 C_1$) being approximately an order of magnitude larger than in samples I and II, Fig. 4(j).

### E. Impedance data and equivalent circuit for sample IV (barrier layer plus doped contact)

The examples of the impedance spectra obtained on sample IV are shown in Fig. 6. The spectrum at 1 sun has the complex shape and is similar to that of sample I, Fig. 6(a). At

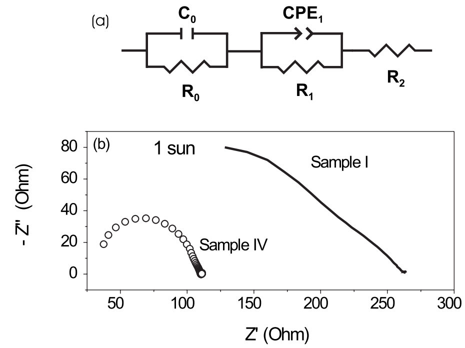


FIG. 7. (a) Simplified equivalent circuit for sample IV with improved back contact. (b) Comparison of impedance spectra on $Z''$-$Z'$ plot for samples I and IV under 1 sun.

lower light intensities, however, it very quickly becomes dominated by a single arc shape, until almost a perfect semicircle is obtained at near dark, Fig. 6(b).

The analysis has shown that to describe these spectra satisfactorily, the equivalent circuit of only two $R$-$C$ sections is needed; while section $R_2$-$C_2$ in the equivalent circuit [Fig. 3(b)] can be substituted by the fixed value resistor $R_2$ $\sim 20$ $\Omega$, due to the improvement of the back contact. It was also found that capacitance $C_1$ was not necessary in this case, so that the circuit is reduced to the simplified form shown in Fig. 7(a). The effective junction capacitance $C_1^*$ is then calculated from the obtained $CPE_1$ values according to the procedure described in the Appendix.

Figure 7(b) shows the comparison of the impedance spectra at 1 sun between sample I and sample IV. It is seen that the overall impedance of sample IV is strongly decreased by the optimization of the back contact. Fits of good quality to the spectra were obtained using the model in Fig. 7(a), and are shown by solid lines in Fig. 6. The extracted parameters are shown in Fig. 8 by solid symbols.

Until this point the potential spatial inhomogeneity of the sample region, represented by the first section $C_0$-$R_0$, has been neglected. However, we have also carried out a fitting procedure substituting capacitance $C_0$ by a constant phase element $CPE_0$. In this case the effective capacitance $C_0^*$ was obtained in the same manner as effective capacitance $C_1^*$ (see Appendix). The quality of the fit is similar to the previous case, and the obtained fitting parameters are shown in Fig. 8 by open symbols. It is seen that both of the approaches give very similar results. Moreover, the obtained values of the parameter $CPE_0$-$P$ vary between 0.95 and 1 ($CPE$-$P=1$ corresponds to an ideal capacitor, $CPE$-$T=C$), which proves that spatial inhomogeneity is very small in this case and can be neglected.

It is seen in Fig. 8(a), that capacitance $C_0$ for sample IV shows practically no variation, just as $C_0$ in sample I, Fig. 4(a). This could be expected, as both of the samples contain ZnO layer. The parameter $CPE_1$-$T$, as well as the associated capacitance $C_1^*$, shows weak variation under lower light intensities. At larger intensities, $V_{oc} \gtrsim 0.65$ V, a transition to the exponential dependence takes place. It can be suggested that this occurs when the diffusion capacitance starts dominating over the depletion capacitance, similar to the case of Si solar cells.[17]

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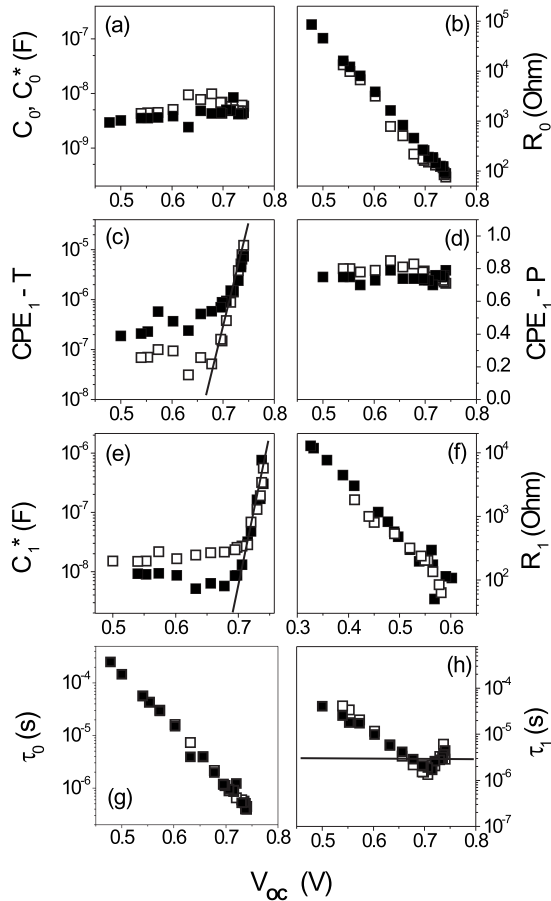


FIG. 8. [(a)–(f)] Equivalent circuit parameters against $V_{oc}$ for sample IV, obtained from the fit of impedance data under varied illumination using the model in Fig. 8(a). Different symbols correspond to the two variations of the fitting procedures: ■—with one CPE, □—with two CPEs. (g) Characteristic time of the first section $\tau_0(V_{oc})$. (h) $\tau_1^*(V_{oc})=R_1C_1^*$, corresponds to the minority carrier lifetime at $V_{oc}>0.65$ V. The straight solid lines are a guide for the eye.

The possible reason why the depletion capacitance is not clearly defined at low $V_{oc}$ values for the other samples [Fig. 4(c)], can be found in the parallel association of $CPE_J$ and $C_1$, chosen to represent the total capacitance of the junction. In this case one can assume that $C_1$ expresses the contribution from the diffusion capacitance, while the $CPE_J$ most likely expresses the depletion contribution. Although it is not straightforward why such separation of the contributions occurred for samples I–III, it is not unnatural. It agrees with the fact that depletion and diffusion parts always contribute into total junction capacitance via parallel association. Also, the diffusion capacitance might be less affected by the spatial inhomogeneity than the depletion part. Hence the former is characterized by $C$ rather than a CPE in the equivalent circuit.

In Fig. 8(h) the characteristic time $\tau_1^*=R_1C_1^*$ is plotted. After an initial decrease it saturates at $V_{oc}>0.65$ V to the value of ~3 μs, with a slight upturn at $V_{oc}>0.72$ V.

Because the diffusion capacitance dominates at $V_{oc} \gtrsim 0.65$ V, we conclude that the averaged value of $\tau_1^*$ in the same region corresponds to the minority carrier lifetime. It should be mentioned also, that the characteristic time only has the physical meaning of lifetime when the capacitance

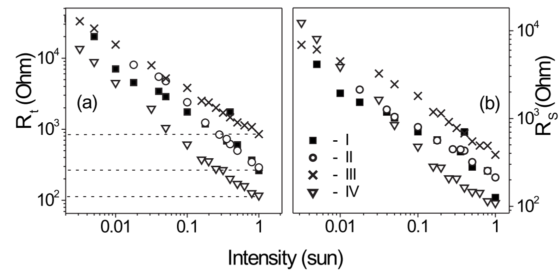


FIG. 9. Total (a) and series (b) resistance for samples I–IV vs light intensity. (■) Sample I, (○) sample II, (×) sample III, and (▽) sample IV.

employed in its calculation is the diffusion capacitance. The obtained value of averaged $\tau_1^*(V_{oc} \gtrsim 0.65 \text{ V})$ is comparable to the value of minority carrier lifetime observed in samples I and II: $\tau_1 \sim 1.5$ μs.

## IV. DISCUSSION

### A. Total and series resistance

From the comparison of $\tau_1$ in samples I–III, Fig. 4(j), it can be concluded that the magnitude of minority carrier lifetime is reduced by the increase in the chemical concentration of As. At the same time this implies that it is not $\tau_1$ that is limiting the device performance as efficiency of sample III is lowest.

On the other hand I–V measurements show that current collection ($J_{sc}$) is strongly reduced at lower $N_{As}$ (sample III), pointing out that the carrier mobility and the device series resistance can be the major factors limiting the device efficiency.

The data for the resistance values from different sections of a device, Figs. 4 and 8, allow the calculation of the series resistance of the cell due to the contact regions as: $R_s=R_0+R_2$, and the total resistance as $R_t=R_s+R_1$. In Fig. 9 $R_t$ and $R_s$ are plotted for samples I–IV. For samples I and II the values of both of the parameters $R_t$ and $R_s$ are very close at light intensities from ~0.1 to 1 sun. This suggests an important conclusion, that under sufficient illumination the ZnO layer does not make a detrimental contribution to the series resistance or carrier mobility. In the same intensity range, for sample III, $R_t$ and $R_s$ are, respectively, factors of three and two larger than in samples I–II; while for sample IV—these parameters are lower by the same factors. Because the influence of the ZnO layer on both $R_t$ and $R_s$ can be considered as negligible, the observed differences between samples can be attributed to the effect of As doping alone.

Sample III has the lowest chemical concentration $N_{As}=1\times10^{17}$ cm$^{-3}$, while three other samples have the concentration of $2\times10^{18}$ cm$^{-3}$. At the same time the net concentration of electrically active acceptors (determined by $C$-$V$) is comparable in all of the cases, $p\sim1\times10^{14}$ cm$^{-3}$).[9] Thus, from comparison in Fig. 9, it can be concluded that enhanced As concentration reduces series resistance, but not by a doping action as such. More likely, this occurs via reduction of the resistance of interfaces such as grain boundaries, where accumulation of excessive As is possible. On the other hand,

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further improvement in $R_t$ and $R_s$ takes place after the reduction of the back-contact resistance via additional doping, as is seen from comparison with sample IV.

### B. Recombination and carrier trapping in CdTe absorber layers

As it was discussed in Sec. IV A, one of the roles of the element $\mathrm{CPE}_J$ (or $\mathrm{CPE}_1$ in the case of sample IV) is to account for the depletion capacitance. Another role of this element is to represent the spatial (statistical) distribution of the junction capacitance in general. This distribution can originate from grain boundaries and structural imperfections, as well as it can be caused by the charged impurities within the absorber layer.

In the previous study a set of several well resolved deep states has been detected in a commercial CdTe/CdS solar cell.[18] These states were self-consistently incorporated into the total equivalent circuit of the device in dark.[1] The number of such deep states, however, can be arbitrary and depends on the sample growth and processing conditions. It was shown in Ref. 19, that if the number of states is large, i.e., they form a broad distribution of the trapping states, the multitude of their individual contributions into a device equivalent circuit can reduce to a single CPE. This is a result of the multiple trapping (MT) model, which was found to describe the effects of such broad trap distributions on the carrier transport in amorphous materials and also die sensitized solar cells.[19,20]

The relevance of the MT description to the studied here devices can be seen from the previous study of the densities of states for samples I and II.[21] There, a very broad distribution of deep states was obtained for both of the samples, with the range of trap energies varying from 0.4 to $\sim 1$ eV. It is thus conceivable, that the MT mechanism can be relevant to the studied samples, and that the contribution of the deep states into equivalent circuit can also occur via the constant phase element. In this case the transport of electrons in the conduction band is effectively slowed down by the trapping-detrapping events. The effective minority carrier lifetime $\tau_1^*$ (obtained using a CPE) is then expected to be larger than the lifetime of electrons in the conduction band (represented by $\tau_1$ in our case), as indeed can be seen comparing the data in Figs. 4(j) and 8(h): $\tau_1 \sim 1.5$ $\mu$s and $\tau_1^* \sim 3$ $\mu$s.

## V. CONCLUSION

A series of CdTe/CdS solar cell devices with the varied chemical concentration of As as well as the structural variations, have been studied by impedance spectroscopy under illumination from 1 to $10^{-4}$ sun. A generalized equivalent circuit model which describes the structure and the operation of the devices has been established. In particular it has been found that three samples in the series are described by exactly the same circuit model despite the variation in structure and doping. The forth device, with an improved back contact, has been described by a simplified variant of the same circuit, also showing a good correlation of the obtained parameters with those in the other samples.

The study of the effect of varied arsenic concentration has shown that the carrier mobility and series resistance are the major factors affected by such doping of the CdTe, as well as the main factors affecting efficiency. Importantly, the effect on $R_s$ from increased As level is induced not by the doping action as such, but rather is due to the accumulation of As at the interfaces and grain boundaries. On the other hand, the minority carrier lifetime is increased in the devices with lower As level, presumably due to the lower disorder, however, the device efficiency is still strongly reduced due to the accompanying increase of $R_s$. The ZnO incorporation has been found to produce no effect on the device impedance and series resistance under 1 sun illumination, while producing a significant contribution into $R_t$ and $R_s$ at lower intensities. High CdTe:As doping at the "back contact has been found to reduce dramatically the total impedance and series resistance.

Impedance measurements in the dark were carried out under varied dc bias and compared to the light measurements. It was shown that the data obtained at nonzero current conditions are much more complex for the analysis as compared to that from the zero current light measurements. The values of minority carrier lifetime obtained in light and dark were found to differ by one order of magnitude. The suggested origin of this difference is the alteration of a particular charge state of impurities and grain boundaries, induced by illumination. It was thus established that for polycrystalline thin-film solar cells the impedance measurements in the light (in the open circuit condition) is the preferred experimental method for equivalent circuit characterization.

## APPENDIX: EFFECTIVE CAPACITANCE OF A *R*-CPE SECTION

The characteristic time of a process represented by an arc or semicircle in the impedance is determined by the inverse of the frequency at which the maximum in $-Z''(Z')$ is attained. In this sense, for the circuit consisting of a single $R$-$C$ parallel assembly, the impedance can be described as

$$Z'_{R\text{-}C} = \frac{aR}{a^2+b^2}, \quad \text{and} \quad -Z''_{R\text{-}C} = \frac{bR}{a^2+b^2} \tag{A1}$$

where $a=1$, and $b=\omega CR$. Then the maximum of the imaginary part can be found at $\omega_{\max}$:

$$\left(\frac{\partial - Z''}{\partial \omega}\right) = 0, \Rightarrow \omega_{\max} = \frac{1}{RC}, \tag{A2}$$

and here $\tau = RC$ is the characteristic time.

In the case of a single $R$-CPE parallel assembly, a depressed semicircle represents its spectrum on $Z''$-$Z'$ plot,[12] while the total impedance of such a circuit is given by

$$Z_{R\text{-CPE}} = \left(\frac{1}{R} + (j\omega)^n Q\right)^{-1}, \tag{A3}$$

where $Q=\text{CPE-}T$, $n=\text{CPE}-P$, and $j=\sqrt{-1}$. Now applying Eq. 2 to Eq. 3 we find

$$\omega_{\max} = \tau^{-1} = (QR)^{1/n}. \tag{A4}$$

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Comparing Eqs. 2 and 4, one can see that the effective capacitance $C^*$ for a $R$-CPE circuit can be defined as

$$C^* = \frac{(QR)^{1/n}}{R}. \tag{A5}$$

Equation 5 describes the approach used for the determination of the equivalent capacitances $C_0^*$ and $C_1^*$ in sample IV, as mentioned in Sec. III E.

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