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Implementation of a Low Power Carry Look Ahead Adder Using Adiabetic Logic

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ABSTRACT: Now–a-days in digital circuit some important issues like high speed, high throughput, small silicon area, and low power consumption is being considered by designers. Full adders are important components in applications such as subtraction, counting, multiplication, filtering, digital signal processors (DSP) architectures and microprocessors. So for designer it is a great interest to design Carry-look ahead adder because of its high speed operation. In this paper power consumption and delay of a 4-bit carry look ahead adder, implemented in static CMOS and adiabetic logic (ECRL) is analyzed.

KEYWORDS: Adiabatic Logic, Low power, CMOS, ECRL.

I.INTRODUCTION

Binary addition is a popular methodology among computational logic elements. The n-bit adder has n one-bit full adders known as ripple carry adder. In this method the carry is computed. The addition is not complete until the n-1th adder has computed the n-1th output. The carry chain is meant for the total delay of the logic element. Therefore, speeding up the adder needs the speeding up the carry chain. As speed of the addition is the main criteria with nominal amount of power consumption, the carry look ahead adder has been chosen. The carry-look-ahead adder is one way to speed up the carry computation. The carry-look-ahead adder breaks the carry computation into two steps, starting with the computation of two intermediate values. If the adder has two inputs ai and bi, then propagate(Pi) and generate (Gi) can be written as follows.

$P_i = A_i(Xor)B_i$ (1)
$G_i = A_i.B_i$ (2)

Both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay.

The sum and carry output can be written as follows

$C_{i+1} = G_i + P_iC_i$ (3)
$S_i = C_i\,(Xor)A_i(Xor)B_i$ (4)

So, C_{i+1} is a function of inputs and C_i . These equations show that a carry signal will be generated in two cases:
1) If both bits Ai and Bi are 1
2) If either Ai or Bi is 1 and the carry-in Ci is 1.

The schematic diagram of sum output of a 4-bit carry-look ahead adder is shown in Figure 1. The Cin and 3 carry outputs have been used to generate 4-bit sum output.

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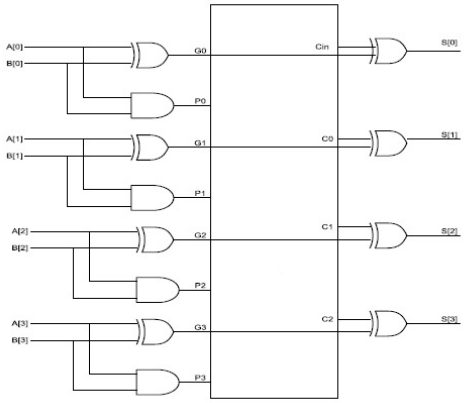

Fig.1 Schematic diagram of output sum

II. ADDER IMPLEMENTATION

The adder is implemented by two methods.

A. STATIC CMOS LOGIC

In standard CMOS circuits, the power dissipation typically occurs during the switching mechanism. The changes are fed from the power supplied to the MOS devices and then dumped into the load capacitor of the circuit. Both the PMOS and NMOS transistors can be assumed as an ideal switch in series with a resistor for the illustration of the effective channel resistance of the switch in addition to the interrelated resistance in the circuit. The pull up and pull down networks are connected to the load capacitance C_L, which is also known as the node capacitance.
The gates used in the adder are shown in Figure 2 for static CMOS logic.

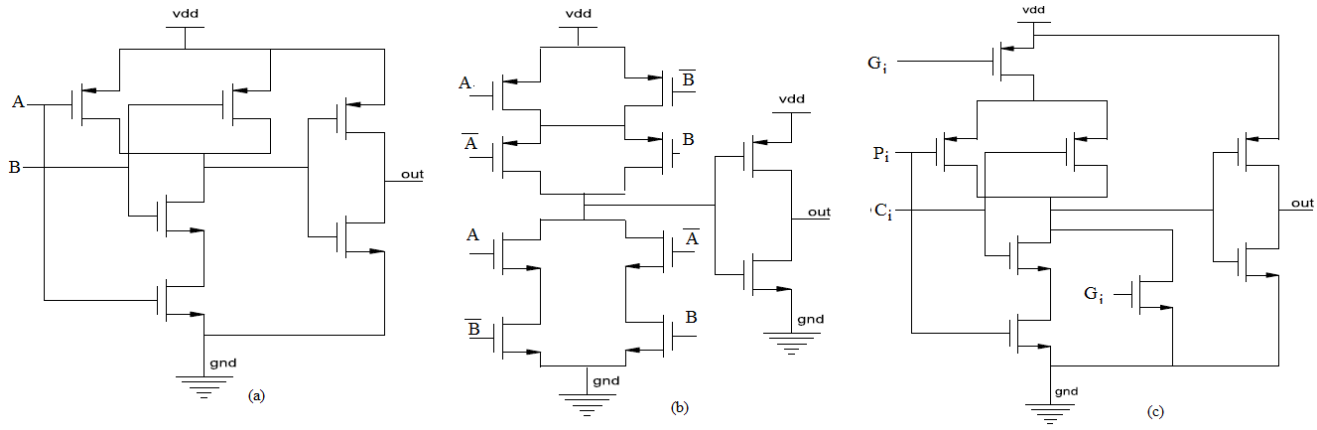

Fig.2 Static CMOS (a)And gate (b) Xor gate (c) Circuit for C_{out}

B. ADIABATIC ECRL LOGIC

The word adiabatic, a greek word means impassable, indicating for the state transition that occurs without any heat loss or heat gain [1,2]. The adiabatic logic family has been designed by implementing PMOS and NMOS transistors of pull down network and pull up network. Conventional CMOS based designs consume a lot of energy in switching process whereas in the adiabatic switching technique the energy dissipation through PMOS during charging process is reduced and some of the energy, stored on load capacitor during the discharging phase is reused [3,4]. Figure 3 illustrates the equivalent model during charging process in adiabatic circuits. Here the output load capacitance is charged by a

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constant current source instead of a constant voltage source used in conventional CMOS structures. R is the on resistance of pull up PMOS network and C_0 is the output capacitance [4].

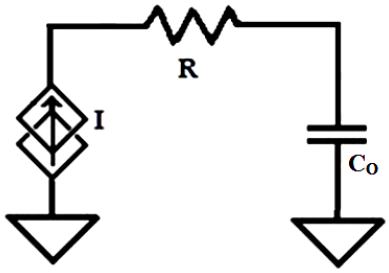

Fig. 3 Equivalent model during charging process in adiabatic circuits

Thus energy dissipation depends upon on resistance R, and it can be minimized by reducing it. Also by increasing the charging time greater than $2RC_0$ dissipation can be reduced up to large extent. Adiabatic circuits do not utilize standard power supplies as in CMOS circuits; it uses pulsed power supply .

In the Adiabatic logic circuits, the load capacitance is charged through a constant current source instead of a constant voltage source as in case of conventional CMOS circuits [5]. The Adiabatic switching technique is commonly used to minimize the energy loss during the charging and discharging of the load capacitor. In adiabatic circuits, all of the capacitors are charged or discharged at a constant current for the minimization of the power dissipation.

Efficient Charge Recovery logic (ECRL) is One of the most simplest design of the Adiabatic logic where the charge recovery part of the circuit is composed of two cross connected pMOS transistors and the logic portion is made of nMOS transistors. Both the actual logic and the inversion of it can be get from this adiabatic logic circuit.
The gates used in the adder are shown in Figure 4 for ECRL.

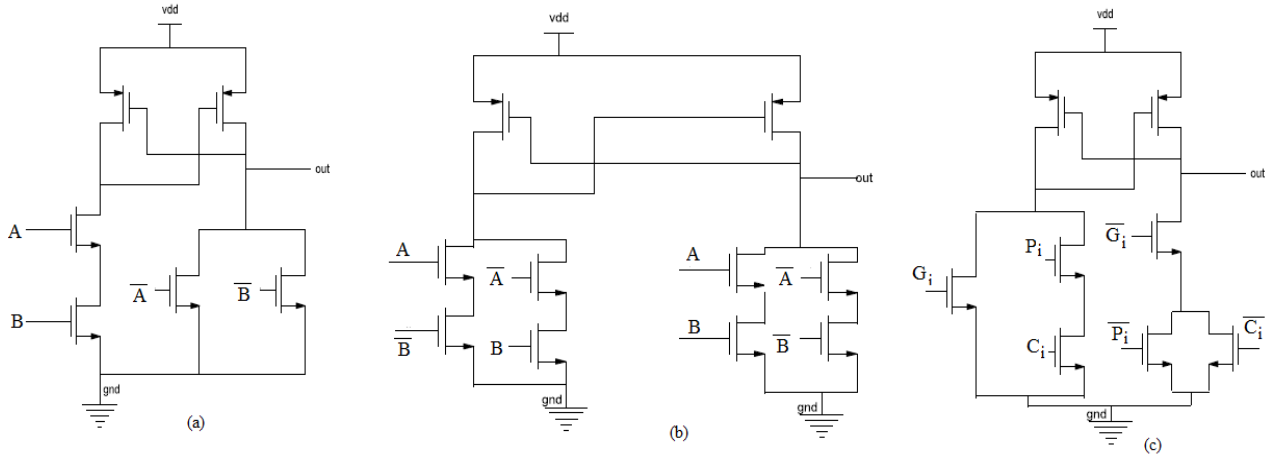

Fig.4 ECRL (a)And gate (b) Xor gate (c) Circuit for C_{out}

III. RESULT ANALYSIS

In this paper we have calculated the power dissipation for static CMOS and ECRL adiabatic 4 bit carry look ahead adder using T-SPICE simulation tool. The observed delay and power are shown in Figure 5 and Figure 6 respectively. From the calculation we have done, it has been found that CLA using ECRL logic have low power dissipation . So, it can be used to design low power circuits. The transistor count and delay is larger than static CMOS logic. Table I indicates the no of transistor required in both logic.

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TABLE I
NO OF TRANSISTOR

Logic style	And Gate	Xor Gate	4 bit CLA
Static CMOS	6	14	168
ECRL	10	14	208

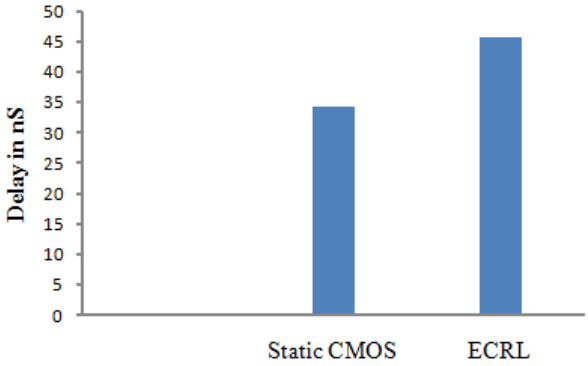

Fig. 5 Observed delay of 4 bit CLA

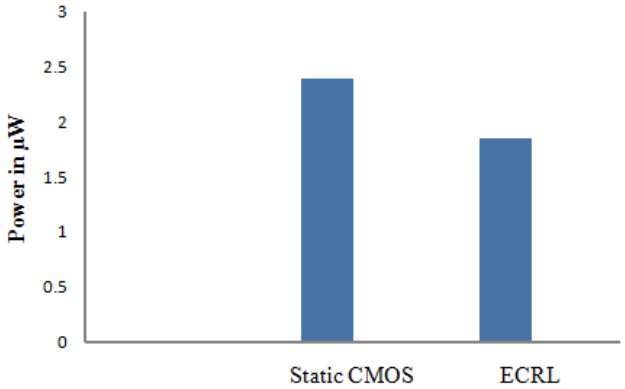

Fig. 6 Observed power of 4 bit CLA

IV. CONCLUSION

Adiabatic logic is an efficient technique for designing low power circuits compared to conventional CMOS logic. Simulation indicates it is a power saving logic. From the analysis we can conclude CLA using ECRL logic is a good option for low power circuit design.

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Dr. Atanu Nag is working as the Assistant Professor in the Department of Physics, Modern Institute of Engineering &Technology. He has published more than 25 papers in International Journals and attended many conferences.

Mr. S Bose completed his M. Tech degree in Electronics & Communication Engineering and is a PhD Research Scholar at Bengal Engineering and Science University-BESU, Shibpur. He has 7 Years of teaching & industry experience