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Implementation of a New Compact Inverter Structure Controlled by Numeric Sinusoidal Pulse Width Modulation for Photovoltaic Applications

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Abstract

In order to cover energy requirement, the photovoltaic is one of the proposed solutions. However, according to the aim of its utilization, the direct current output voltage of photovoltaic source should be adjusted. The boost inverter is a recent power processing stage that can increase, filter and alternate direct current input voltage. So as to control it, there are various modulation types. Among them, the sinusoidal pulse width modulation is presented in a new digital form. The operating principle of the aforementioned inverter and command have been analyzed and verified by simulation and realization. Furthermore, frequency analysis of output voltage signal proves efficient results.

Keywords: Renewable energy; Boost; Inverter; SPWM; Control; Microcontroller

Introduction

Energy crises and environmental pollution caused by consumption of traditional energy sources lead scientists to think about renewable energies to satisfy the world needs of electricity [1]. So, nowadays renewable energies are the most important subjects that researches and studies discuss [2]. Among these energy types, the solar is predicted to cover the maximum need of energy in the future [3]. Thus, a lot of articles present different photovoltaic systems structures [2,4,5], which are based on many power processing stages. This paper will focus on the inverter stage and its command. The structure presented here is very recent and understudied; it allows a conversion in a single stage with AC output voltage higher than the input voltage [6]. It is the boost inverter. The inverter supply is provided by three series batteries of 24 V. Thus, the inverter is powered by 72 V. The inverter output is modulated by a digital sinusoidal pulse width modulation SPWM inspired from the analogical one.

To give more details on this structure, this paper will contain in the first part the construction of the inverter, its principle of operating, and a simulation which interpret its performance. In the second part, the experimental study is presented to prove simulation results.

System Description

The boost inverter discussed here allows producing a filtered and amplified alternative voltage. It contains two bidirectional boost converters connected deferentially to a load [6,7]. Controlled by sinusoidal pulse width modulation SPWM command, each converter produces a DC voltage and an alternative component. The alternative components are sinusoidal signals and in phase opposition, whereas the DC components have the same value. This structure is shown by Figure 1 [8].

The output voltages V_{01} and V_{02} for both converters are presented by Eq. (1) and Eq. (2) [9,10].

$$V_{01}(t) = V_{dc} + V_{max}\sin(\omega t) \quad (1)$$

$$V_{02}(t) = V_{dc} - V_{max}\sin(\omega t) \quad (2)$$

The output voltage of the inverter is in "Eq. (3)"

$$V_{02(t)} = V_{01}(t) - V_{02}(t) = 2 * V_{max}\sin(\omega t) \quad (3)$$

In order to explain the functioning of this inverter, we will consider one converter as shown in Figure 2 [9,10]:

The functioning of the converter is divided into two parts:

[0, d*T_{c3}]: The switch M_3 is closed while M_4 is open, I_{l3} increases linearly, D_4 is reverse polarized, C_3 provides the load with energy, which decreases V_{01}.

[d*T_{c3}, T_{c3}]: The switch M_4 is closed while M_3 is open, C_3 is charging by I_{l3}. So, the voltage V_{01} increases [9,10].

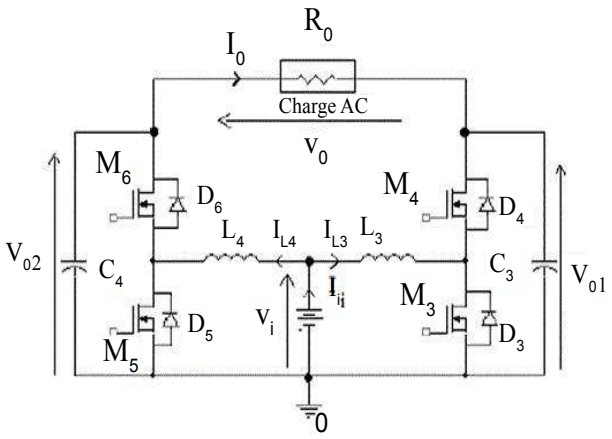

Figure 1: Boost inverter.

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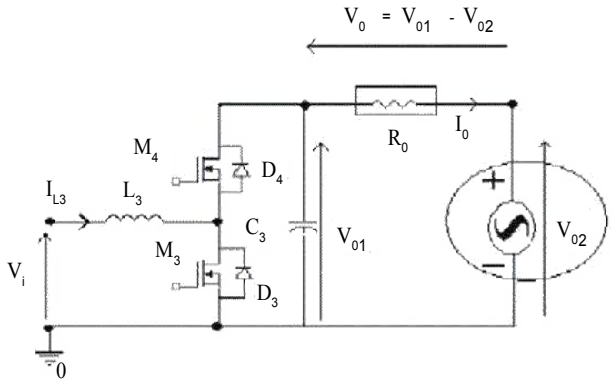

Figure 2: Equivalent circuit of the boost inverter.

Where d is the duty cycle, Tc is the switching period

When one converter is in boost operating the other should be in buck operating. The average voltage's expression for the first converter [11] is in Eq. (4) while that of the second is corresponding to Eq. (5):

$$V_{01} = \frac{Vi}{1-d} \tag{4}$$

$$V_{02} = \frac{Vi}{d} \tag{5}$$

Then the transfer function can be concluded in Eq. (6):

$$\frac{V_0}{Vi} = \frac{2d-1}{d(1-d)} \tag{6}$$

(6) For d_0=0.5, V_0=0, then if we vary d near to d_0 we will have an AC output voltage. Via the transfer function we can conclude that the duty cycle is "Eq. (7)"

$$d = 0.5 - \frac{2 - \sqrt{4 + \left(\frac{V_0}{V_i}\right)^2}}{2 * \left(\frac{V_0}{V_i}\right)} \tag{7}$$

A linearization of this equation around d_0 gives "Eq. (8)":

$$d = \frac{1}{2} + \frac{V_0}{8 * V_i} \tag{8}$$

If we consider that V_0 is sinusoidal we will have "Eq. (9)"

$$d = \frac{1}{2} + \frac{V_{0\max} \sin(2\pi f t)}{8 * V_i} \tag{9}$$

Where f is the frequency

This equation presents the duty cycle's variation near to d_0. To elaborate the command SPWM, in order to have a sinusoidal V_0, we will use the aforementioned "Eq. (9)".

The Digital Sinusoidal Pulse Width Modulation

To produce a sinusoidal voltage using this inverter, we command it with a digital modulation SPWM inspired from the analogical one. It applies the same concept which is logic comparison of a sinusoidal wave to another triangular. So as to command the interrupters, we make use of the intersections of these signals [11-13].

As Figure 3 presents, the triangular signal is produced by a binary counter. It counts till a maximum value, stored in a register, then counts down until a minimal value. The sinusoidal one is represented by a table of values obtained by sampling a sinusoidal signal; this table is stored in a memory. The period of sampling is the same as commutation period of the inverter, which is equal to the period of the triangular signal elaborated by the counter.

In each period of sinusoidal signal, a software comparison between these two signals is done so as to produce an impulsion in higher or lower state.

The sinusoidal signal period gives suit of periodic impulsions modeled in width according to a sinusoidal law.

The numeric command SPWM is implemented in the microcontroller 16 F876 (20 MHz). The resulted SPWM signal should command MOSFET transistors. Since the intensity and the amplitude of this signal are unable to commutate the MOSFET, we added a driver between the microcontroller and the transistors. It is IR2111 circuit.

We can also produce the timing sequence by Excel software or Matlab and store it on the chip. This will allow us to optimize the chip performance.

Finally, in order to protect the microcontroller we added an optocoupler before the driver.

The circuit which produces the SPWM signals is presented in Figure 4.

Simulation

This part present a simulation of the inverter structure and its command discussed in the beginning under a power of 300 W. The inverter characteristics simulated are: Inductor: 0.23 µH, The capacitor: 260 µF, MOSFET: W45NM50 (Table 1).

The following Figures 5-10 show the realized inverter circuit in Orcade software and its simulation results:

According to the simulation results, the output voltage waveforms are sinusoidal; they have a frequency of 50 Hz and amplitude of 110 V.

Realization

After verification and validation by simulation, now we present a practical implementation of the realized inverter structure and its command.

Magnetic Circuit	EI40
Wire section	5,27 mm²
Value of air gaps	2 mm
Number of coils	45

Table 1: Inverter characteristics.

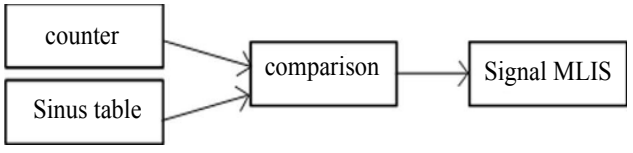

Figure 3: Method of SPWM signal generation.

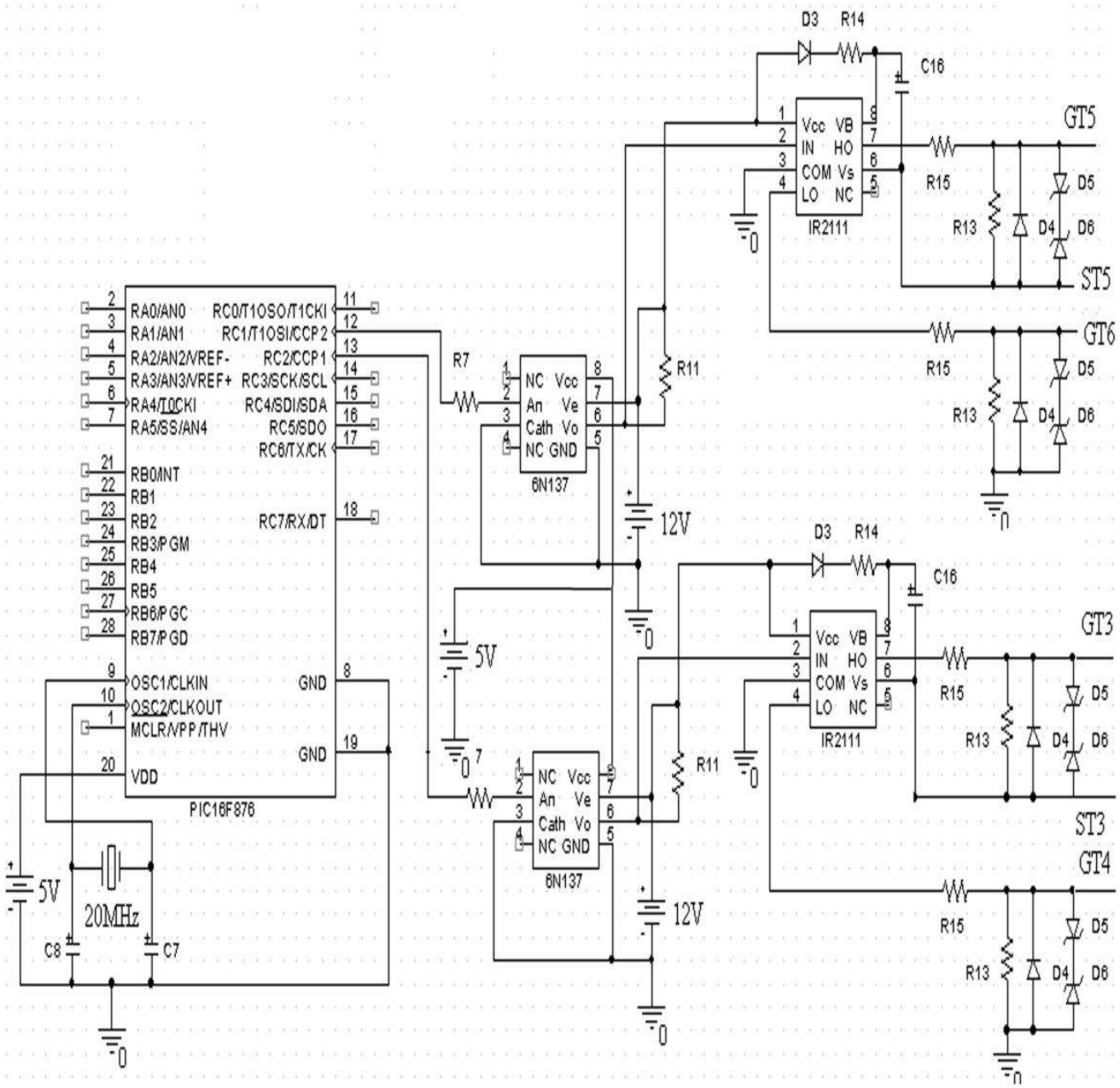

Figure 4: SPWM electroniccuit cir.

Inverter

In Figure 11 below shows the fabricated inverter.

The command card: The control card is built with the microcontroller PIC16F876 and three circuits. They are used for isolation, adaptation and interfacing with the microcomputer. This card has two inputs and five outputs, four of them are used to command the switches of the inverter.

In Figure 12 below shows the realized command card.

The microcontroller chosen to implement the SPWM technique has two PWM outputs and a memory. The outputs generate the SPWM signal whereas the memory accommodates the program. The maximum clock frequency that the microcontroller can accept is 20 MHz. The implementation of the mechanism SPWM in the microcontroller goes through three steps: Firstly, a configuration in pulse with modulation mode of two outputs "CCP1" and "CCP2" should be done.

Secondly, the period T_{C3} of PWM signals is defined according to "Eq. (10)":

$$T_{C3} = (PR_2 + 1) \times T_{OSC} \times T_P \quad (10)$$

Where the period of the oscillator is T_{osc}, the predivisor of timer 2 is T_p and PR_2 is a register.

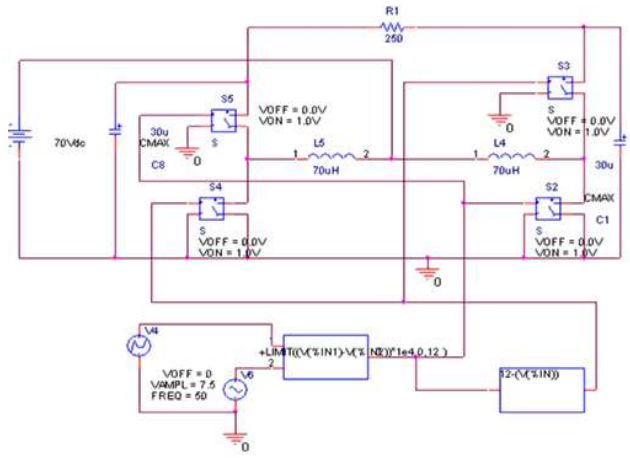

Figure 5: Boost inverter.

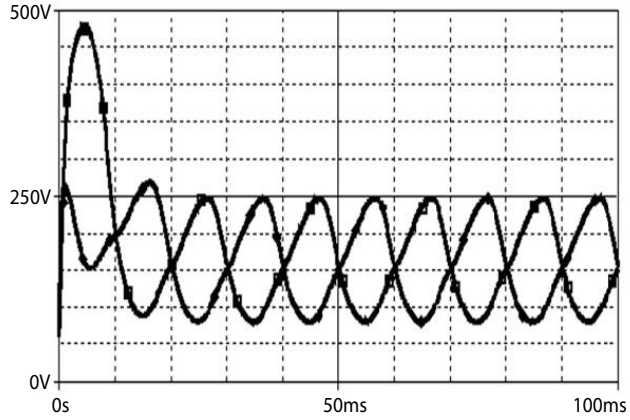

Figure 6: Output voltages of each converter.

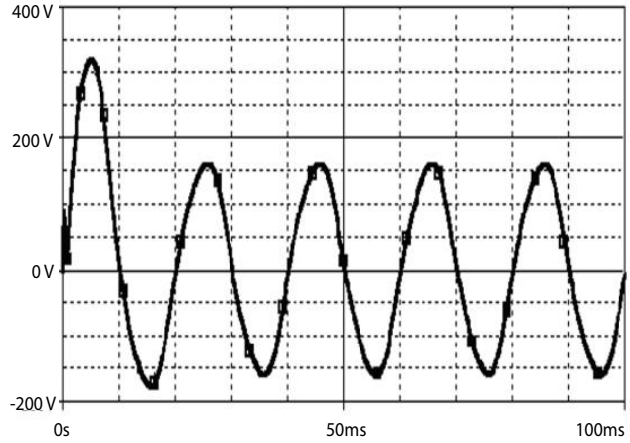

Figure 7: The inverter output voltage for a resistive load.

In order to fix the T_{C3} value to a required one, we should load the register PR_2 by a decimal value from "0" to "255".

Thirdly, the values K_i, which give the duty cycles D_i of number n, will be stored in a table and then loaded periodically according to a repetitive process. The loading procedure will be done by a timekeeper; it can belong to one of registers CCPR1L or CCPR2L according to "Eq. (11)" or "Eq. (12)".

$$(CCPR1L) \times T_{OSC} \times T_P \quad (11)$$

$$(CCPR2L) \times T_{OSC} \times T_P \quad (12)$$

Depending on "Eq. (13)", the generation of table's values K_i can be done by using a software tool. Which help to obtain the duty cycle D_i depending on "Eq. (14)".

$$K_i = B + A \times Sin\left(\frac{2 \times \pi \times i}{n}\right) \quad (13)$$

The value of i goes from 1 until n

$$D_i = \frac{k_i}{PR_2} \quad (14)$$

The constants B, A and n will be determined as described subsequently.

The number n presents the number of duty cycles. It's given by the report T_{c3}/T_r.

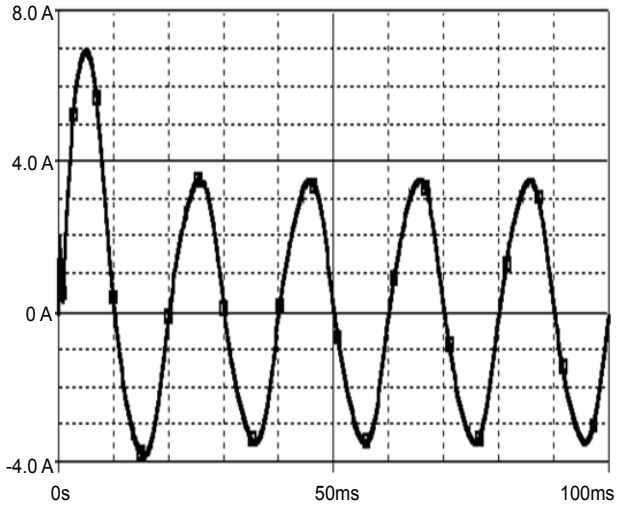

Figure 8: Boost inverter output current for a resistive load.

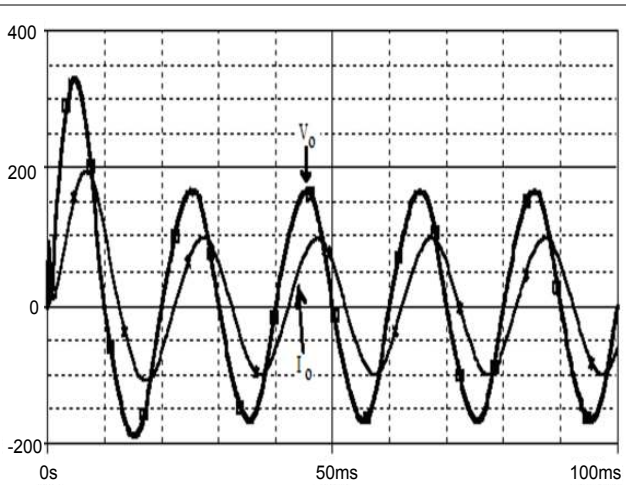

Figure 9: Boost inverter output current and voltage for a RL load.

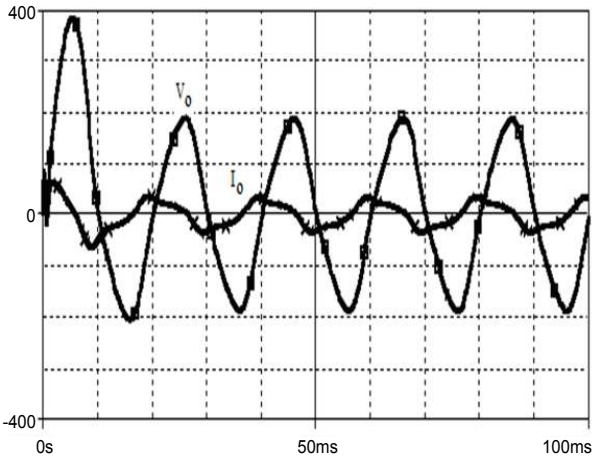

Figure 10: Boost inverter output current and voltage for a RC load.

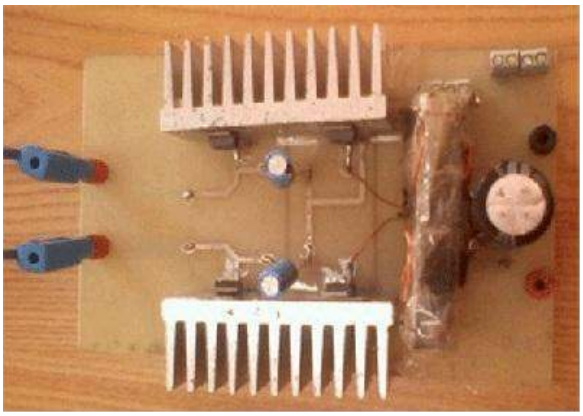

Figure 11: Realized boost inverter.

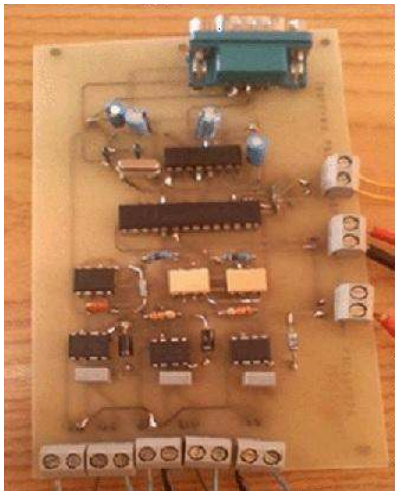

Figure 12: Command card.

To choose A and B, on the one hand, we should consider the size of both registers CCPR1L and CCPR2L of 8 bits, thus these constants are positive and decimal. On the other hand, they will be chosen in order to have the duty cycle value equal to 50% for t=0, equal to 95% for t=T_r/4 and equal to 5% for t=3 T_r/4.

The maximum duty cycle value 95% is obtained by "Eq. (15)":

$$\sin\left(\frac{2\times\pi\times i}{n}\right)=1 \quad (15)$$

That will help to conclude the value of B+A

As the duty cycle value 50% is obtained depending on "Eq. (16)":

$$\sin\left(\frac{2\times\pi\times i}{n}\right)=0 \quad (16)$$

The value of B and then that of A will be easily deduced.

The implanted SPWM program undergoes from an interruption. This made the two values Ki and 255-Ki read and loaded simultaneously in both registers CCPR1L and CCPR2L. Then during every period $T_{C3,}$ two complementary motives SPWM are produced. This is caused by the over follow of timer 2. So we obtain the two desired signals SPWM during the period T_r.

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Experimental results

The output differential voltage of the realized boost inverter, applied on a resistive load, a capacitive load and inductive load, is presented in Figures 13-15.

These results show an output voltage highly near to be sinusoidal. It has a frequency of 59.94, a RMS voltage of 110.

Frequency analysis

Applying Fast Fourier Transform FFT on the inverter output voltage of every loads type offer various characteristics which are illustrated in Figure 16.

The fundamental has amplitude of 110 V; the 3rd harmonics remains the most dominant with low amplitude of 3.32 V. This value can be negligible compared to the amplitude of the fundamental.

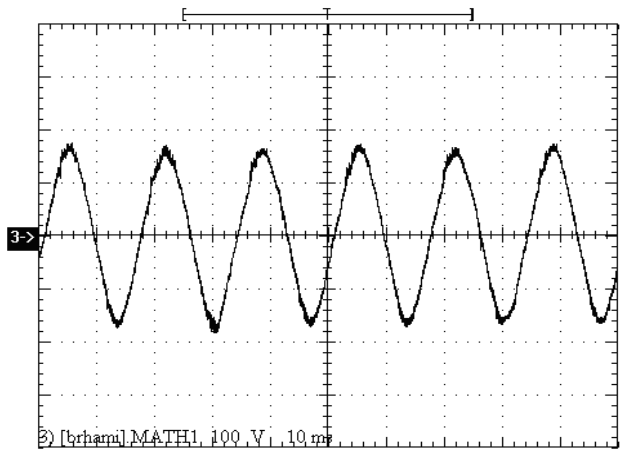

Figure 13: Output voltage V_0 for a resistive load.

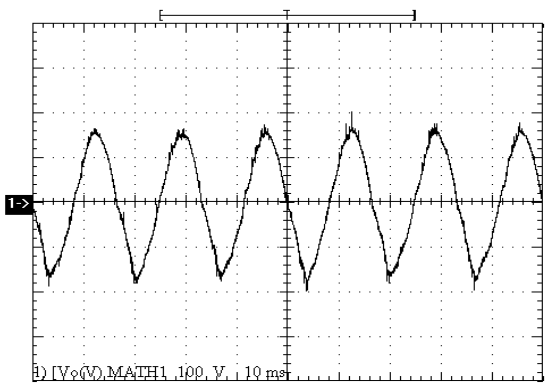

Figure 14: Output voltage V_0 for an inductive load.

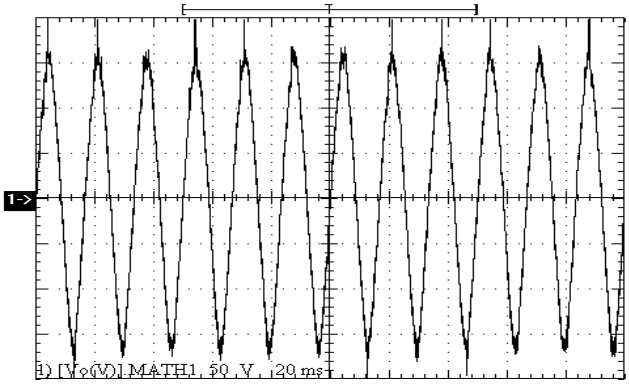

Figure 15: Output voltage V_0 for a capacitive load.

Voltage = 110.09 V Voltage THD = 4.164 % Power Factor = n/a Apparent Power = n/a			Current = n/a Current THD = n/a Displacement Power Factor Reactive Power = n/a		Voltage = 110.91 V Voltage THD = 4.588 % Power Factor = n/a Apparent Power = n/a			Voltage = 112.21 V Voltage THD = 4.622 % Power Factor = n/a Apparent Power = n/a		
	Frequency	**Voltage RMS**	**Voltage % of Fund.**	**Voltage Phase**	**Voltage RMS**	**Voltage % of Fund.**	**Voltage Phase**	**Voltage RMS**	**Voltage % of Fund.**	**Voltage Phase**
Fundamental	59.940 Hz	109.60 V	100.000 %	0.0000	110.65 V	100.000 %	0.0000	110.80 V	100.000 %	0.0000
Harmonic 2	119.88 Hz	928.34m V	0.847 %	-62.551	2.5168 V	2.275 %	-69.076	3.0067 V	2.714 %	-93.327
Harmonic 3	179.82 Hz	3.3271 V	3.036 %	-1.2173	3.7867 V	3.422 %	15.665	3.8359 V	3.462 %	1.7724
Harmonic 4	239.76 Hz	898.29m V	0.820 %	144.65	1.0919 V	0.987 %	-151.30	543.63m V	0.491 %	151.75
Harmonic 5	299.70 Hz	1.2976 V	1.184 %	-172.00	1.4031 V	1.268 %	150.63	511.54m V	0.462 %	164.54
Harmonic 6	359.64 Hz	1.1826 V	1.079 %	-73.766	624.79m V	0.565 %	-17.426	508.27m V	0.459 %	151.08
Harmonic 7	419.58 Hz	981.44m V	0.895 %	41.093	390.88m V	0.353 %	-163.07	763.53m V	0.689 %	74.691
Harmonic 8	479.52 Hz	757.23m V	0.691 %	19.301	678.75m V	0.613 %	130.41	441.99m V	0.399 %	-155.89
Harmonic 9	539.46 Hz	1.3087 V	1.194 %	-167.52	264.53m V	0.239 %	-75.936	554.53m V	0.500 %	169.37
Harmonic 10	599.40 Hz	827.25m V	0.755 %	-23.389	378.94m V	0.342 %	99.914	492.39m V	0.444 %	18.786
Harmonic 11	659.34 Hz	467.90m V	0.427 %	29.883	290.74m V	0.263 %	60.180	54.044m V	0.049 %	-56.266
Harmonic 12	719.28 Hz	430.21m V	0.393 %	70.364	683.51m V	0.618 %	56.649	159.31m V	0.144 %	-44.136
Harmonic 13	779.22 Hz	343.88m V	0.314 %	-15.485	301.10m V	0.272 %	-91.870	20.104m V	0.018 %	140.58

Figure 16: FFT for different load types.

Practical results obtained show a favorable functioning of this inverter; its yield can be improved by an optimal choice of the interrupters used to establish it.

Conclusion

In this paper we have established and evaluated a new inverter structure which allows boosting, undulating and filtering a DC voltage in a single stage.

The modulation is implemented in a digital form using a microcontroller which guaranties a good functioning. And the realization done supports and shows the optimal functioning of the inverter with different linear and non linear loads.

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