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Implementation of Designed PV Integrated Controlled Converter System

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ABSTRACT Photovoltaic (PV) energy has increased drastically at an average annual rate of 60% in the last few years. It quickly became an integral part of the power system networks. This increase, in turn, has triggered the evolution of PV power converters with more efficiency and reliability. In this paper, a prototype of the PV integrated controlled converter system is designed, which is applicable in water pumping for irrigation. Main components of this system are floating dual boost converter (FDBC), three-phase voltage source inverter (VSI) and three-phase squirrel cage induction motor (pump). For address the issue of PV voltage fluctuations, a voltage mode controller is designed for the FDBC which regulates the output voltage of the FDBC to a fixed value irrespective of any voltage fluctuations at the PV side.

INDEX TERMS Floating dual boost converter, photovoltaic system, power converter.

NOMENCLATURE

v_{in}/v_o	The input voltage of FDBC/ Average output voltage of FDBC
v_{C1}/v_{C2}	The voltage across C_1/Voltage across C_2
i_{in}/i_o	The input current of FDBC/ Average load current of FDBC
i_{L1}/i_{L2}	Inductor (L_1) current/Inductor (L_2) current
Δv_c /Δi_L	Capacitor ripple voltage of FDBC /Inductor ripple current
$\Delta v_0/\Delta i$	Output voltage ripple of FDBC /Input current ripple of FDBC
R	Resistive load of FDBC
d	The duty cycle of FDBC
f_s	Switching frequency

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I. INTRODUCTION

In today's world, the most important downside faced in the field of the power sector is the incrementing power demand and is probably to rise to 76% by 2030. In overpopulated countries, like India, there is a dearth of power-generating resources, and as a result, many cities and towns are facing constant load shedding and black-outs. Another concern is that the power generating stations and distribution locations are far from each other resulting in insufficient power supply to the rural areas. Renewable energy sources (RES) in conjunction with power electronics is one of the potential solutions to tackle the problems of power demand and lack of flexibility in power distribution. Solar energy is considered to be one of the most important renewable energy sources (RES) because it is free of cost, abundantly available and pollution-free. The technology of converting solar energy into electricity is called photovoltaic (PV) and is done using semiconductor that exhibits photovoltaic. Solar energy-based applications are being widely used in many islands and rural

areas where the distribution networks do not reach. One of the most promising applications is solar water pumping for irrigation.

Agriculture is the backbone of India. Statistically, 64% of the cultivated land depends on monsoon. Therefore it is essential to provide and improve irrigation methodology in India. However, due to lack of generation and distribution of electric energy in agricultural areas of India, it is difficult to implement an effective and efficient irrigation system. PV water pumping irrigation system is one of the feasible solutions to this problem. PV systems for water pumping applications are extensively used around the world as they are highly reliable systems that inherently require low maintenance. Use of solar energy for irrigation is suggested in [1]. In [2] authors proposed a solar-powered automatic irrigation system. Solar-powered drip irrigation scheme is presented in [3]. Optimal design of the solar-powered fuzzy control irrigation system is proposed in [4].However, high initial cost and low energy conversion efficiency result in high expense [5]. Therefore, there is scope and need for research in this domain.

Though there are various techniques for solar-based irrigation, the basic system includes a PV system, a converter module and a motor (pump) as load. PV fed DC motor for water pumping is available in the literature. However, they have limited applications due to the high cost and maintenance problems of DC motors for being commutators type machines [6]. On the contrary, the induction motor is free from brushes and commutators and maintenance is almost negligible. Thus DC motors are now replaced by induction motors for solar pumping.

The output of PV is low-level DC voltage and needs to be boosted to a higher level for any potential application [7]. The converter module does this. A transformer in many applications is used to provide increased voltage gain [8]. However, for large power conversion the size as well as the cost of the transformer increases. Thus making the system bulky and expensive. As a result, transformer-less power electronic converter systems are now becoming popular [9]. Transformer-less power electronic converter systems consist of a DC-DC boost converter and also an inverter if the load is AC. The voltage gain is controlled by the duty cycle of the DC-DC boost converter. The conventional boost converter topology cannot be used for high voltage conversion [10]. Some potential topologies of DC-DC converter with high gain are presented in [11], [12]. However, the concept of high current ripples is a drawback. The technique of interleaving reduces high ripple current. However, the voltage gain is the same as that of the conventional boost converter. Some of the interleaved topologies with high voltage gain are presented in [13], [14]. Other high gain topologies are proposed in [15]–[21]. The converter topology implemented in this paper was proposed in [22]. It comprised of two conventional boost modules connected in parallel at the input, namely the non-floating topology and the floating topology. Parallel connection of the two modules at the input side and the phase-shifted control signals between the two switches ensures interleaving. This topology is known as floating dual boost converter (FDBC). Another issue that has to be tackled is the problem of PV voltage fluctuation. As it is evident that the PV voltage is a function of irradiance which varies with time, thus the PV output voltage is not constant throughout when driving a constant load. This problem of voltage fluctuations needs to be addressed [23]–[34].

The objective of this work is to design a prototype of a PV integrated controlled converter system applicable to water pumping for irrigation. Main components of this system are an FDBC, a three-phase voltage source inverter (VSI) and a three-phase squirrel cage induction motor (pump). For address the issue of PV voltage fluctuations, a voltage mode controller is designed for the FDBC which regulates the output voltage of the FDBC to a fixed value irrespective of any voltage fluctuations at the PV side.

II. PROPOSED SYSTEM DESCRIPTION

Block diagram of the proposed system shown in Fig. 1. This system is basically a PV fed converter module driving an induction motor. The input to the system is from a series of connected PV panels. Each PV panel is rated for 35 V, 8 amps. Four such panels are connected in series to obtain a PV array of rating 140 V, 8 amps. The PV array is the input to the floating dual boost converter (FDBC). The PV voltage is boosted to 485 V by the FDBC to drive the induction motor. The DC output of the FDBC is fed to a conventional three-phase voltage source inverter (VSI) for conversion from DC to AC and then connected to the three-phase induction motor. The three-phase VSI is operated in 180 degrees conduction mode. The motor is rated for 400 V (rms), 1.8 amps. A voltage mode controller is incorporated using DSPIC30F4011 for the FDBC. The voltage mode controller ensures that the input voltage to the VSI is maintained constant irrespective of voltage fluctuations in the PV output voltage.

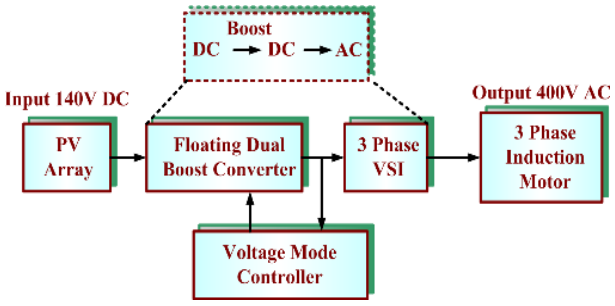


FIGURE 1. Block diagram of PV integrated controlled converter system.

III. MODELLING OF FDBC

The floating dual boost converter, also known as a two-phase interleaved double dual boost converter, consists of two modules. Module 1 comprises of L_1, S_1 and C_1 and module 2 comprises of L_2, S_2, and C_2. The steady-state operating point is chosen at duty cycle $> 50\%$. Fig. 2(a) shows a circuit diagram and Fig. 2(b) shows the switching sequence of FDBC.

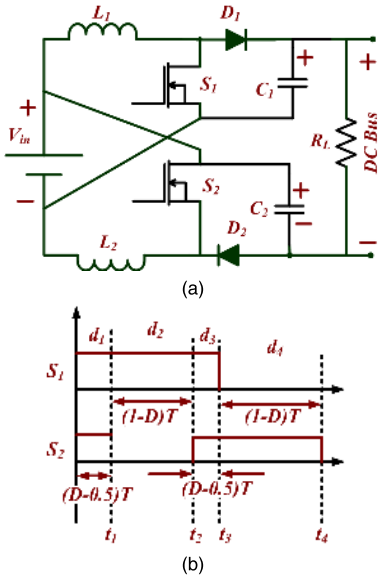


FIGURE 2. Circuit diagram and switching sequence of FDBC, (a) circuit diagram of FDBC, (b) switching sequence for $d > 0.5$ of FDBC.

The output voltage, output current, input current and voltage stress across the switches and diodes is given by,

$$v_o = v_{C1} + v_{C2} - v_{in} \tag{1}$$

$$i_o = v_o/R \tag{2}$$

$$i_{in} = i_{L1} + i_{L2} - i_o \tag{3}$$

$$v_s = v_{C1} + v_{C2} = v_o - v_{in} \tag{4}$$

A. LARGE SIGNAL MODEL

Mode 1 (0 to t_1): When S_1 and S_2 are turned ON. Fig. 3(a) shows the circuit during mode 1. L_1 and L_2 are charging, and C_1 and C_2 are discharging. State-space representation of mode 1 is represented by,

$$\dot{x} = A_{m1}x + B_{m1}u \Rightarrow \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{RC_1} & 0 & \frac{-1}{RC_1} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{RC_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \times \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{RC_1} \\ \frac{1}{L_2} \\ \frac{1}{RC_2} \end{bmatrix} v_{in} \tag{5}$$

$$y = C_{m1}x + D_{m1}u \Rightarrow [V_o] = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + [-1]\, V_{in} \tag{6}$$

Mode 2 (t_1 to t_2): When S_1 is turned ON, and S_2 is turned OFF. Fig. 3(b) shows the circuit during mode 2. L_1 and C_2 are charging while L_2 and C_1 are discharging. State-space representation of mode 2 is represented by (7) and (8).

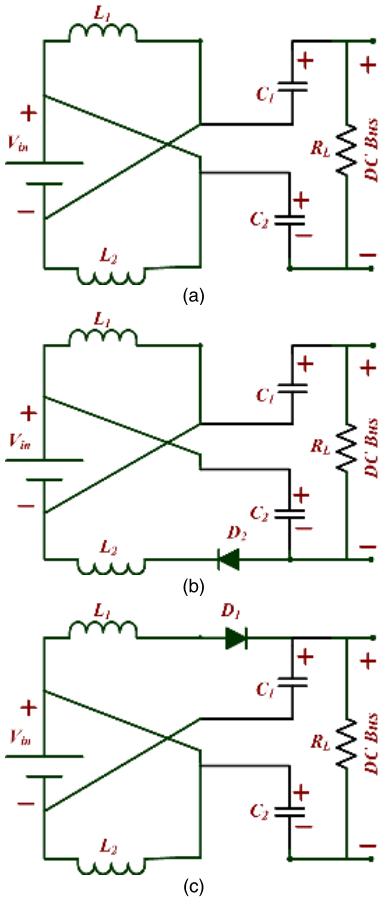


FIGURE 3. FDBC equivalent circuit (a) mode 1, (b) mode (2), (c) mode 3.

$$\dot{x} = A_{m2}x + B_{m2}u \Rightarrow \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{RC_1} & 0 & \frac{-1}{RC_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{-1}{RC_2} & \frac{1}{C_2} & \frac{-1}{RC_2} \end{bmatrix} \times \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{RC_1} \\ \frac{1}{L_2} \\ \frac{1}{RC_2} \end{bmatrix} v_{in} \tag{7}$$

$$y = C_{m2}x + D_{m2}u \Rightarrow [V_o] = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + [-1]\, V_{in} \tag{8}$$

Fig. 3(c) shows the circuit during mode 3. L_2 and C_1 are charging while L_1 and C_2 are discharging. State representation of mode 3 is also likewise obtained. The averaged

large-signal model is obtained using the circuit averaging method in [35]. In FDBC $L_1 = L_2 = L$ & $C_1 = C_2 = C$, Therefore the averaged large-signal model of floating dual boost converter is,

$$\dot{x} = A_{ave}x + B_{ave}u \Rightarrow \begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{i}_{L2} \\ \dot{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-\overline{d}_1}{L} & 0 & 0 \\ \frac{\overline{d}_1}{C} & \frac{-2}{RC} & 0 & 0 \\ 0 & 0 & 0 & \frac{-\overline{d}_2}{L} \\ 0 & 0 & \frac{\overline{d}_2}{C} & \frac{-2}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \\ \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} v_{in} \tag{9}$$

$$y = C_{ave}x + D_{ave}u \Rightarrow [v_o] = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + [-1]\, v_{in} \tag{10}$$

B. STEADY STATE VOLTAGE GAIN

Averaged large-signal model = Steady-state model + Small-signal model

$$x = X + \hat{x} \tag{11}$$

$$y = Y + \hat{y} \tag{12}$$

where X and Y are the steady-state model $\hat{x}$ and $\hat{y}$ is a small signal model.

$$\left.\begin{aligned} &v_{in} = V_{in} + \hat{v}_{in};\ v_o = V_o + \hat{v}_o;\ i_{L1} = I_{L1} + \hat{i}_{L1} \\ &i_{L2} = I_{L1} + \hat{i}_{L1};\ v_{C1} = V_{C1} + \hat{v}_{C1};\ v_{C2} = V_{C2} + \hat{v}_{C2} \\ &d_1 = D_1 + \hat{d}_1;\ d_2 = D_2 + \hat{d}_2 \end{aligned}\right\} \tag{13}$$

During steady-state $x = X$, $y = Y$ and $\dot{X} = AX + BY = 0$, therefore the voltage gain is given as,

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{1}{1 - D_1} + \frac{1}{1 - D_2} - 1 = \frac{1 + D}{1 - D} \quad (Where\ D_1 = D_2 = D) \tag{14}$$

The voltage gain of FDBC is given by (14).

C. LINEARIZED SMALL SIGNAL MODEL

The small-signal model is obtained by substituting (13) in the averaged large-signal model ((9) and (10)).

$$\begin{bmatrix} \hat{i}_{L1} + I_{L1} \\ \hat{v}_{C1} + V_{C1} \\ \hat{i}_{L2} + I_{L2} \\ \hat{v}_{C2} + V_{C2} \end{bmatrix} = P \begin{bmatrix} \hat{i}_{L1} + I_{L1} \\ \hat{v}_{C1} + V_{C1} \\ \hat{i}_{L2} + I_{L1} \\ \hat{v}_{C2} + V_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \\ \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} (\hat{v}_{in} + V_{in}) \tag{15}$$

where, (16) as shown at the bottom of the next page.

The multiplication of two small signals yields a minimal value, thus

$$\hat{x}.\hat{x}\ or\ \hat{y}.\hat{y}\ or\ \hat{x}.\hat{y} = 0 \tag{17}$$

Using $\dot{X} = AX + BY = 0$ and (17) in (15) and (16) results in,

$$\dot{\hat{x}} = A\hat{x} + B_1\hat{u}_1 + B_2\hat{u}_2 \Rightarrow \begin{bmatrix} \dot{\hat{i}}_{L1} \\ \dot{\hat{v}}_{C1} \\ \dot{\hat{i}}_{L2} \\ \dot{\hat{v}}_{C1} \end{bmatrix} = A \begin{bmatrix} \hat{i}_{L1} \\ \hat{v}_{C1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \\ \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} \frac{V_{C1}}{L} \\ \frac{I_{L1}}{C} \\ \frac{V_{C2}}{L} \\ \frac{I_{L2}}{C} \end{bmatrix} \hat{d} \tag{18}$$

$$\hat{y} = C\hat{x} + D_1\hat{u}_1 + D_2\hat{u}_2 \Rightarrow \hat{v}_o = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} \hat{i}_{L1} \\ \hat{v}_{C1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \end{bmatrix} + [-1]\, \hat{v}_{in} + [0]\, \hat{d} \tag{19}$$

The linearized small-signal model of FDBC is represented by (18) and (19). The voltage mode controller for the FDBC is designed based on this small-signal model of the FDBC.

TABLE 1. Components constraint of FDBC.

Components	$I_{average}$	V_{max}
Transistor	$(i_{in}$-$i_o)/2$	v_{out}-v_{in}
Diode	i_o	v_{out}-v_{in}
Inductor	$(i_{in}$-$i_o)/2$	–
Capacitor	0	v_{out}-v_{in}

D. PARAMETER DESIGN

In this topology, the switches have to handle lower current and voltage rating while the size of the input inductances and output capacitances decreases due to the interleaving concept. Table 1 shows the components constraint [35]. The inductor value is calculated using (20) [35],

$$L = \frac{2v_{in}}{\Delta i_{in} f_s}(D - 0.5) \tag{20}$$

The capacitor value is calculated using (21) [35],

$$C = \frac{2i_o}{\Delta v_o f_s}(D - 0.5) \tag{21}$$

E. TRANSFER FUNCTION

It is essential to derive the small-signal transfer function of the converter in order to design a controller for the same. The generalized transfer function equation is given as,

$$Y(s) = C(sI - A)^{-1}BU(s) + DU(S) \Rightarrow \frac{Y(s)}{U(s)} = C(sI - A)^{-1}B + D \tag{22}$$

The transfer functions of FDBC are given as,

$$\frac{\widehat{v}_o(s)}{\widehat{v}_{in}(s)} = C(sI - A)^{-1}B_1 + D_1 @ \widehat{d} = 0 \tag{23}$$

$$\frac{\widehat{v}_o(s)}{\widehat{d}(s)} = C(sI - A)^{-1}B_2 + D_2 @ \widehat{v}_{in} = 0 \tag{24}$$

The input to output transfer function is represented by (23), and the control to output transfer function is represented by (24). Substituting the value of A, B_2, C, D_2 from (18) and (19) in (24),

$$\frac{\widehat{v}_o(s)}{\widehat{d}(s)} = \frac{-3.467e^5s^3 + 4.469e^9s^2 + 2.433e^{11}s + 1.28e^{16}}{s^4 + 533.3s^3 + 5.685e^6s^2 + 1.497e^9s + 7.87e^{12}} \tag{25}$$

The control to output transfer function for the designed FDBC is represented by (25).

IV. CONTROLLER DESIGN

Proportional integral derivative (PID) controller is one of the most common control loop mechanism present and is extremely mainstream in industrial control systems. Generally, PI type controllers are used for the DC-DC converter. When incorporated with a DC-DC converter as a voltage controller, a PID controller attempts to reduce the error between the sensed output voltage and the reference voltage by outputting a control voltage that can adjust the duty cycle accordingly. PI controller is linear. However, DC-DC converters are non-linear. Therefore the design of a PI controller for a DC-DC converter is realized using a linearized small-signal model of the converter. Fig. 4 shows a closed-loop structure for the designed FDBC. In Fig. 4, V_{ref} is the steady-state output voltage; v_c is the control voltage that can adjust the duty cycle (d). It is evident from the figure that the PI controller addresses the small-signal disturbances arising at the output side and reduces it to zero by controlling the duty cycle.

Design of PI controller involves the calculation K_p and K_i. The most incorporated method to tune a PI controller is the Ziegler-Nichol's method as it does not involves complex modelling of the plant and also handles problems like

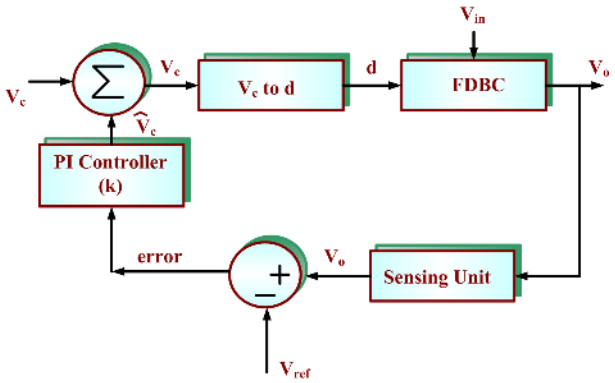


FIGURE 4. Closed loop system of FDBC.

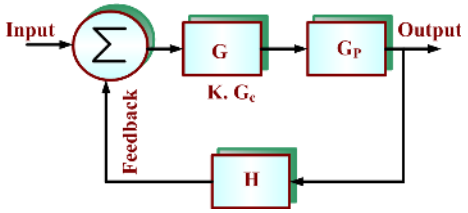


FIGURE 5. Block diagram of a closed loop plant.

uncertainty, modelled dynamics, etc. The drawback of this method is that it is tedious and time-consuming as it is a trial and error method. Other techniques like bode plot and root locus techniques are also popular but require the mathematical modelling of the system. In the case of FDBC, the small-signal transfer function has a zero on the right-hand side of the S plane, making it a minimum phase system. Bode plot will work for non-minimum phase systems only, therefore, cannot be used to design a PI controller for FDBC.

Root locus technique was not very popular before the advent of powerful mathematical tools like MATLAB, Octave etc. The reason being, this method is very computationally intensive and requires complex mathematical calculations which increase the room for error. To understand this technique, let us take a general block diagram of a closed-loop plant, as shown in Fig. 5. Where G_p is a plant

$$P = \begin{bmatrix} 0 & \frac{-(D_1 + \widehat{d}_1)}{L} & 0 & 0 \\ \frac{-(D_1 + \widehat{d}_1)}{C} & \frac{-2}{RC} & 0 & 0 \\ 0 & 0 & 0 & \frac{-(D_2 + \widehat{d}_2)}{L} \\ 0 & 0 & \frac{-(D_2 + \widehat{d}_2)}{C} & \frac{-2}{RC} \end{bmatrix}$$

$$\left[\widehat{v}_o + V_0\right] = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} \widehat{i}_{L1} + I_{L1} \\ \widehat{v}_{C1} + V_{C1} \\ \widehat{i}_{L2} + I_{L1} \\ \widehat{v}_{C2} + V_{C2} \end{bmatrix} + [-1]\,(\widehat{v}_{in} + V_{in}) \tag{16}$$

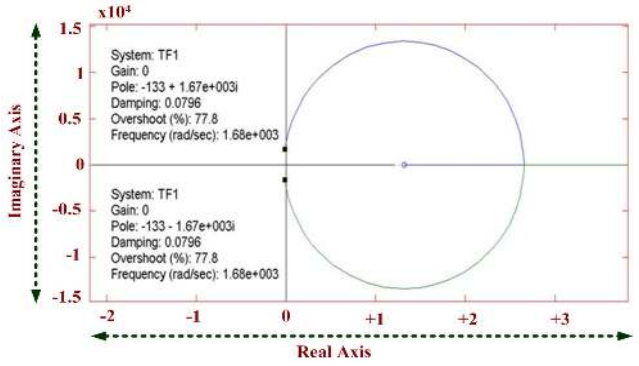


FIGURE 6. Root locus of the plant (FDBC).

transfer function, G is controller transfer function (KG_c), K is controller gain, G_c is the pole-zero structure of the controller, H is the feedback transfer function.

$$TF_c = \frac{n_c}{d_c} = \frac{KG_cG_p}{1 + KG_cG_pH} \tag{26}$$

where TF_c is the closed-loop transfer function of the plant. G_c is given by,

$$G_c = \frac{(s+a)}{s} \tag{27}$$

$$a = \frac{K_i}{K_p} \tag{28}$$

$$K_p = K \tag{29}$$

$$K_i = aK \tag{30}$$

Now to obtain the location of the pole of TF_c, d_c has to be equated to zero,

$$1 + KG_cG_pH = 0 \tag{31}$$

Now for a given value of G_c, G_p, H, if we vary K from then the location of the poles of TF_c will vary accordingly. Values of K_p and K_i for the voltage controller of FDBC is obtained using the root locus technique. Followings are the steps to design the controller for FDBC using root locus technique.

The plant is the FDBC, and the transfer function of the plant from the control point of view will be the control voltage gain as in (25). The transfer function of the plant is, (32), as shown at the bottom of the next page.

Fig. 6 shows the root locus of G_p. Each pole location, shown and consists of two poles. The close loop transfer function (TF_c) is calculated using (23). G_p is the plant transfer function. Since unity feedback is considered in this case, therefore H is taken as unity. As the designer has the liberty to choose the pole location, the value of K and G_c are obtained accordingly. The closed-loop transfer function of FDBC for the chosen pole location is given as, (33) shown at the bottom of the next page.

The root locus of TF_c is shown in Fig. 7(a). The two poles marked in the figure are the poles which will be varied to obtain a desirable step response. It is seen that a fifth pole in introduced in TF_c when compared to the open-loop transfer function, this pole is added due to the integrator. It is also seen

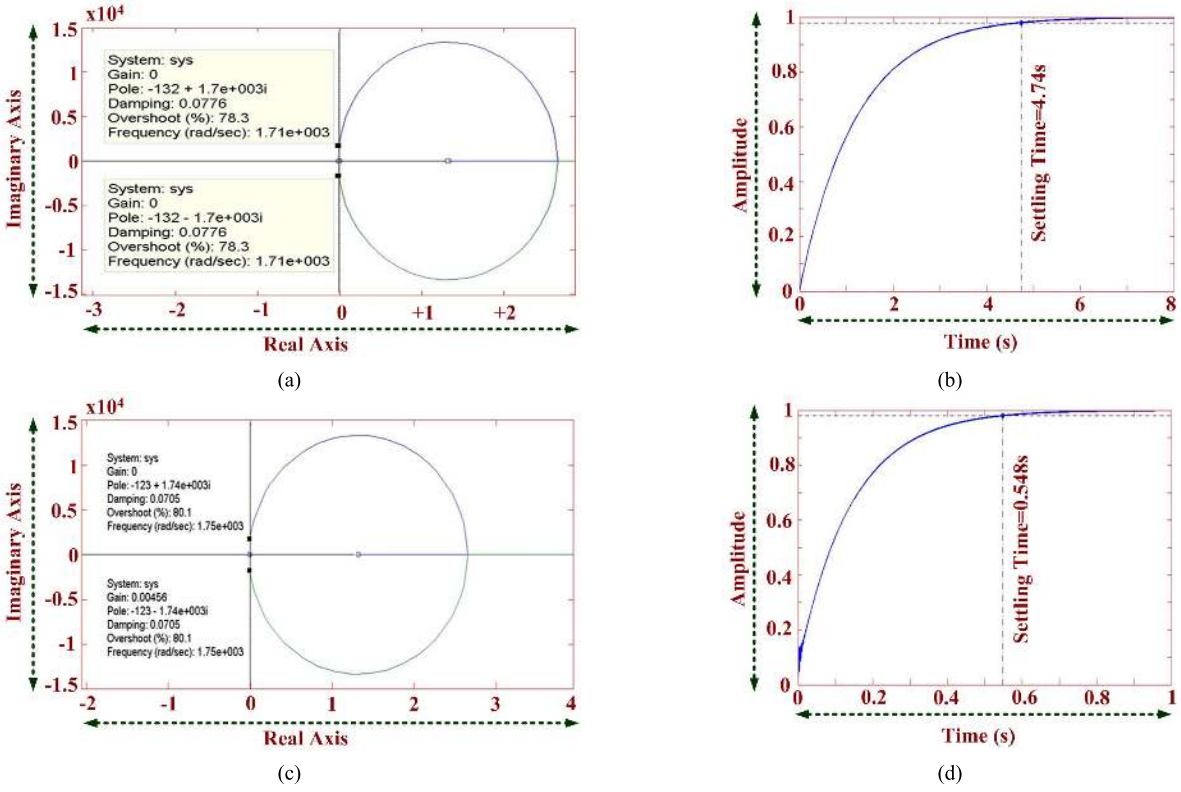


FIGURE 7. Root locus and response (a) root locus of TF_c, (b) step response of TF_c, (c) root locus for the new TF_c, (d) step response of the new TF_c.

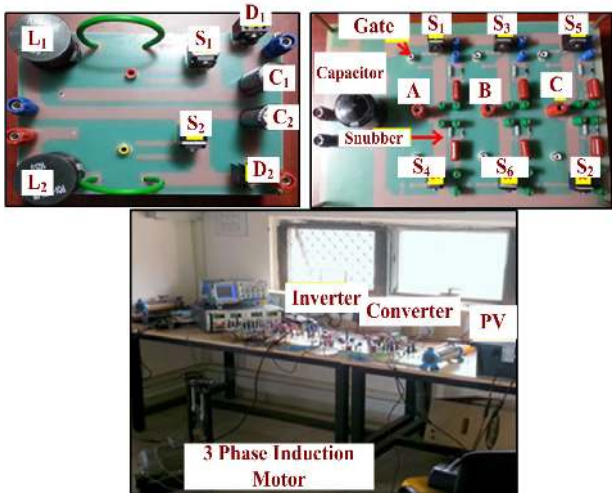


FIGURE 8. Experimental setup of proposed work.

TABLE 2. Hardware specifications.

FDBC Specifications	
Input Supply (PV array)	140 Volts, 8 Amps (DC).
Required Output (Max)	495 Volts, 1.5 Amps (DC)
Steady state duty cycle=56%	56%
Switch part number	IPA60R199CP (Mosfet)
Diode part number	STTH806
Inductor rating/Inductor part number	560 µH/PCV-2-564-08L
Capacitor rating	120µF, 600V
VSI Specifications	
Input Supply(FDBC)	495 Volts, 1.5 Amps (DC).
Required Output (Max)	400 Volts (rms), 1 Amps (rms) (AC)
DC-Link Capacitor rating	1000uF, 500 Volts
Switch part number	FGA25N120ANTD (IGBT)
3-phase Induction Motor (Squirrel Cage)	
Ratings	400 Volts, 1.8 Amps, 0.72 kW
Frequency	50 Hz
RPM	1415
PF	0.8

in the root locus of TF_c. The step response of TF_c is obtained to validate the performance of the controller with the desired performance requirement. Fig. 7(b) shows the step response of TF_c.

Obtain new poles- From the step response, it can be inferred that the settling time of the controller is high. Thus we to move the poles from its initial position to a new position along the root locus. However, the pole position should be selected such that it is on the left-hand side of the s-plane. After multiple iterations, the desirable step response was obtained for FDBC.

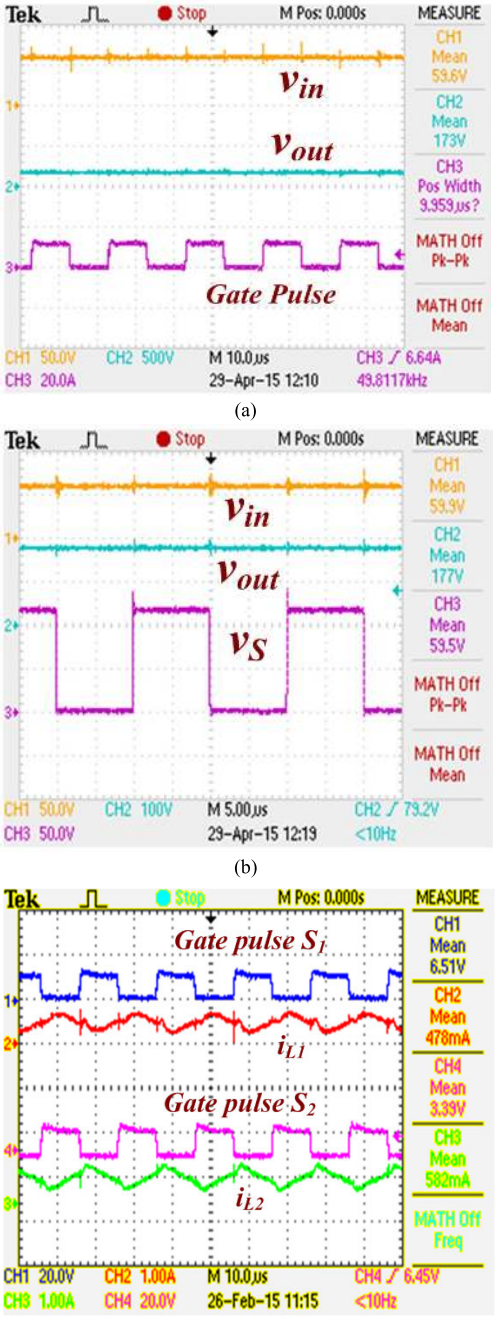


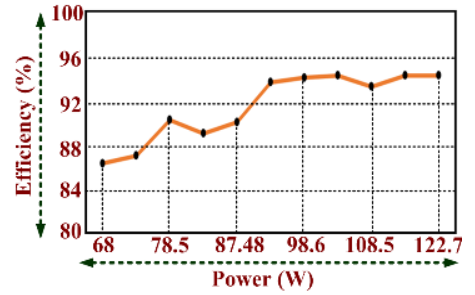
FIGURE 9. The output waveform of FDBC in hardware, (a) input voltage, output voltage and duty cycle, (b) input voltage, output voltage and voltage stress across switches, (c) inductor current.

The new closed-loop transfer function (TF_C) is expressed as, (34) shown at the bottom of this page.

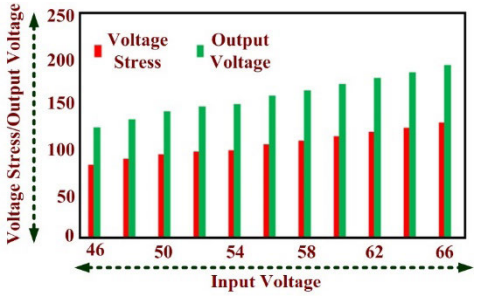
$$G_p = \frac{\widehat{v}_o(s)}{\widehat{d}(s)} = \frac{-3.467 \times 10^5 s^3 + 4.469 \times 10^9 s^2 + 2.433 \times 10^{11} s + 1.28 \times 10^{16}}{s^4 + 533.3 s^3 + 5.685 \times 10^6 s^2 + 1.497 \times 10^9 s + 7.87 \times 10^{12}} \tag{32}$$

$$TF_c = \frac{-1.761 s^4 + 2.252 \times 10^4 s^3 + 3.506 \times 10^6 s^2 + 6.5141 \times 10^{10} s + 6.501 \times 10^{12}}{s^5 + 531.4 s^4 + 5.709 \times 10^6 s^3 + 1.501 \times 10^9 s^2 + 7.939 \times 10^{12} s + 6.501 \times 10^{12}} \tag{33}$$

$$TF_c = \frac{-14.59 s^4 + 1.866 \times 10^5 s^3 + 2.905 \times 10^7 s^2 + 5.397 \times 10^{11} s + 5.387 \times 10^{13}}{s^5 + 518.7 s^4 + 5.872 \times 10^6 s^3 + 1.526 \times 10^9 s^2 + 8.41 \times 10^{12} s + 5.3871 \times 10^{13}} \tag{34}$$

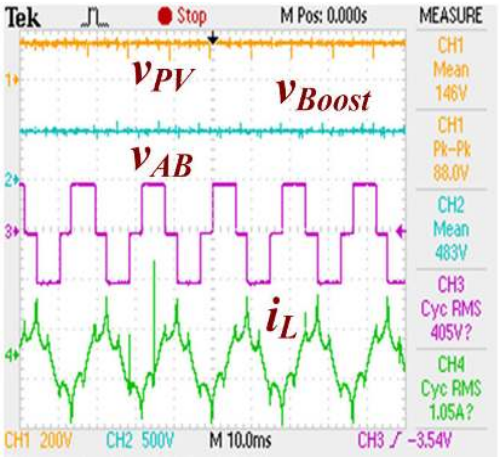


(a)

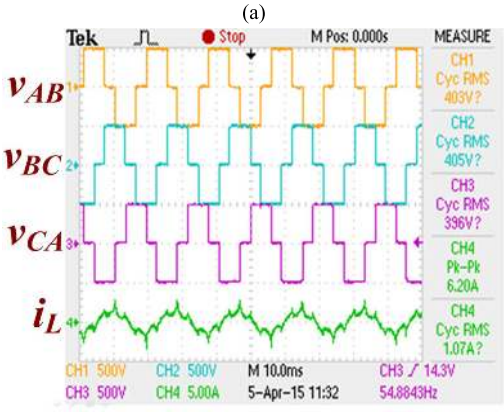


(b)

FIGURE 10. Performance graph of FDBC, (a) power VS efficiency curve, (b) bar graph representing output voltage and voltage stress of switches.



(a)



(b)

FIGURE 11. Output waveform of the entire system (a) output waveform of the PV voltage, FDBC voltage, VSI voltage and current, (b) motor output waveform.

Fig. 7(c) shows the root locus for the new TF_c. The new pole locations are highlighted in the root locus. Fig. 7(d)

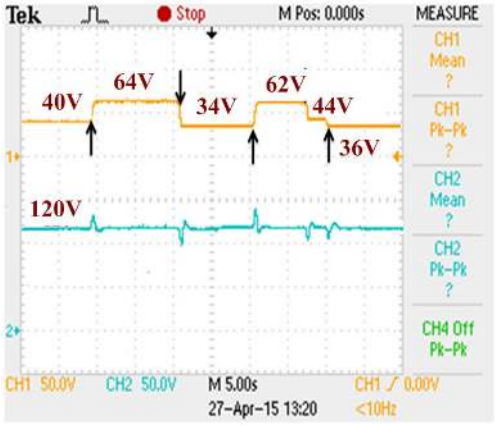


FIGURE 12. Closed-loop output waveform of FDBC in hardware.

shows the step response of the new TF_c. It can interfere that the settling time of the system has reduced from 4.74 sec to 0.548 sec. Thus, the pole position can be varied accordingly to obtain the desired response. For the selected pole location, the value of K is obtained, and K_p (1.2) and K_i (0.25) are calculated using (29) and (30) for the voltage controller of FDBC. Realizing the above steps requires complex and long mathematical computation; thus, these steps are computed using MATLAB.

V. HARDWARE SPECIFICATIONS

The specifications of the setup are given in Table. 2, the Experimental setup is shown in Fig. 8. Fig. 9(a) shows the input voltage, output voltage and duty cycle and Fig. 9(b) shows the input voltage, output voltage and voltage stress across the switch of the FDBC in hardware. Fig. 9(c) highlights the inductor current for both the modules of FDBC. Fig. 10(a) shows the plot for input power VS efficiency for the fabricated FDBC. Fig. 10(b) shows the bar graph of output voltage and voltage stress across the switches for a specific input voltage. It is inferred from the plot that this topology offers low voltage stress across its switches.

The output waveform of the entire system is shown in Fig. 11(a). It highlights the PV voltage, the output voltage of the FDBC, motor phase to phase voltage and motor phase current. Fig. 11(b) shows all the three-phase to phase voltages and the phase current of the motor. It is observed that $V(line)_{rms} = 0.81V_{in}$, $V_{in} = 483\ V$, $V(line)_{rms} = 483^{*}0.81 = 396\ V$ for the 180° mode three-phase inverter used.

As discussed earlier, the PV output voltage as functions of time or instead function of irradiance, which is a function of time. The output voltage of the PV fed FDBC when driving a constant load has to be maintained constant despite the variations in PV voltage. The voltage mode controller is designed for this purpose. The hardware results of the closed-loop operation of FDBC are shown in Fig.12. The reference voltage is set at 120V (V_{ref}). From Fig. 12 it is observed that the output is maintained constant at the reference value.

VI. CONCLUSION

A PV based system using floating dual boost converter (FDBC), a three-phase voltage source inverter (VSI) and a three-phase squirrel cage induction motor (pump) are designed and implemented. It has been observed that the DC-link voltage obtained from the DC-DC converter varies with solar input voltage variation. So, it is essential to control either the DC-link voltage of the inverter or the output voltage of the inverter to obtain better performance. Hence, a voltage mode controller has been designed and implemented to keep the output of the DC-DC converter constant. The DC-DC converter is tested in closed-loop for different input voltage, and the performance of the voltage mode controller has been verified.

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