IMPLEMENTATION OF MULTI-VALUED LOGIC GATES USING FULL CURRENT-MODE CMOS CIRCUITS

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ABSTRACT

In this paper, a novel multi-valued logic gate set implemented as current-mode CMOS circuits. The gate set consists of *min, max, inverter, literal* and its *complement,* the latter two based on a novel current-mode threshold scheme. They are shown to exhibit superior static and dynamic behaviors and consume less area compared to previous designs.

I. INTRODUCTION

The current-mode design has been attractive due to its simplicity, superior dynamic behavior at low voltage swing with a cost of static power dissipation. Although some current-mode multi-valued logic, (MVL), studies are proposed for I^2L, [2]-[3], for CCD, [4], and for CMOS, [5]-[6], most studies prefer using voltage, [1], for switching a desired level of current, [5]-[6]. Due to technology dependency, [5], most studies employ different disjunctives instead of max gate. However, voltage use leads larger area and oscillatory behavior in higher radix.

In this study a novel current-mode threshold operation scheme is proposed to implement (complementary) literal circuit to be used together with other propositional MVL gates, such as min and max.

II. BACKGROUND AND NOTATION

Consider an r-valued m-variable function $f(X)$ where $X=\{x_1, x_2,\ldots, x_m\}$ and each x_i takes on a value from the set $R=\{0, 1,\ldots, r\text{-}1\}$ where r is the radix. The function $f(X)$ is a mapping $f : R^m \to R$. Therefore, there are r^{r^m} possible different functions, [5].

In current-mode MVL, (CM-MVL), logic levels are represented by current levels in terms of a *base current* value, I_b, where it is taken to be 10μA in this study. Thus, level 0 is associated with the value of null, level 1 is associated with I_b= 10μA and so on. The logic level k corresponds to the continuous interval of x such that $k: \{x \mid (k-0.5)I_b \le x < (k+0.5)I_b\}$.

Definition 2.1- A *min* operator is defined as

$$\min(x,y) = x \cap y \tag{1}$$

Definition 2.2- A *max* operator is defined as

$$\max(x,y) = x \cup y \tag{2}$$

Definition 2.3- The *complement* of x is defined as

$$\bar{x} = r - 1 - x \tag{3}$$

Definition 2.4- The *literal* is defined as

$$z[a,b] = {}^{a}x^{b} = \begin{cases} r-1 & \text{if } a \le x \le b \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

The *complementary-literal*

$$z[a,b] = \overline{{}^{a}x^{b}} = \begin{cases} r-1 & \text{if } x \le a \text{ or } x \ge b \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

From (1) and (4) or (5), a *k-valued literal* can be formed as $z[a,b] = k \cap z(a,b)$.

Definition 2.5- A *k-valued product term* in terms of literals is defined by

$$P_k : \bigcap_{i \in \{1,2,\ldots,m\}} g(x_i) = k \tag{6}$$

where the operation '$\cap$' refers to min operation over *unary operation*, $g(x_i)$, such as a *literal*, unless otherwise stated, i.e.,

$$P_k : [\, k_1 \cap {}^{a1}x_1^{b1} \,] \cap [\, k_2 \cap {}^{a2}x_2^{b2} \,] \ldots = k \tag{7}$$

Definition 2.6- A *multi-valued function* can be expressed in terms of the product terms as, [7].

$$f(x_1, x_2, \ldots, x_m) = \bigcup_{j \in R} P_j \tag{8}$$

where the '$\cup$' implies max operator.

III. BASIC CIRCUIT ELEMENTS

III-i Primitives:

1) Sum: Basically, a sum circuit is a node in the circuit, where some currents enter and/or some currents leave.

2) Constant: Logic levels represent constants in CM-MVL. They can be generated with current sources using

either enhancement mode p-type or n-type transistors, depending on the current sourcing or sinking action desired.

3) Current-Mirror: They are used for generating single or multiple-replica of currents. An n-type current mirror and its symbol are shown in Fig.1 where M_d stands for diode-connected transistor while M_m for mirror transistor.

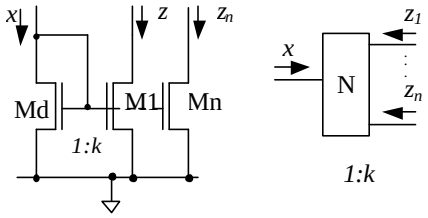


Fig.1: n-type current mirror and its symbol

A current can be redirected by cascading n- and p-type mirrors, which allows one to copy multiple sinking currents as shown in Fig.2 where $z_1,\ldots,z_n$ can be any multiple of x and PMOS transistors are of aspect ratio of (W/L)=3.5.

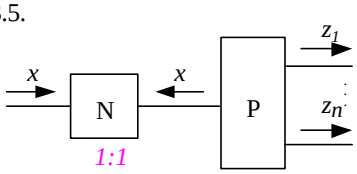


Fig. 2: Multiplying and redirecting a current

4) Input and Output Circuits: A diode-connected transistor is used as the input circuit of a gate as well as the output circuit, with aspect ratio of (W/L)=1.

III-ii Secondary Blocks:

The gate circuits are formed by using *truncated difference* operation, [5], defined by

$$x \,\Xi y = \begin{cases} x - y & \text{if } x \geq y \\ 0 & \text{otherwise} \end{cases} \qquad (9)$$

It can be shown that

$$\min(x,y) = x - (x \,\Xi\, y) = x \,\Xi\, (x \,\Xi\, y)$$

$$\max(x,y) = x + (y \,\Xi\, x) = x \,\Xi\, (y \,\Xi x) \qquad (10)$$

The truncated difference can be realized using the circuit with DC characteristics shown in Fig.3,

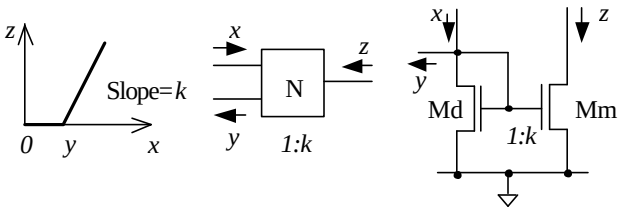


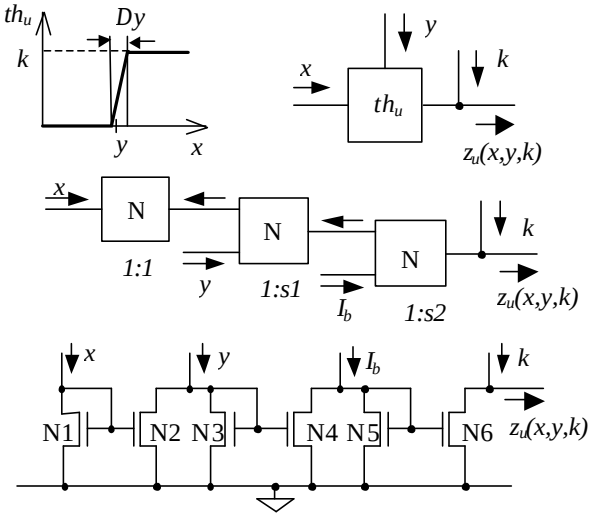
Fig.3: DC transfer characteristics of truncated difference operation and its diagrams

Based on the truncated difference operation, a novel current-mode *threshold* operation can be implemented.

The *k-valued upper and lower threshold* operations, z_u and z_l, can be defined, respectively as

$$th_u: \quad z_u(x,y,k) = \begin{cases} k & \text{if } y \geq x \\ 0 & \text{otherwise} \end{cases}$$

$$th_l: \quad z_l(x,y,k) = \begin{cases} k & \text{if } y \leq x \\ 0 & \text{otherwise} \end{cases} \qquad (11)$$



Trans.	N1,3	N2	N4	N5	N6
W/L	1/1	1/1+ε	s1/1	1/s2	s2/1

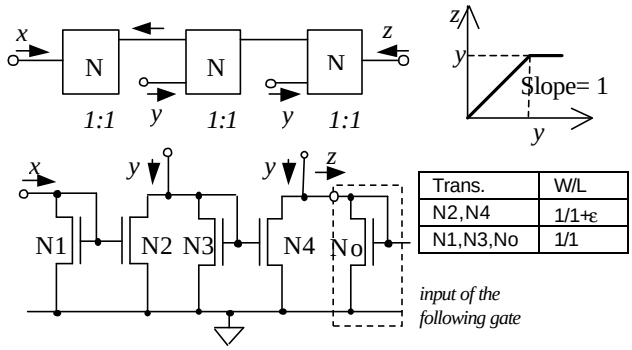
e is between 0.1 and 0.2 used for eliminating the effects of transistor mismatching and channel modulation for optimum DC characteristics.

Fig. 4: The *upper-threshold* circuit DC characteristics, symbol, proposed structure, and circuit schematics.

The *lower-threshold* characteristics can be obtained by flipping horizontally the upper-threshold characteristic by interchanging x and y. In this study, $s1$ is chosen to be equal to I_b/DI while $s2 \geq \sqrt{r}$.

IV. IMPLEMENTATION OF GATES

Based on the building blocks given in section III, MVL gates can be implemented.



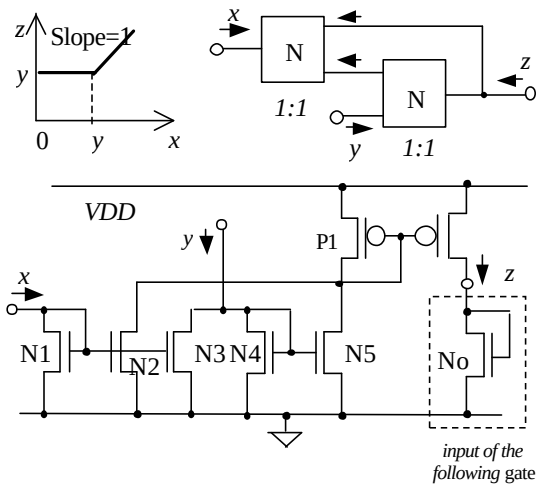
Trans.	W/L
N2,N4	1/1+ε
N1,N3,No	1/1

Fig.5: DC transfer characteristics of max(x,y) operation, and proposed max(x,y) circuit

Although descriptions are straightforward, the gate implementations are subject to transistor mismatching, the effect of which can be reduced by taking larger transistors in designs. However, it is desirable to develop a minimum-size transistor profiles for estimating optimum DC and transient behavior of each gate set on primary and secondary structures.

1) Min Gate: This operator can be realized using Eqn. 10, as shown in Fig.5.

2) Max Gate: Using the complement definition, a max operation, $z=max(x,y)$, with a desired DC transfer characteristic can be constructed as shown in Fig.6.



Trans.	N1,4, No	N2,3,5	P1,2
W/L	1/1	1/1+ε	3.5/1

Fig.6: DC transfer characteristics of max(x,y) operation, and proposed *max(x,y)* circuit

3) Inverter: An MVL inverter can be designed as a truncated difference circuit as illustrated in Fig.7,

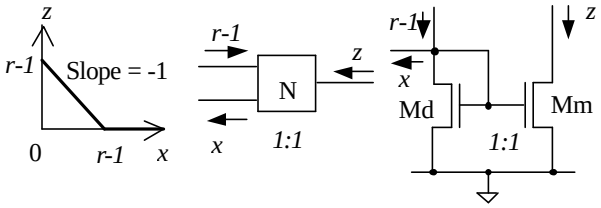


Fig.7: DC transfer characteristics of inverter and its circuit diagram

4) Literal: A literal circuit performs *window comparator* function for the input current and generates an output between two logic levels of input. A *k*-valued literal circuit and its complement can be implemented by using two upper-threshold circuits cascaded with the same design transistor dimensions, as shown in Fig. 8, where due to space limitation only the block diagram is given,

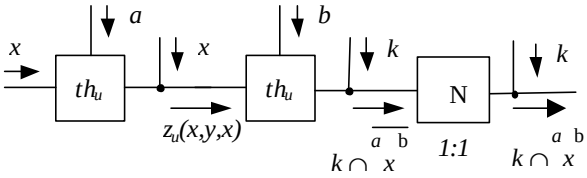


Fig.8: Literal structure.

V. SIMULATION RESULTS

Fully extracted outputs of designed gates are simulated with HSPice using AMI-SC's 1µm technology (level 49) parameters for 2.7V supply voltage.

2) Min Gate: DC and transient simulation results of the proposed min gate are illustrated in Fig. 9. It is seen that radix-8 operation can be achieved with given transistor aspect ratios considering logic level definitions.Fig.9,

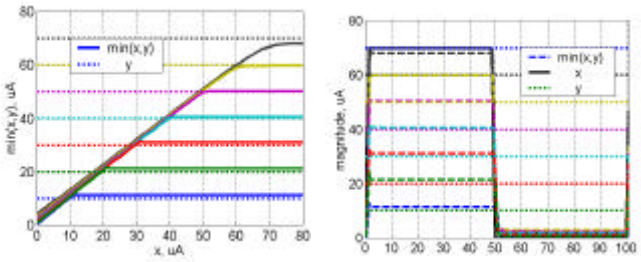


Fig. 9: Simulation results of min(x,y) gate.

2)Max Gate: DC and transient simulation results of the proposed max gate are illustrated in Fig. 10. As min gate, it is seen that a radix-8 operation can be achieved with given transistor aspect ratios.

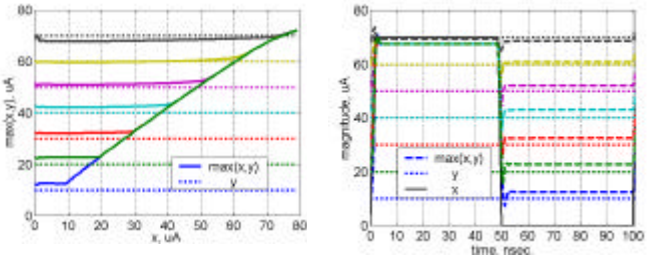


Fig. 10: Simulation results of max(x,y) gate.

Due to different current-paths of *x* and *y*, the gate exhibits some overshoot and undershoot which can be remedied with proper current-mirror structures in the path of *x* from output to input.

3)Literal(s): An *r-valued* system has $n_r = \frac{r.(r+1)}{2}$ literals. The literals of type *{z[a,a] }* are called *dot-literals*, while for the case of a^1b, the literal is called *interval literal* where $a,b \hat{I} R$. Fig. 11 illustrates DC and transient simulation results of some literals and their complements of *x* where the min operation is denoted with '.'.

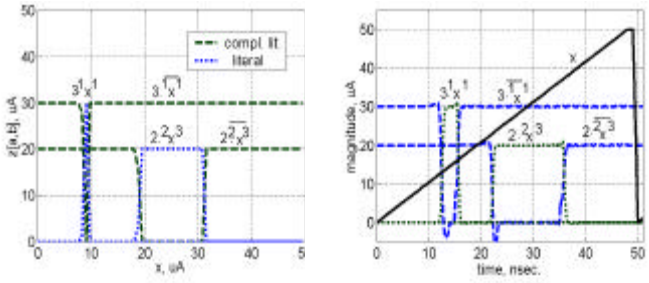


Fig. 11: Simulation results of some literals of *x*.

VI. COMPARISON WITH PREVIOUS DESIGNS

Most comprehensive technology independent MVL design studies in CMOS, [5]-[6], incorporate current-mode operation with voltage-mode binary coding. Due to its simplicity, [5], the *truncated sum* operation defined by

$$tsum(x,y):\ x \oplus y = \min(x+y, r-1) \qquad (12)$$

is employed as disjunctive. Although the scheme in [5] is simple, voltage-mode use imposes considerable restrictions on higher radix design. Below we demonstrate inefficiencies of conventional voltage use in MVL design in terms of DC behavior and consumed area associated with it.

1- Design Cost: The cost can be determined by the transistor count per gate. A cost comparison with regard to transistor count of this study and [5] is given in Table 1, considering that inputs sink and outputs source, and omitting the biasing circuits,

Table 1. Transistor counts

	This study	Ref.[5]
Min	4	7
Literal	16	12
Compl. Literal	14	12
Truncated Sum	*not available*	11
Max	7	*not available*

Another meaningful design cost comparison may be given in terms of the consumed active area, which is essentially determined by desired DC operation of a given gate for the same design parameters. A typical comparison is presented in Table 2 without considering biasing circuitries for given technology, in which A_0 is the total area of output block of the gate.

Table 2. Active area, (μm)^2, without bias circuits

	This study	Ref.[5]
Min	4	$10+A_0$
Literal	33	$23.5+A_0$
Compl. Literal	31	$23.5+A_0$
Max	10	*not available*
Truncated Sum	*not available*	$16+(r-1)+1.5A_0$

The maximum linear operation output current that determines the maximum radix is considerably limited in the previous designs. It can be shown that the output block area increases *exponentially* when the radix increases in the old designs using voltage to control the output current. The design topology proposed in this study eliminates this restriction.

2- DC Behavior:

2-i Previous Designs: Most voltage-controlled current-mode MVL design schemes, e.g., [4] and [5] use the basic structure shown in Fig. 12.

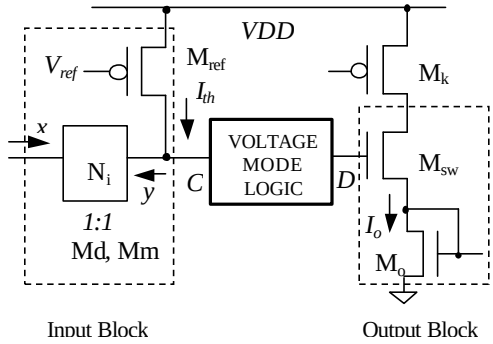


Fig.12: General structure of a voltage-controlled MVL implementation

In Fig. 12, I_o is the desired output current and M_o is the input transistor of following gate. M_{sw} is the NMOS or PMOS switching transistor, M_k is a transistor supplying the effective output current, I_o.

When M_{sw} is on, it operates in linear region providing the current I_o. The transistor M_{sw} conducts if

$$VDD - V_{gs,o} \geq V_{th,sw}$$

where subscript '*o*' denotes the transistor M_o and 'sw' denotes M_{sw} both taken NMOS. An *upper bound* for output current is given by

$$I_o < \frac{\left[VDD - (VTO_o + V_{th,sw})\right]^2 .KP_o}{2\left(\frac{L}{W}\right)_o} \qquad (13)$$

where VTO_o, is the zero-bias threshold voltage of M_o. $V_{th,sw}$ is the threshold voltage of M_{sw} and *KP* is the process transconductance.

However the *desired operation* of the structure is to be determined by M_{sw}. The upper-bound of controllable ouput current range is determined by triode-mode operation range of M_{sw}. The lower bound for its dimension is given by

$$\left(\frac{W}{L}\right)_{sw} \geq \frac{2I_o}{\left[VDD - \sqrt{\frac{2I_o}{(W/L)_o.KP_o}} - (VTO_o + V_{th,sw})\right]^2 .KP_{sw}} \qquad (14)$$

where $b = KP(W/L)$ is the *transconductance*. As can be seen from eqn.(14), dimensions of M_{sw} is lower bounded

and increases severely as the ouput current approaches the maximum output current given by eqn.(13). Moreover, the situation becomes worse with body-bias effect. The fact that M_k has to operate in saturation as current source puts forward larger $(W/L)_{sw}$ values. Hence, the output block area, which is directly proportional to $ß_o+ß_{sw}$, becomes very large. A *minimum area* of the output block is achieved with resized M_o by a constant factor $(1+d)$. Therefore, succeeding *gates have to be scaled up* with the same factor, which implies an *exponential increase in total area of the design by*$(1+d)$. It can be shown that $d=3.1$ for no-body-biased M_{sw} while $d=1.8$ for body-biased M_{sw}. The minimum values of $(W/L)_{sw}$ can be calculated from

$$\left(\frac{W}{L}\right)_{sw} \geq \frac{KP_o.(W/L)_o}{(1+d).\left[1-\sqrt{\frac{1}{1+d}}\right]^2.KP_{sw}} \qquad (15)$$

2-i Proposed Designs: The *maximum allowable linear operation range* of input can be investigated considering the structure shown in Fig. 13, where M_L represents a current-controlled current-source.

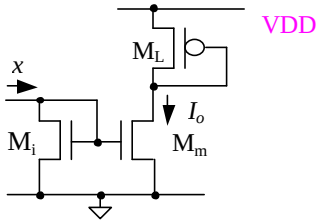


Fig.13: A generic structure of a full-current mode design topology

To realize a *linear operation* between I_o and x, M_i and M_m has to operate in saturation, i.e. $V_{ds,m} \geq V_{gs,i} - VTO_m$

It can be shown that

$$I_o = (b_m / b_i)x \quad iff \quad x \leq \left(\frac{b_i}{2}\right)\left(\frac{VDD - VTO_L}{1+\sqrt{b_m / b_L}}\right)^2 \qquad (16)$$

The maximum range can be determined by setting $b_L \to \infty$

Table 3- Static and dynamic simulation results of gates

Gate	Av. Delay (ns)		Av. Pow. Dis. (mW)	
	Ref.[5]	New gate	Ref.[5]	New gate
Min	2.5	1.8	0.27	0.32
Tsum/Max	7.3	1.5	0.38	0.24
Literal (3 1x1)	8.8	3.8	0.16	0.27
(2 2x3)	9.6	4.1	0.18	0.33

It can be seen no body-bias effect is involved, hence yielding a more technology independent operation. Another advantage is that *linear operation range with minimum-size* NMOS transistors, 120µA for the technology used, is even larger than the *maximum operation output current* of any voltage-mode involved MVL structure, allowing higher radix. A detailed DC related issues can be found in [8].

A comparison with regard to investigated gates is introduced in Table 3,

VII. CONCLUSION

In this study, CMOS current-mode realization of a complete set of MVL operators including *max* gate, as a novelty, is introduced. A novel current-mode threshold circuit is designed and used for realizing *literal* circuits. The DC and transient analysis have been investigated. The study reveals the fact that conventional voltage switched current-mode design methods require exponentially increasing area as the radix increases, and leads higher level of parasitics and oscillatory behavior due to feedthrough. The circuits in this study eliminate these problems and operate faster. Another advantage is the fact that no radix constraint is imposed. Circuits are obtained by using very simple algebraic manipulations. The main drawbacks of the new circuits are larger power consumption and the sensitivity to transistor mismatchings.

VIII. ACKNOWLEDGEMENT

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IX. REFERENCES

[1] D. A. Freitas and K. W. Current, "A CMOS Current comparator circuit", Electron. Lett., vol. 19, no. 17, pp. 695-696, Aug. 1983.

[2] M. Davio and J. P. Deschamps, " Synthesis of discrete functions using I^2L technology", IEEE Trans. Comput., vol. C-30, pp. 653-661, Sept. 1981.

[3] T. T. Dao, E. J. McCluskey, "Multivalued Integrated Injection Logic", IEEE Trans. Comput., vol. C-26, no. 12, Dec. 1977.

[4] H. G. Kerkhoff, M. L. Tervoert, " Multiple-Valued Logic Charge-Coupled Devices", IEEE Trans. Comp., vol. C-30, no. 9, pp. 644-652, Sept. 1981.

[5] A. K. Jain, R.J. Bolton and M. H. Abd-El Barr,"CMOS Multiple-Valued Logic Design, -Part I and II", IEEE Trans. Circuits and Systems, vol. 40, no. 8, pp. 503-532, Aug. 1993.

[6] K. W. Current, "Current-Mode CMOS Multiple Valued Logic Circuits", IEEE J. Solid-State Circuits, vol. 29, no. 2, pp. 95-107, Feb. 1994.

[7] C. M. Allen, D. D. Givone, "A minimization technique for multiple-valued logic systems", IEEE Trans. Comput., vol. C-17, pp. 182-184, Feb. 1968

[8] I. E. Ungan and M. Askar, "A Wired-AND Current-Mode Logic Circuit Technique in CMOS for Low-Voltage High-Speed and Mixed-Signal VLSIC", Analog Integrated Circuits and Signal Processing, vol. 14, pp. 59-70, 1997.