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Research Article

Implementation of Power Efficient Flash Analogue-to-Digital Converter

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An efficient low power high speed 5-bit 5-GS/s flash analogue-to-digital converter (ADC) is proposed in this paper. The designing of a thermometer code to binary code is one of the exacting issues of low power flash ADC. The embodiment consists of two main blocks, a comparator and a digital encoder. To reduce the metastability and the effect of bubble errors, the thermometer code is converted into the gray code and there after translated to binary code through encoder. The proposed encoder is thus implemented by using differential cascade voltage switch logic (DCVSL) to maintain high speed and low power dissipation. The proposed 5-bit flash ADC is designed using Cadence 180 nm CMOS technology with a supply rail voltage typically ±0.85 V. The simulation results include a total power dissipation of 46.69 mW, integral nonlinearity (INL) value of −0.30 LSB and differential nonlinearity (DNL) value of −0.24 LSB, of the flash ADC.

1. Introduction

Flash ADC has a high data conversion speed, low resolution, and large chip area along with large power dissipation and is therefore preferred for providing high sampling rates. Other architectures like successive approximation register, sigma delta, and dual slope offer less data rate and high resolution compared to flash converter [1–4].

The sparkle or bubble error is caused due to the imperfect input settling time or mismatching time of inputs of comparator. If the output of comparator is either a logic "1" or logic "0," then this condition is known as metastability condition that can be reduced by using Gray code encoder because Gray code encoding allows only 1-bit change in the output at a time which may improve metastability.

The typical block diagram of flash ADC is as shown in Figure 1. The blocks of flash ADCs are resistor string, comparator's block, and thermometer to gray and gray to binary encoder. It plays an important role especially in optical data recording, magnetic read channel applications, digital communication systems, and so forth that require a high data processing rate and optical communication systems [5–10]. Generally, multi-GS/s ADCs which have low resolution are used in high speed measurement systems [11]. The flash ADC contains bunch of 2^n resistors and $2^n - 1$ comparators for n bit ADC. The resistor string provides reference voltage (V_r) to comparators. These reference voltages and input signal voltages (V_i) are simultaneously activated by the comparators containing $2^n - 1$ comparators [2]. If $V_i > V_r$, then the output of comparator goes high and when $V_i < V_r$, the output of comparator records low. Hence, the output of comparator is known as thermometer code. Flash ADC is designed for 5 bits ($n = 5$) and the number of resistors required is $2^n = 2^5 = 32$, whereas the number of comparators required is $2^n - 1 = 2^5 - 1 = 31$. The important role for ADC is performed by analogue blocks. The design constraints of conversion speed are defined especially by the comparators used in the design of flash ADC [8].

ADCs are used in application areas of camera, digital TVs, mobile phones, wireless sensor networks, transmitter and receiver circuits, and the conversion processes of signals for base band applications [12–16].

The thermometer code is a good solution for low resolution and high speed converters; as the error rate increases, the resolution and the speed also increase [15, 16].

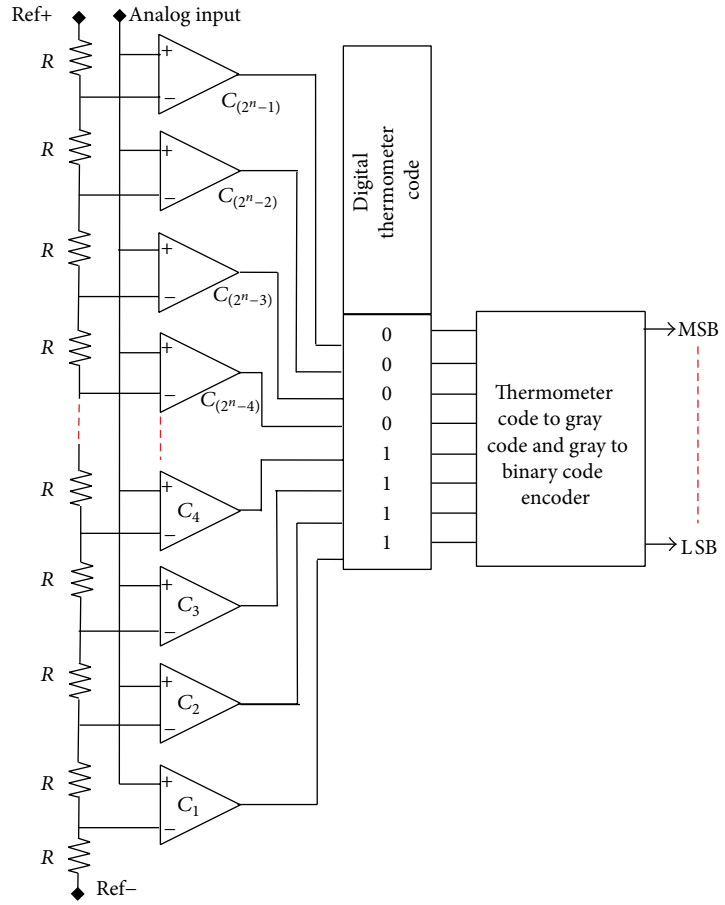


Figure 1: Block diagram of flash analogue-to-digital converter.

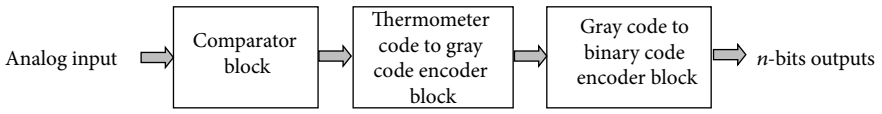


Figure 2: The proposed flash ADC architecture.

The flash ADC requires a more number of comparators to increase resolution. There is an exponential increase in the number of comparators; hence, the circuit requires large chip area, high bandwidth, and more power consumption. Another important area of 5-bit flash ADC is in the application of orthogonal frequency division multiplexing ultrawide band systems [17–21]. There has been much work in implementation of low power and high speed encoders for the design of the flash ADC. The ROM-based encoder is simple and straight forward design, as it is slow and cannot suppress bubble errors. Wallace tree based encoder counts the number of bits "1" in the thermometer code. The disadvantages of this encoder are large delay and power consumption [22–24]. In this approach, the thermometer code to Gray code and Gray to binary code encoders is used, where the gray code encoder is efficient in removing metastability condition and in suppressing the bubble errors. The encoder in this paper has the benefits of high encoding speed and low power consumption, as the DCVSL is used to gain high speed. The proposed flash ADC is designed using encoder as shown in Figure 8.

The rest of the paper is endowed with all design steps and simulation results. The concluding section of the proposed flash ADC performance is compared with the similar designs in the references.

2. Design Steps of 5-Bit Flash ADC

The proposed flash ADC block diagram is as shown in Figure 2. It consists of comparator block, thermometer to Gray code encoder block, and Gray code to binary code encoder block.

2.1. Comparator Structure. The comparator circuit of the designed flash ADC is as shown in Figure 3 and the transistor aspect ratios are given in Table 1. In this schematic, transistors

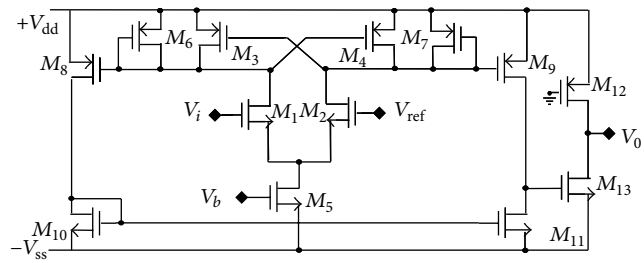


Figure 3: Schematic of comparator.

M_1, M_2 are the NMOS input differential pairs driven by M_5 tail current NMOS transistor. This differential pair is loaded by PMOS cross-coupled transistors ($M_3 - M_4$), which has a positive feedback loop and diode-connected PMOS transistors ($M_6 - M_7$). The purpose of cross-coupled feedback loop is to increase the voltage gain of differential pair ($M_1 - M_2$) and to load the output resistance. M_{10} and M_{11} form a current mirror and its reference current is provided by the transistors (M_6, M_8) together [9].

The common source PMOS amplifier (M_9) amplifies the first-stage output of the comparator [21]. The last stage of the comparator is current source inverter circuit ($M_{12} - M_{13}$). This inverter achieves higher voltage gain than CMOS inverter [22]. The results of the complete comparator are shown in Figures 4(a), 4(b), and 4(c). The offset voltage and gain band width product of comparator are 17.2 mV and 6.77 GHz.

2.2. Design of the Proposed Encoder. The conversion of the thermometer code output of the comparator to binary code is one of the bottlenecks in the high speed flash ADC design [1]. Programmable logic array-read-only memory, exclusive OR encoder, or Wallace tree encoder structures are generally used for conversion [23, 24]. The Wallace tree adder technique is effective in removing the bubble errors but it is at the cost of speed reduction and increased power dissipation [25]. The metastability condition occurs due to the time variation between the comparators input and the effect of bubble errors can be reduced by converting the thermometer code to Gray code. The truth table corresponding to 5-bit binary to gray code is presented in Table 2. The relationship between thermometer code, Gray code, and binary code is given below [3]:

$$G_0 = T_1\overline{T_3} + T_5\overline{T_7} + T_9\overline{T_{11}} + T_{13}\overline{T_{15}} + T_{17}\overline{T_{19}} + T_{21}\overline{T_{23}} + T_{25}\overline{T_{27}} + T_{29}\overline{T_{31}},$$

$$G_1 = T_2\overline{T_6} + T_{10}\overline{T_{14}} + T_{18}\overline{T_{22}} + T_{26}\overline{T_{30}},$$

$$G_2 = T_4\overline{T_{12}} + T_{20}\overline{T_{28}},$$

Table 1: Comparator schematic transistor aspect ratios.

Transistor	W (μm)	L (μm)
M_1, M_2	3.0	0.2
M_3, M_4, M_7, M_9	6.0	0.2
M_5	2.0	0.18
M_6, M_8	6.0	0.18
M_{10}, M_{11}, M_{13}	2.0	0.2
M_{12}	0.4	0.2

$$G_3 = T_8\overline{T_{24}},$$

$$G_4 = T_{16},$$

$$B_0 = G_0 \oplus B_1,$$

$$B_1 = G_1 \oplus B_2,$$

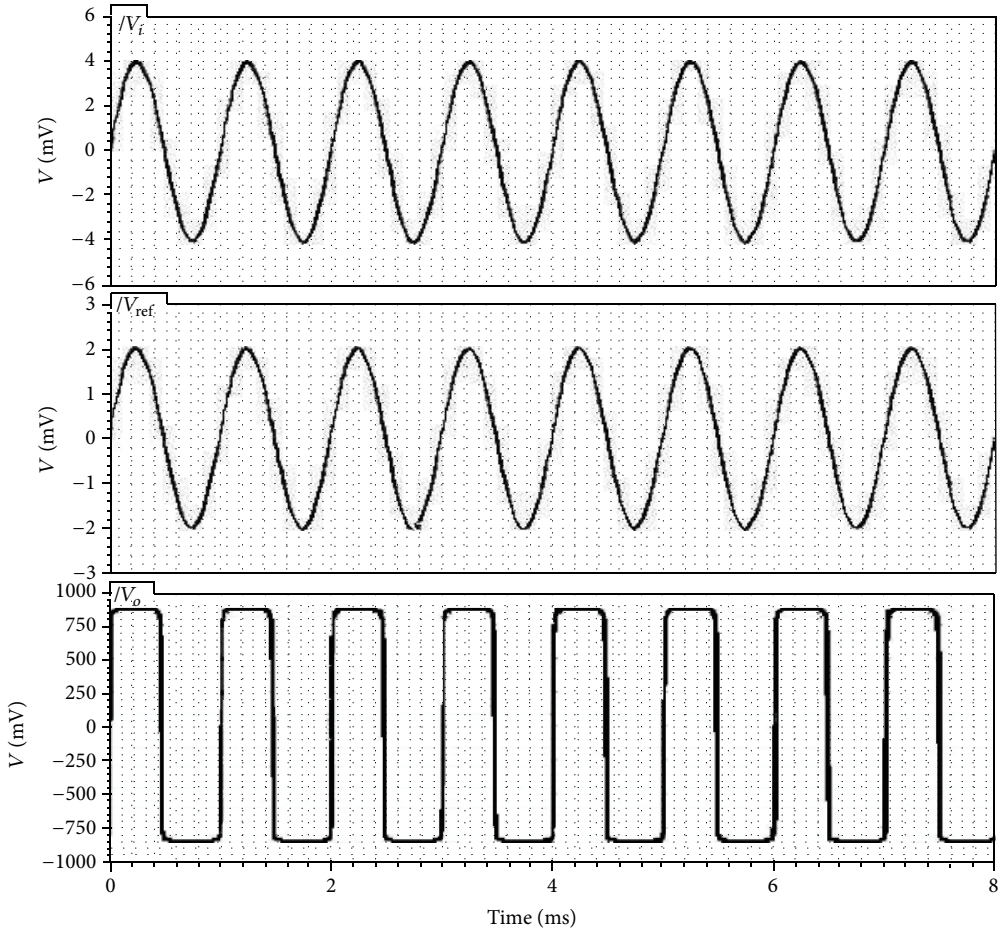
$$B_2 = G_2 \oplus B_3,$$

$$B_3 = G_3 \oplus B_4,$$

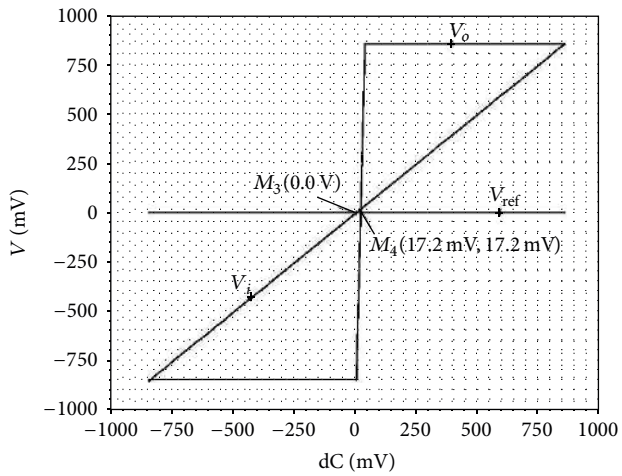
$$B_4 = G_4. \quad (1)$$

The equations are derived from the following truth Table 2 for this encoder.

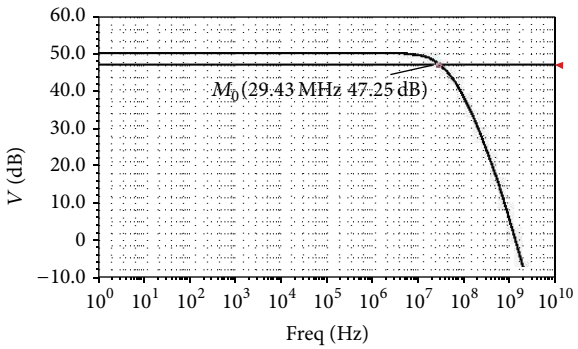
2.3. Implementation of the Proposed Encoder. There are different logic styles to implement the design of the thermometer code to Gray and Gray to binary code encoders. To avoid the static power dissipation and to achieve high speed, the implementation of encoder is validated using DCVSL [26]. DCVSL gate has speed advantage over pseudo-NMOS logic, there by the parasitic capacitance of the output node of DCVSL logic gets reduced and faster response is achieved. The static power consumption present in static CMOS logic is eliminated in DCVSL [9]. DCVSL is a CMOS circuit technique that has potential advantages over conventional NOR/NAND logic in terms of circuit delay, layout density, logic flexibility, and power dissipation [10].



(a) Transient analysis of comparator



(b) The DC analysis results of the comparator



(c) Gain plot of the comparator

Figure 4

Table 2: Binary to gray code encoder truth table.

B_4	B_3	B_2	B_1	B_0	G_4	G_3	G_2	G_1	G_0	Thermometer code ($T_{31}, T_{30}, \ldots, T_1$)
0	0	0	0	0	0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	0	0	0	1	1	00000000000000000000000000000011
0	0	0	1	1	0	0	0	1	0	00000000000000000000000000000111
0	0	1	0	0	0	0	1	1	0	00000000000000000000000000001111
0	0	1	0	1	0	0	1	1	1	00000000000000000000000000011111
0	0	1	1	0	0	0	1	0	1	00000000000000000000000000111111
0	0	1	1	1	0	0	1	0	0	00000000000000000000000001111111
0	1	0	0	0	0	1	1	0	0	00000000000000000000000011111111
0	1	0	0	1	0	1	1	0	1	00000000000000000000000111111111
0	1	0	1	0	0	1	1	1	1	00000000000000000000001111111111
0	1	0	1	1	0	1	1	1	0	00000000000000000000011111111111
0	1	1	0	0	0	1	0	1	0	00000000000000000000111111111111
0	1	1	0	1	0	1	0	1	1	00000000000000000001111111111111
0	1	1	1	0	0	1	0	0	1	00000000000000000011111111111111
0	1	1	1	1	0	1	0	0	0	00000000000000000111111111111111
1	0	0	0	0	1	1	0	0	0	00000000000000001111111111111111
1	0	0	0	1	1	1	0	0	1	00000000000000011111111111111111
1	0	0	1	0	1	1	0	1	1	00000000000000111111111111111111
1	0	0	1	1	1	1	0	1	0	00000000000001111111111111111111
1	0	1	0	0	1	1	1	1	0	00000000000011111111111111111111
1	0	1	0	1	1	1	1	1	1	00000000001111111111111111111111
1	0	1	1	0	1	1	1	0	1	00000000011111111111111111111111
1	0	1	1	1	1	1	1	0	0	00000001111111111111111111111111
1	1	0	0	0	1	0	1	0	0	00000011111111111111111111111111
1	1	0	0	1	1	0	1	0	1	00000111111111111111111111111111
1	1	0	1	0	1	0	1	1	1	00001111111111111111111111111111
1	1	0	1	1	1	0	1	1	0	00011111111111111111111111111111
1	1	1	0	0	1	0	0	1	0	00111111111111111111111111111111
1	1	1	0	1	1	0	0	1	1	01111111111111111111111111111111
1	1	1	1	0	1	0	0	0	1	11111111111111111111111111111111
1	1	1	1	1	1	0	0	0	0	11111111111111111111111111111111

The design of CMOS logic with DCVSL has many advantages over static CMOS logic approach, and DCVSL has speed advantage over domino logic circuit. This logic style has both noninverting and inverting logic implementation, where domino logic cannot implement inverting logic operational gates. However, these advantages are achieved at the expense of the large area and the complexity associated with dual logic networks including complementary signals [27].

In this paper DCVSL circuit is proposed, which does not require complementary inputs. The proposed DCVSL simplifies the logic tree complexity, reduces dynamic power, and improves the performance of the circuits. The proposed DCVSL is as shown in Figure 5.

To reduce the power consumption and to increase the performance, many clocked versions of DCVSL gates have been introduced. The reduction of parasitic capacitances at the output node provides a faster response and the static power consumption is eliminated [28, 29]. The operation of DCVSL is as follows. During precharge (clk = 0) phase, transistors Q_4, Q_5 are turned ON; the output node is charged to V_{DD}. The input is given to the NMOS logic tree and the logic of operation is implemented using n-channel MOSFET. A diode Q_3 works as a dynamic current source to limit the amount of charge transferred from one output node. For the implementation of fast error-correction logic in memories, this DCVSL logic can be used [10]. The schematic of the Gray code encoder for each bit is designed using proposed circuits shown in Figure 6.

The circuits of Gray code bit-0, 1, 2, 3, 4 are shown in Figures 6(a), 6(b), 6(c), 6(d), and 6(e). The logic of these circuits is designed from (1) using the DCVS logic, and a CMOS inverter is used at the output stage of the circuit.

By using the XOR gate, the Gray code will be converted into binary code. The schematic of 2-input XOR gate is as shown in Figure 7. The design of complete encoder is as

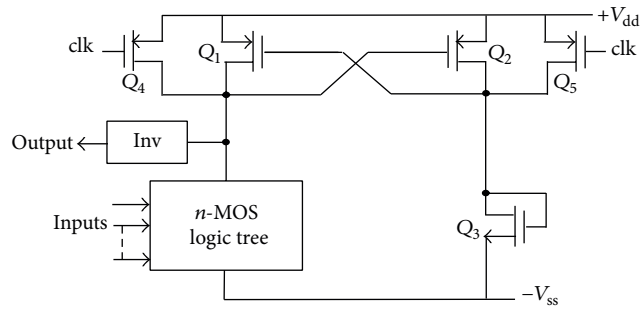
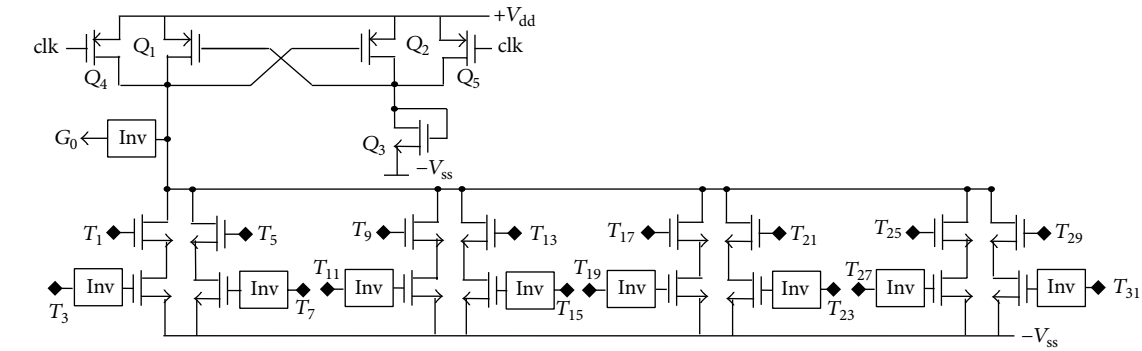
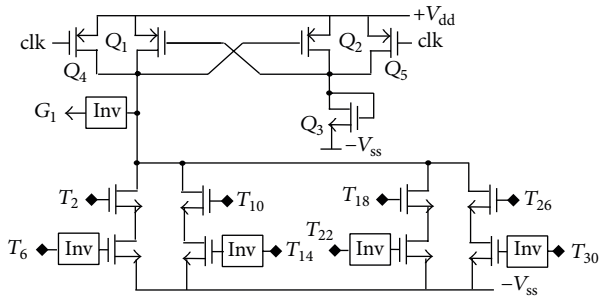


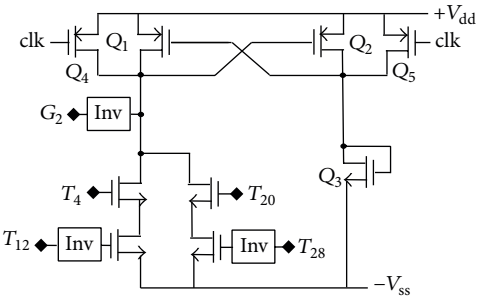
Figure 5: Schematic of proposed circuit using DCVS logic.



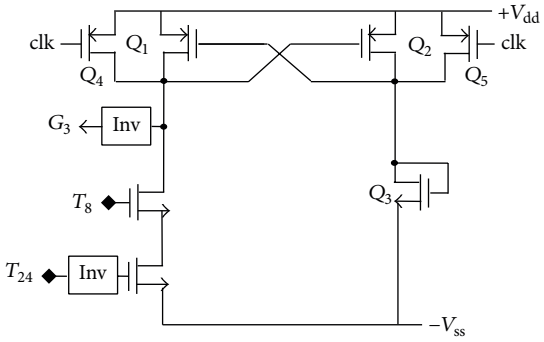
(a) Gray code BIT-0 generation circuit



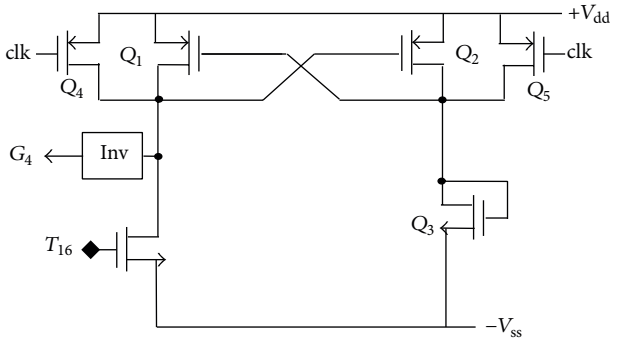
(b) Gray code BIT-1 generation circuit



(c) Gray code BIT-2 generation circuit



(d) Gray code BIT-3 generation circuit



(e) Gray code BIT-4 generation circuit

Figure 6: Schematic of Gray Code encoder using DCVS logic.

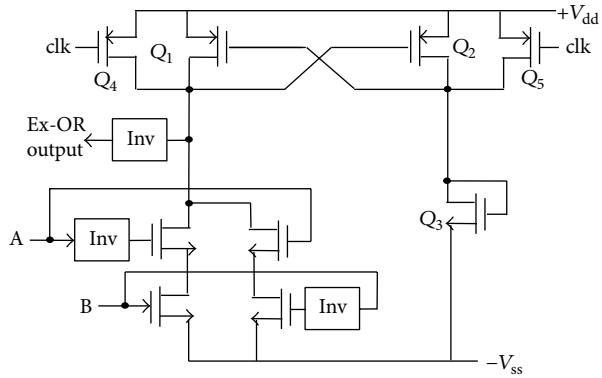


Figure 7: Schematic of two-input Ex-OR gate.

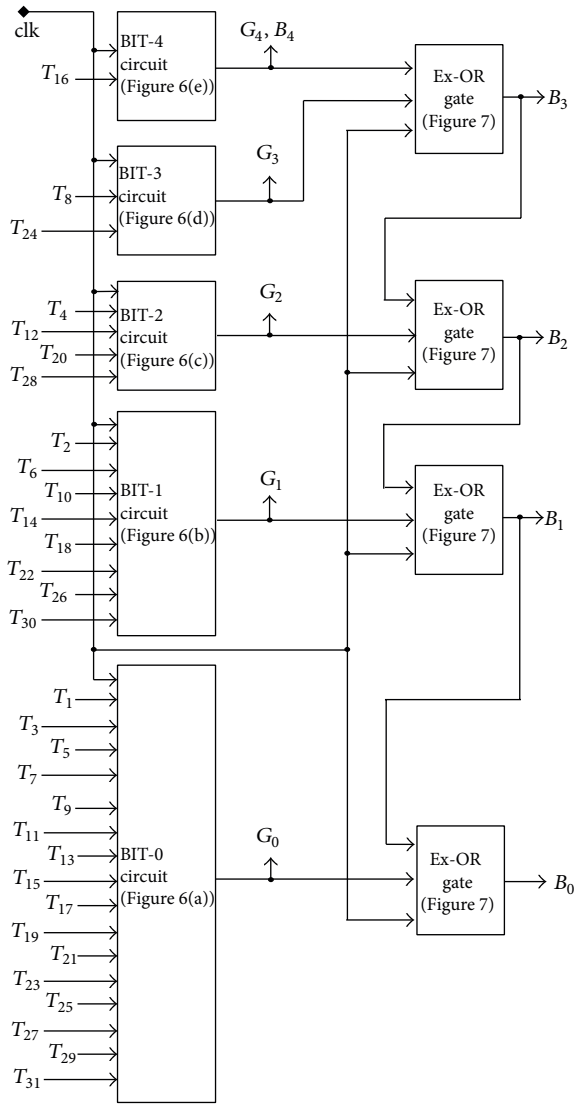


Figure 8: Complete schematic diagram of encoder.

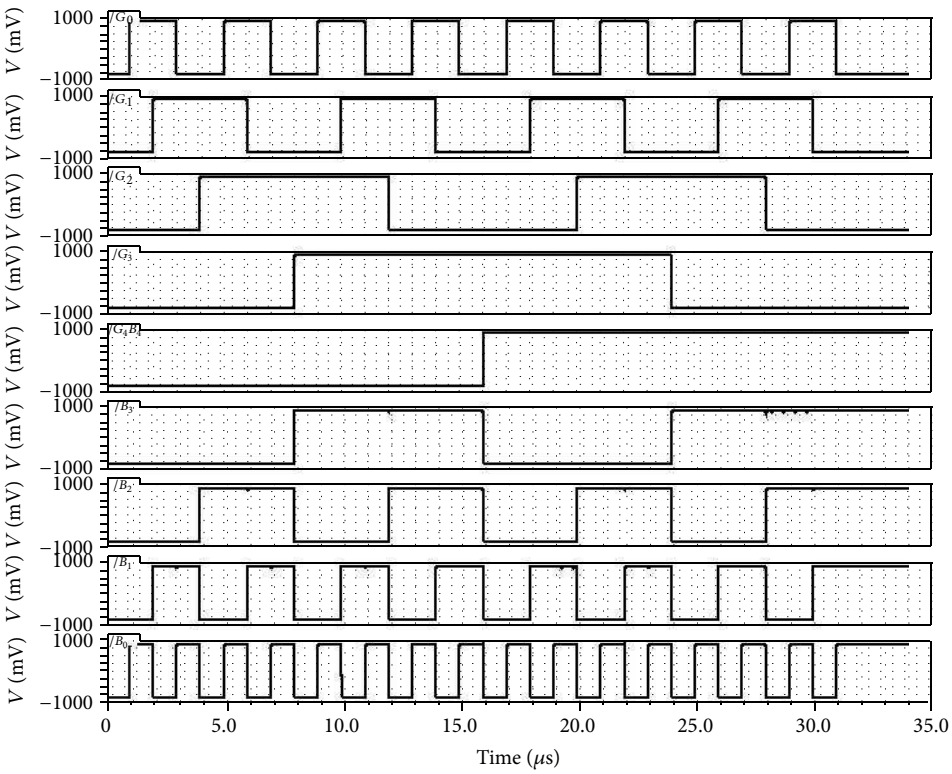


Figure 9: Simulation results of encoder.

Table 3: Summary of proposed encoder.

Results	Proposed Encoder
Resolution	5-bit
Worst case delay	30 μs
Technology	180 nm
No. of Transistors	156
Supply Voltage	±0.85 V
Current	3.56 mA
Power Dissipation	6.06 mW

Table 4: Transistor count of the designed system blocks.

Name of the block	Transistors count
Comparator block	403
Gray code encoder block	96
Binary encoder block	60
Total flash ADC blocks	559

shown in Figure 8. The results of the proposed encoder are presented in Table 3.

3. Simulation Results

The complete design of 5-bit 5-GS/s flash ADC circuit as shown in Figure 1 is simulated using Cadence and the model parameters of a gpdk 180 nm CMOS process. As resolution increases, the maximum frequency of operation will get decreased. The encoder in Figure 8 is simulated by providing thermometer code as input which is presented in Table 2 and the results of encoder are as shown in Figure 9 and it is verified using truth Table 2.

A ramp-shaped analogue input signal between −0.45 and 0.75 V, at 1 MHz, is applied to the ADC input for transient analysis and the simulation results of 5-bit flash ADC obtained are as shown in Figure 10. Figure 11 shows the following linearity plots of differential nonlinearity (DNL) and integral nonlinearity (INL). Transistor count of the designed system blocks is shown in Table 4. The RC extracted layout of the complete converter is shown in Figure 12. The advantages of this flash ADC are as follows: power consumption is at minimum, errors in the design are minimized, and the proposed configuration is designed at the high sampling rate 5-GS/s. The performance summary and its comparison with similar works in the literature are listed in Table 5 given below.

4. Conclusion

A 5-GS/s 5-bit flash ADC is designed in 180 nm CMOS technology using Cadence tools. In this flash ADC, the proposed encoder uses a logic style called DCVSL structure that improves the performance in terms of power consumption and speed. The proposed flash ADC is highly linear with worst-case DNL of −0.24 LSB and INL of −0.30 LSB and also has a low power consumption of 46.69 mW. This

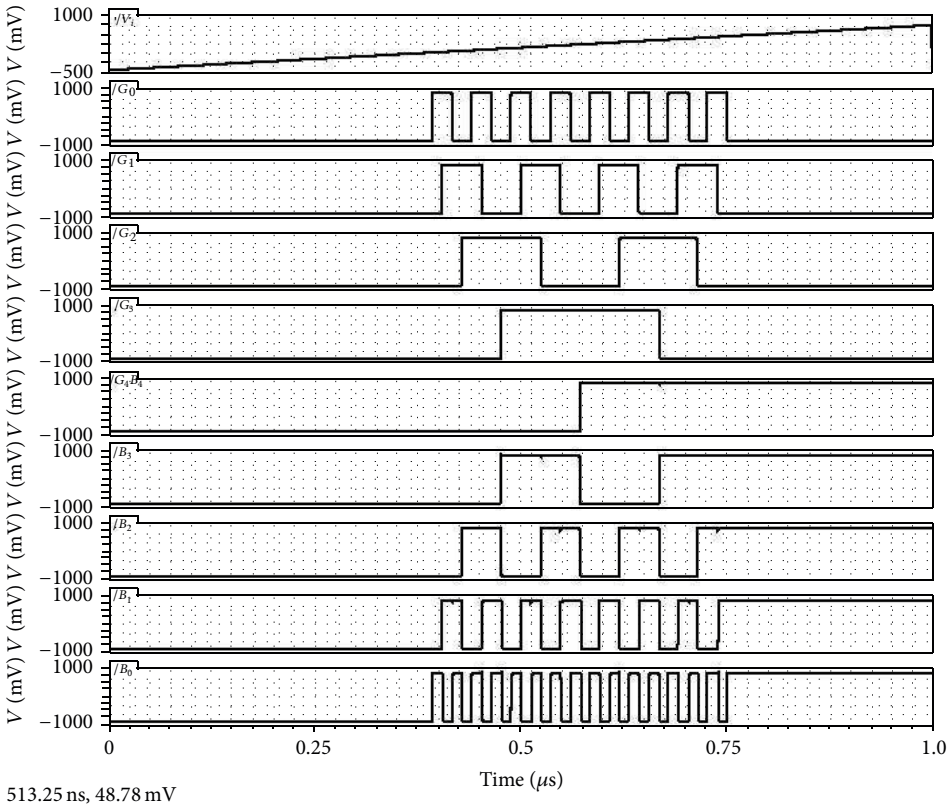


Figure 10: The 5-bit simulation results of flash ADC.

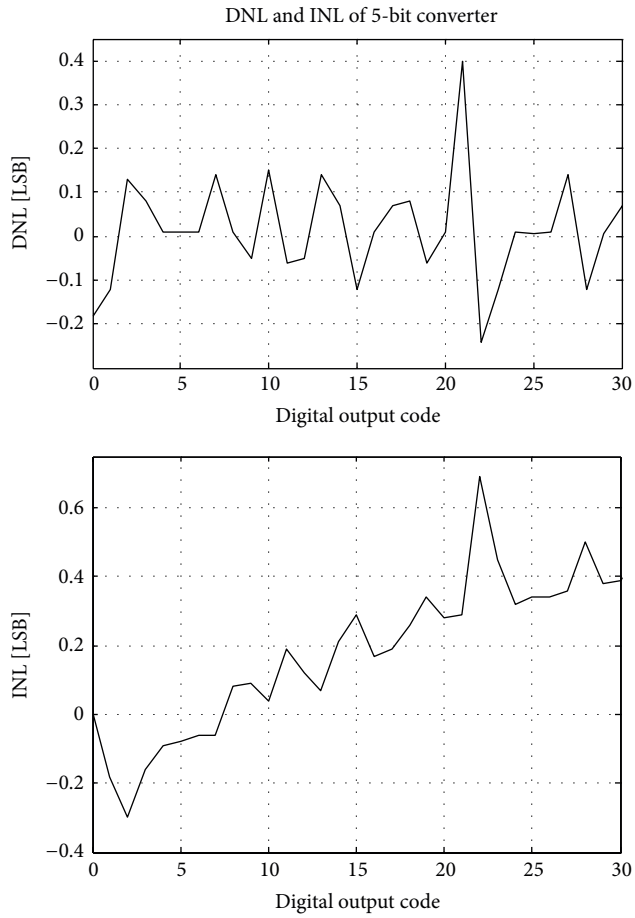


Figure 11: DNL and INL of flash ADC.

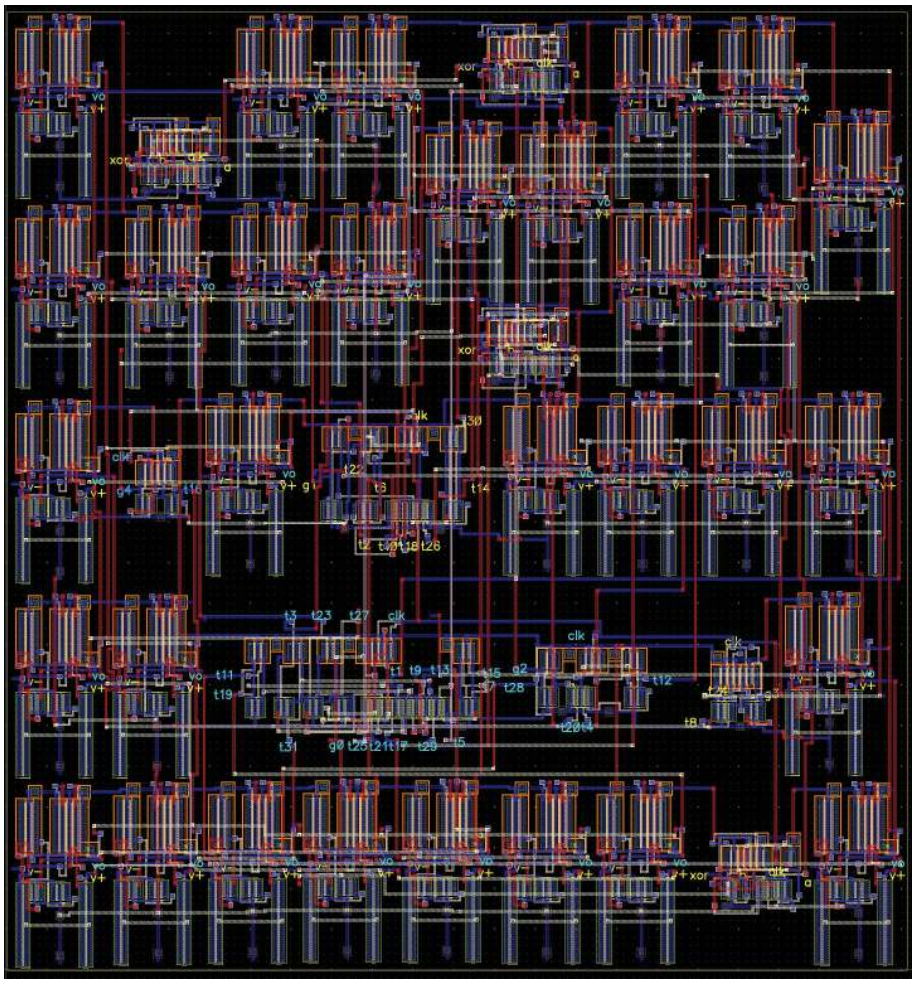


Figure 12: RC extracted layout of flash ADC.

Table 5: Comparative performance analysis of candidate design.

		References			
	Proposed ADC simulated results	Simulated results [8]	Simulated results [11]	Simulated results [18]	Simulated results [19]
Technology	180 nm	180 nm	500 nm	180 nm	180 nm
Resolution	5-bit	5-bit	5-bit	5-bit	4-bit
Supply voltage	±0.85 V	1.8 V	2.5 V	1.5 V	1.8 V
Analogue input voltage range	−0.45 V to 0.75 V	differential input range ± 0.4 V	—	—	1 Vpp
Power (mW)	46.69	63	83	68.63	70
Sampling rate GS/s	5	1	1.5	—	5.0
Maximum DNL (LSB)	−0.24	0.175	0.43	0.0012	0.34
Maximum INL (LSB)	−0.30	0.261	0.32	0.0015	0.24

circuit can be expected to find wider applications in many applied electronics, communications, instrumentation, and signal processing applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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