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Implementation of silicon-on-glass MEMS devices with embedded through-wafer silicon vias using the glass reflow process for wafer-level packaging and 3D chip integration

Chiung-Wen Lin[1], Chia-Pao Hsu[2], Hsueh-An Yang[3], Wei Chung Wang[1,3] and Weileun Fang[1,2]

[1] Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu, Taiwan
[2] Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan
[3] Advanced Semiconductor Engineering Inc., Kaohsiung, Taiwan

E-mail: fang@pme.nthu.edu.tw

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Abstract
This study presents a novel system architecture to implement silicon-on-glass (SOG) MEMS devices on Si–glass compound substrate with embedded silicon vias. Thus, the 3D integration of MEMS devices can be accomplished by means of through-wafer silicon vias. The silicon vias connecting to the pads of devices are embedded inside the Pyrex glass. Parasitic capacitance for both vias and microstructures is decreased and mismatch of coefficient of thermal expansion (CTE) is reduced. In applications, the glass reflow process together with the SOG micromachining processes were employed to implement the presented concept. Successful driving of the resonator through the silicon vias is demonstrated. The wafer-level hermetic packaging can be further achieved by anodic bonding of a Pyrex7740 wafer. Hermeticity of the packaged device performed by helium leak test satisfied MIL-STD-883E. The packaged SOG device is SMT (surface mount technology) compatible and ready for 3D microsystem integration.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The 3D integration of chip sets is regarded as a promising device architecture for next generation microsystems. The chip size of integrated circuits (IC) can be significantly reduced after replacing planar 2D interconnects with vertical 3D interconnects. Presently, various research on 3D heterogeneous integration of IC has been reported, for instance the vertical stacking of chips with [1–3] or without interposer [4, 5]. Similarly, the 3D MEMS packaging also provides many advantages such as smaller footprint and SMT compatibility. Thus the techniques to realize 3D integration of MEMS devices attract considerable attention. In general, the 3D integration of MEMS devices can be accomplished by means of through-wafer interconnections. For instance, approaches to fabricate through-wafer vias in a capping wafer have been reported [6, 7]. Through-wafer vias embedded inside the substrate of MEMS devices are employed in [8–11].

Metal deposition and electroplating are the most popular approaches to prepare the interconnections inside through-wafer vias [6–8]. However, the aspect ratio of the metal-via is limited to the deposition process. For instance, voids may occur in high aspect ratio metal electroplating, and the conformal coating of high aspect ratio vias is a challenge for physical vapor deposition of metal. Moreover, failure may arise from the large coefficient of thermal expansion (CTE)

mismatch between the metal and silicon. On the other hand, for non-RF MEMS applications [9–11], single crystal silicon (SCS) is also employed to act as the through-wafer vias. These SCS vias are directly patterned on the low-resistivity silicon substrate by BOSCH DRIE (deep reactive ion etching) technology. Hence, high-aspect-ratio vias and small via pitch can be achieved. The electrical insulation of these SCS vias is easily provided by air [9] and dielectric materials [10, 11] during the fabrication processes. The glass flow process (GFP) technology has been exploited in [12] to mold the glass using the silicon substrate. The GFP technology is further employed to massively fill the dielectric material into a silicon substrate with SCS vias [13]; thus, a glass capping with SCS vias is achieved.

According to the simple fabrication process, the applications of silicon-on-glass (SOG) wafers for MEMS devices are gradually increased. The SOG wafer is prepared after the bonding of single crystal silicon with Pyrex 7740 glass (chemical composition: SiO_2 80.6%, Na_2O 4.0%, B_2O_3 13.0%, Al_2O_3 2.3% and miscellaneous traces 0.1% [14]). The typical SOG MEMS processes involve the patterning of silicon device layer using BOSCH DRIE, and the following microstructure releasing process using HF glass etching. Since the SOG wafer employs the dielectric glass as the handling substrate, the parasitic capacitance noise can be significantly reduced. This characteristic is especially attractive for capacitance-type MEMS sensors [15–17]. This study presents a glass reflow process to implement SOG MEMS devices on Si–glass compound substrate with embedded silicon vias, as shown in figure 1(*a*). The silicon vias are patterned by photolithography and DRIE, and then hermetically sealed by Pyrex7740 after the glass reflow process. Meanwhile, the single crystal silicon (SCS) on Si–glass compound substrate is exploited to fabricate MEMS devices. This SOG device with embedded silicon vias is ready for 3D integration with IC, as shown in figure 1(*b*). The merits of this device architecture and process flow are: (1) parasitic capacitance for both vias and microstructures is decreased; (2) mismatch of coefficient of thermal expansion (CTE) is reduced; (3) ease of wafer-level 3D integration of MEMS devices; (4) ready for wafer-level hermetic packaging by anodic bonding and (5) compatible with surface mount technology (SMT).

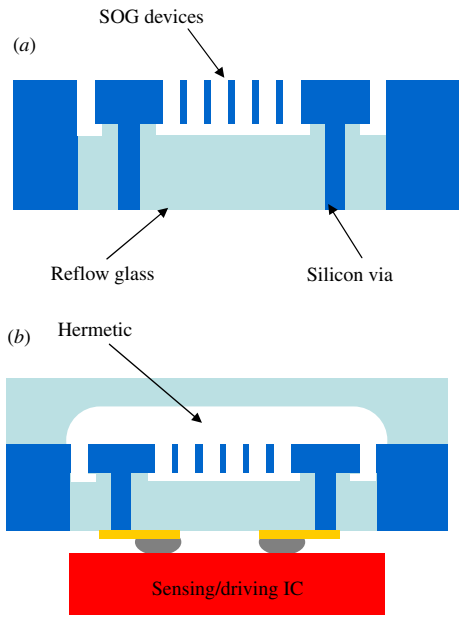

Figure 1. The concept of the present system architecture, (*a*) the SOG devices with embedded through-wafer silicon via and (*b*) the packaging and 3D integration of the present SOG device.

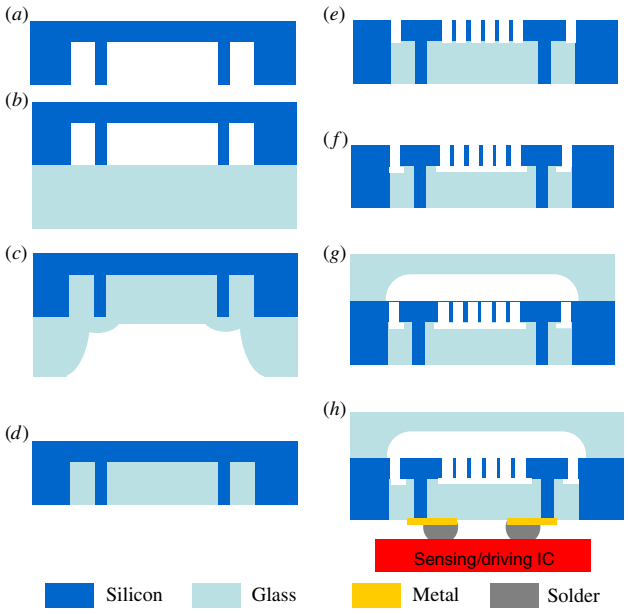

Figure 2. Process flow for SOG devices with embedded through-wafer SCS vias.

2. Concept and process steps

The fabrication process illustrated in figure 2 has been established to implement the present architecture in figure 1(*a*). As shown in figure 2(*a*), the photolithography and the BOSCH DRIE were performed on the backside of double-side polished silicon wafer to fabricate the cavities and silicon vias. The planar dimensions of via and the pitch between vias were defined by photolithography. The length of via and the thickness of SOG device were determined by DRIE. As shown in figure 2(*b*), anodic bonding of Pyrex7740 glass wafer and silicon wafer was performed using a commercial bonder in vacuum chamber, with voltage of 1000 V and temperature of 400 °C. In general, the ambient pressure in the vacuum chamber was 5 mTorr during bonding, and the pressure inside the cavity sealed by silicon and glass was much smaller than 1 atm after bonding. As illustrated in figure 2(*c*), the bonded Si–glass wafer was then placed into a 750 °C furnace for 6 h to perform the glass reflow process. Under the assistance of pressure load, the spaces surrounding silicon vias were filled with glass. As shown in figure 2(*d*), the lapping process was used to planarize the surface of reflow glass. Moreover, this process was also employed to expose one end of the silicon vias for electrical interconnection. Thus, Si–glass

compound substrate with embedded through wafer silicon vias was achieved. As shown in figure 2(*e*), the SCS on Si–glass compound substrate was patterned by photolithography and DRIE to define the microstructures. The compound substrate was then immersed into HF solution to isotropically etch the glass. The backside of the compound substrate was protected using a chuck with O-ring sealing during the HF etching. The microstructures were fully released after glass etching, so as to form the suspended SOG devices with embedded silicon vias, as shown in figure 2(*f*). The wafer-level packaging of MEMS devices can be further accomplished after capping with Pyrex7740 glass wafer. Thus, as illustrated in figure 2(*g*), the electrical interconnect was easily achieved using the silicon vias. Moreover, an additional patterned metal layer at the backside of the compound substrate was exploited to redistribute the bonding pads. The wafer-level 3D integration of MEMS devices and other chips is also achieved, as shown in figure 2(*h*).

3. Experiment and results

To demonstrate the feasibility of the present concept shown in figure 2, various SOG devices with embedded through-wafer silicon vias were fabricated on Si–glass compound substrate. The following wafer-level capping of these SOG devices using Pyrex7740 glass wafer is also implemented. In addition, various tests regarding the performances of silicon vias and SOG devices, and the quality of 3D packaging unit were also investigated.

3.1. Fabrication and integration

After the glass reflow process, the optical image of this Si–glass compound substrate is shown in figure 3(*a*). The glass massively filled into the silicon cavity after the reflow process is clearly observed. As shown in figure 3(*b*), the profile measured using a stylus profilometer indicates the surface topology of Pyrex7740 glass after the reflow process depicted in figure 2(*c*). The maximum depth variation of the glass surface is 453.8 μm which is very close to the via-depth of 450 μm defined by DRIE. It indicates that the reflow glass has properly filled into the cavity surrounding the via. The photo in figure 4(*a*) shows the planarized Si–glass compound substrate with embedded silicon vias after glass lapping (as illustrated in figure 2(*d*)). It is also observed from the zoom-in photo in figure 4(*a*) that one end of the silicon vias is exposed successfully, whereas, the vias remain surrounded by the glass. Moreover, this study further placed the sample into HF solution for 7 min to remove 53 μm thick glass from the backside of the compound substrate, as shown in figure 4(*b*). Thus, part of the SCS via is exposed from the glass, and the rest of this SCS via (approximately 397 μm long) is still embedded inside the glass. As shown in the zoom of the SEM micrograph in figure 4(*b*), the glass is in tight contact along the periphery of SCS via. The SEM micrograph in figure 5 shows a patterned SCS microstructure on Si–glass compound substrate (as the process shown in figure 2(*e*)). The silicon and the glass on this compound substrate are indicated in the photo. In addition,

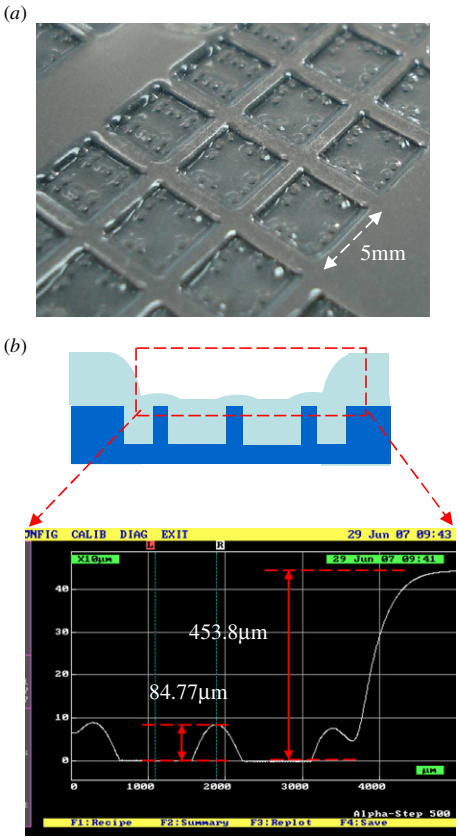

Figure 3. (*a*) The optical micrograph and (*b*) the measured surface profile of substrate right after the glass reflow process shown in figure 2(*c*).

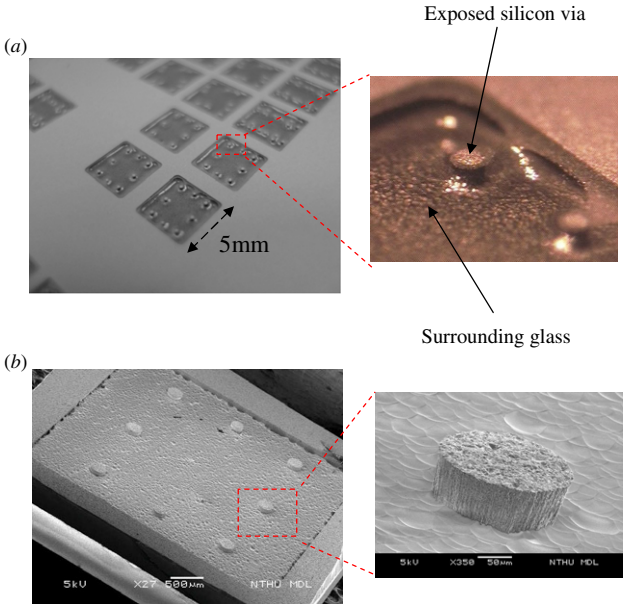

Figure 4. (*a*) The optical micrographs of SCS vias and surrounding Si–glass compound substrate after the lapping process in figure 2(*d*) and (*b*) the SEM micrographs of the SCS via and its surrounding glass after removing 53 μm thick glass by HF.

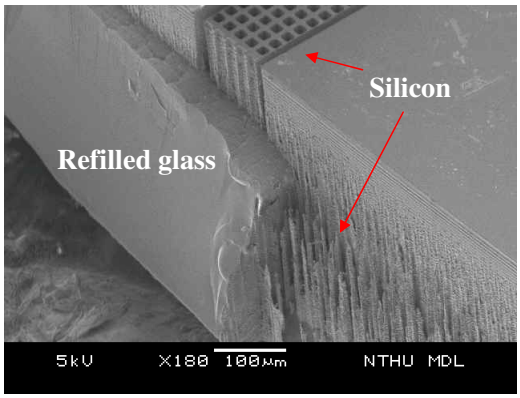

Figure 5. The SEM micrograph of a patterned SCS microstructure on Si–glass compound substrate.

this photo also clearly shows that the cavity underneath the patterned SCS structures is completely filled by the reflow glass.

Figure 6(*a*) shows SEM micrographs of two typical fabricated devices, including a linear accelerometer (left) and a comb-drive resonator (right). The glass underneath the suspended microstructures has been fully removed by isotropic etching indicated in figure 2(*f*), so as to lead to a rough surface. As shown in figure 6(*b*), the broken substrate is further employed to show the silicon via under the bonding pad and the fully suspended SCS structure. The silicon vias are connecting perfectly with the bonding pad. In addition, the silicon vias are anchored to the Si–glass substrate properly by the surrounded glass. The chips in figure 7(*a*) show various packaged

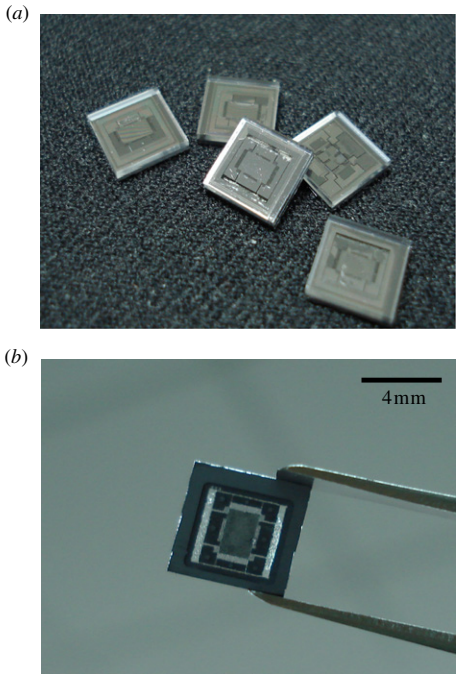

Figure 7. The optical micrographs of (*a*) various packaged SOG devices and (*b*) the transparent region of the packaged device shows the existence of glass on the compound substrate.

SOG MEMS devices on the present Si–glass compound substrate using the wafer-level packaging process indicated in figure 2(*g*). Thus, various typical SOG MEMS devices such as accelerometers and gyroscopes with embedded SCS vias can

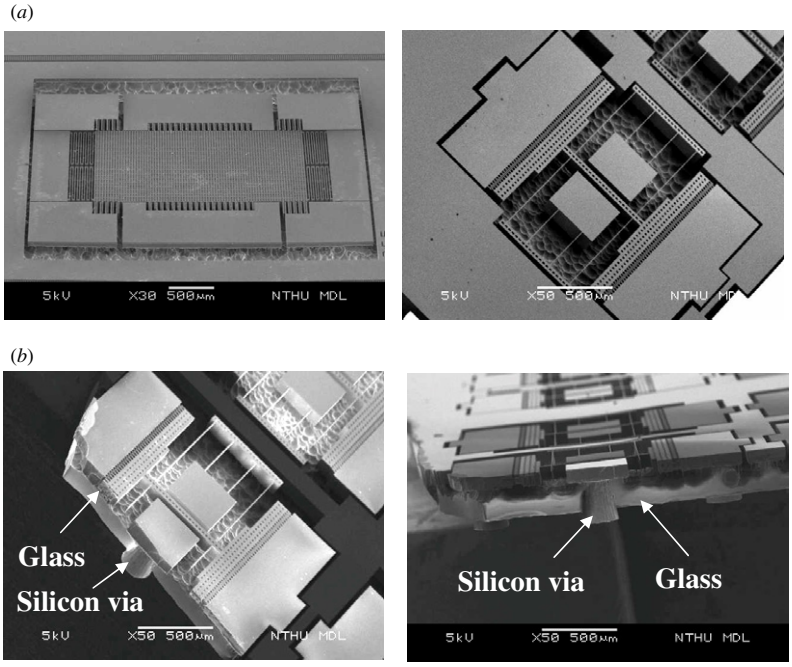

Figure 6. The SEM micrographs of (*a*) two typical fabricated SOG devices after being suspended from the substrate and (*b*) the cross-sectional view of the SOG device which clearly shows the suspended SCS microstructures and SCS vias.

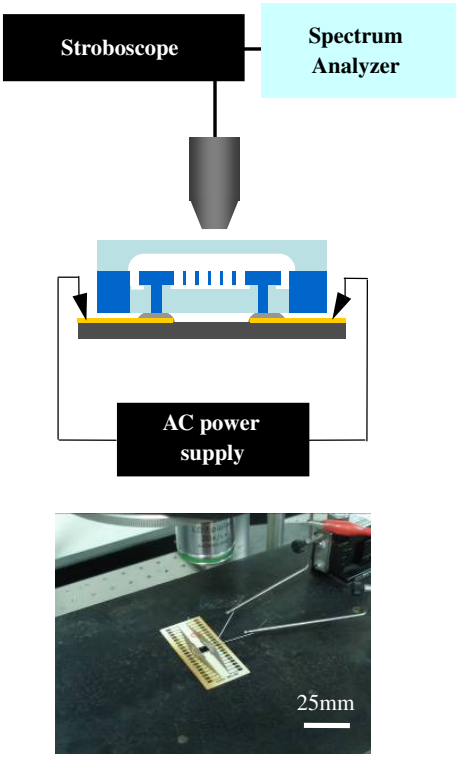

Figure 8. The experimental setup to measure the dynamic response of a SOG resonator.

be packaged using this technique. The transparent regions in figure 7(*b*) show the existing glass on the compound substrate.

3.2. Tests

The test setup in figure 8 was established to measure the dynamic response of the micromachined SOG actuators, so as to further characterize the performance of embedded through-wafer silicon vias. The chip containing the SOG resonator was bonded on a PCB, and the driving signal from an AC power supply was provided to the resonator through the SCS via, as depicted in figure 8. The in-plane dynamic response of the resonator was measured using a commercial stroboscope with a resolution of 0.1 μm. Figure 9 shows the typical dynamic response of the resonator driven at the frequency range of 800–1400 Hz, and the measured resonant frequency is 1.10 kHz with a quality factor of 40.89. As a result, the test demonstrates that the present process successfully fabricates SOG MEMS devices on Si–glass compound substrate. Moreover, the packaged device has been successfully driven through the present SCS vias.

Following the conditions specified in MIL-STD-883E, method 1014.9, the hermeticity of the SOG MEMS device with embedded SCS vias was evaluated by an industrial helium leak test system. As shown in figure 2(*g*), the test sample had an equivalent packaging volume of 0.72 mm^3. The sample was placed into a chamber with high ambient pressure of He gas to force the He into the space sealed by the sample. The bomb pressure was 5 bar for 2 h. The dwell time of this test

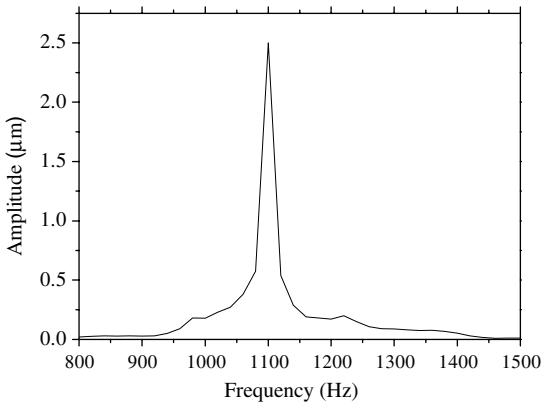

Figure 9. The typical measured frequency response of the SOG resonator.

was less than 5 min. After that, the test sample was placed into a vacuum chamber to measure the leakage of He gas. The measured helium leak rate was 5.0×10^{-8} atm cc s^{-1}. This result indicates that the present SOG MEMS device with embedded SCS vias has satisfied the test standard of MIL-STD-883E, method 1014.9 [18].

4. Conclusions

This research successfully demonstrates a novel device architecture for SOG MEMS components on Si–glass compound substrate with embedded SCS vias. The GFP process was used to prepare the Si–glass compound substrate. The SCS vias monolithically integrated with the pads of MEMS devices are embedded inside the bulk Pyrex glass. Parasitic capacitance for both vias and microstructures is decreased and mismatch of CTE is reduced. In applications, the GFP together with SOG micromachining processes were performed to implement the presented device architecture. Successful driving of a resonator through the vertical silicon vias has been demonstrated. Moreover, wafer-level packaging was also accomplished by capping the present device with Pyrex7740 glass wafer. The measurements showed that the packaged device with embedded silicon vias had a helium leak rate of 5×10^{-8} atm cc s^{-1}, which satisfied the standard of MIL-STD-883E. The leakage can be further reduced by adjusting the glass reflow parameters such as temperature ramping–cooling procedure. This SOG device with embedded through-wafer silicon vias is a promising approach for the heterogeneous integration of driving and sensing circuits by vertical stacking. As a result, the final packaged SOG device is SMT compatible and ready for 3D integration.

The present process has the potential to provide design flexibility and fabrication advantages. For instance, as shown in figures 2(*b*)–(*c*), a thin silicon device layer may experience the risks of deformation or damage during the thinning and bonding processes. In this regard, a thick silicon device layer can be employed in the processes of figures 2(*a*)–(*c*). After that, an additional chemical mechanical polishing (CMP) process can be applied in figure 2(*d*) for the thinning of the silicon device layer. In addition, the pressure inside the cavity

sealed by silicon and glass in figure 2(*b*) can be increased during the bonding process. This will lead to an air gap between the interface of the device silicon layer and the reflow glass in figure 2(*c*). Thus, the higher lateral etching rate at the interface of silicon and glass during DRIE (named the notching effect) [19] can be prevented.

Acknowledgments

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