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Implementation of Soft-Switching Auxiliary Current Control for Faster Load Transient Response

DONGWOOK KIM, JONGUN BAEK, JISU LEE, JOONHO SHIN, AND JONG-WON SHIN, (Member, IEEE)
Department of Energy Systems Engineering, Chung-Ang University, Seoul 06974, South Korea

Corresponding author: Jong-Won Shin (jwshin@cau.ac.kr)

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ABSTRACT A control circuit for the auxiliary buck/boost converter was designed and implemented to improve the load transient response of the buck converter. The circuit shapes the auxiliary inductor current in the critical conduction mode through peak current mode control. The soft-switching operation of the auxiliary switches minimizes the power loss and thus increases the efficiency of the auxiliary converter. Along with the design guidelines and estimated power loss to improve the performance of the proposed control technique, the implementation of the control circuit is explained in detail. Simple analog ICs such as operational amplifiers and comparators, and a couple of logic gates suffices the realization of the proposed control. A prototype buck converter whose input voltage, output voltage, and switching frequency were 15 V, 3.3 V, and 200 kHz, respectively were tested with the implemented control circuit to verify the performance of the proposed control technique.

INDEX TERMS Buck converter, load transient response, capacitor charge balance, critical conduction mode, peak current mode, soft switching.

NOMENCLATURE

A. COMPONENTS, VOLTAGES, AND CURRENTS OF THE CONVERTER SYSTEM

Δi_O	magnitude of the output current variation
Δv_O	deviation of output voltage
C_O	output capacitor of the main buck converter
C_{oss}	equivalent output capacitance of the auxiliary MOSFETs
i_{L1}	main inductor current
i_{L2}	auxiliary inductor current
i_O	load current
L_1	main inductor
L_2	auxiliary inductor
Q_i	i^{th} MOSFET
R_s	resistance for current sensing
v_{dsi}	drain-source voltage of i^{th} MOSFET
v_{gsi}	gate-source voltage of i^{th} MOSFET
V_{in}	input voltage of the converter
v_O	output voltage of the converter
V_O	DC component of the output voltage of the converter

B. PARAMETERS IN TIME-DOMAIN WAVEFORM AND CONTROL CIRCUIT

Δt_d	time delay between the load current transition and the first turn-on of auxiliary MOSFET
A_0	trapezoidal area between i_{L1} and i_O curves during Δt_d in the time domain
A_i	i^{th} area between i_O and $i_{L1}+i_{L2}$ in the time domain
D_0	pulse signal generated by conventional voltage-mode controller to control Q_1 and Q_2
D_1	output signal of SR latch to control Q_3
D_2	output signal of SR latch to control Q_4
k_n	coefficient to determine the magnitude of N_{env} when i_O steps down
k_{n1}	gain of op-amp 3
k_{n2}	gain of op-amp 5

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k_p	coefficient to determine the magnitude of P_{env} when i_O steps up
k_{p1}	gain of op-amp 2
k_{p2}	gain of op-amp 4
N_{env}	envelope that determines the peak values of i_{L2} when i_O steps down
N_{first}	pulse signal to trigger the first turn-on of Q_4 when i_O steps down
N_n	number of switching cycles of the auxiliary MOSFETs when i_O steps down
N_p	number of switching cycles of the auxiliary MOSFETs when i_O steps up
N_{trig}	flag signal for the transient caused when by stepping-down i_O
P_0	pulse signal input to gate driver to drive Q_1 and Q_2
P_1	pulse signal input to gate driver to drive Q_3
P_2	pulse signal input to gate driver to drive Q_4
P_{env}	envelope that determines the peak values of i_{L2} when i_O steps up
P_{first}	pulse signal to trigger the first turn-on of Q_3 when i_O steps up
P_{trig}	flag signal for the transient caused by stepping-up i_O
T_{off}	OFF-time of the auxiliary MOSFET
T_{on}	ON-time of the auxiliary MOSFET
t_{res}	half resonant period between C_{oss} and L_2
T_t	duration of the load transient period
V_{ref}	reference output voltage in the voltage-mode control loop

I. INTRODUCTION

Switch-mode power supplies for microprocessors and digital signal processors are required to tightly regulate the output voltage during the load transient. Beginning with the time-optimal control (TOC) of the buck converter to minimize the output voltage fluctuation without the aid of auxiliary circuit components [1], various control schemes have been reported to improve the load transient response.

Studies [2]–[6] utilize resistive auxiliary circuits for its simple structure and control. The auxiliary switched parallel inductor [2] and the auxiliary switched resistor [3], [4] suppresses the output voltage fluctuation at the cost of reduced efficiency during the load transient. The increased electromagnetic interference (EMI) owing to the high di/dt of the auxiliary switches is another drawback of these techniques. The auxiliary inductor in parallel with the bidirectional switches achieves the capacitor-charge-balance (CCB) to lessen the output voltage deviation during the load transient [5], [6]. However, these control methods require complicated control circuits and impose a heavy computational burden on the digital integrated circuit (IC). Additionally, the freewheeling current through the resistor degrades the efficiency.

Nonresistive auxiliary circuits improve the dynamic response as well [7]–[25]. The average current mode control of a parallel buck converter has been proposed to reduce the settling time of the output voltage [7]. The tapped inductor [8], [9] and the coupled inductor [10], [11] achieves rapid transient response despite their complicated magnetic design. An optimally scaled auxiliary circuit has enhanced the dynamic response by combining the concepts of the TOC and auxiliary buck/boost converter [12]. The flying-capacitor three-level buck converter [13] reduces the voltage stress on the switches and increases the slope of the inductor current during the transient, which reduces the output voltage deviation. Another auxiliary inductor [14], [15] employs the soft-switching by the resonance with extra capacitors. However, the auxiliary switches must operate in different ways as the load current increases or decreases, and this may require a complicated control circuit.

The high-frequency switching controllers of the auxiliary circuit have been described in previous papers [16]–[24]. A buck/boost converter was proposed [16] to achieve a fast response by employing the output impedance correction circuit. This concept was later extended to the multiphase buck converter with the peak current mode (PCM) control [17]–[18]. Works shown in [19]–[21] control the average current of the auxiliary inductor to secure CCB during the load transient. An adaptive slope control discussed in [22]–[24] also maintains the CCB to further improve the load transient response. Similarly, the flyback-transformer-based buck converter [25] enhances the transient recovery by increasing the slope of the inductor current, particularly in the unloading transient. These control techniques require high-speed sensors and high-performance digital ICs, which increases the complexity and cost of the controller.

This paper presents peak-current-controlling the inductor current of the auxiliary buck converter in critical conduction mode (CRM). This control technique has the two representative advantages: the robustness of the output voltage to the step load transients, and the soft turn-on of the auxiliary MOSFETs to attenuate the power loss and switching noise. The proposed technique is suitable to where stringent output regulation is required with frequent load current variation, e.g., point-of-load converter.

The prior arts [19]–[24] are similar to the proposed technique since they also control the inductor current of the auxiliary buck converter. The proposed technique outperforms these approaches by improving the efficiency of the auxiliary converter while maintaining the same dynamic performance.

The original concept of the proposed control has firstly been addressed in [26]. This paper focuses on the analysis and implementation of the control circuitry with comprehensive explanations. A laboratory prototype was built employing analog devices such as operational amplifiers (op-amps), comparators, and logic gates. For simplicity, digital processors or complicated arithmetic ICs were not utilized. The rest of this paper is organized as follows: Section II describes the operation of the auxiliary converter by the proposed control. Section III shows the design and verification by simulation of the control circuit for the optimal dynamic performance.

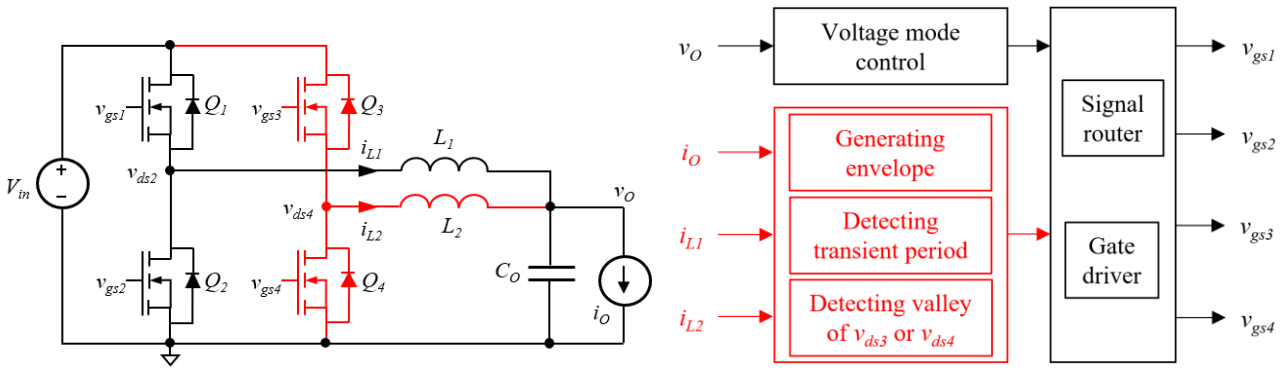

FIGURE 1. (a) Main buck converter (Q_1, Q_2, and L_1) and auxiliary buck/boost converter (Q_3, Q_4, and L_2). Switches Q_3 and Q_4 are operated by the proposed auxiliary current control. (b) Simplified control circuit diagram of the proposed control technique.

The implementation and signal processing of the control circuit is discussed in Section IV. The experimental results and conclusions are in Sections V and VI, respectively.

II. OPERATION PRINCIPLES OF PROPOSED AUXILIARY CURRENT CONTROL TECHNIQUE

Fig. 1(a) presents the main buck converter (Q_1, Q_2, and L_1) and auxiliary buck/boost converter (Q_3, Q_4, and L_2, drawn by red lines) connected in parallel. In the steady-state, Q_1 and Q_2 are operated by the voltage mode controller (VMC) and Q_3 and Q_4 are kept OFF. During the load transient, Q_3 and Q_4 are activated to control i_{L2} and improve the transient response. Switches Q_1 and Q_2 are fully kept ON or OFF during the transient. Fig. 1(b) shows the functional block diagram of the proposed control. The blocks in red, e.g., generating envelope, detecting transient period, and detecting valley of v_{ds3} and v_{ds4}, are the genuine parts to realize the proposed control. These components are explained in detail in Section IV.

The key voltages and currents of the proposed control are shown in Fig. 2. During the transient period caused by stepping-up i_O at t_1–t_5, Q_1 is kept ON and Q_2 is kept OFF as shown in Fig. 2(a). The auxiliary converter works as a PCM-controlled buck converter in CRM. The proposed control shapes i_{L2} into a triangular wave under a positive envelope, P_{env}. The switching period of the auxiliary converter consists of the three following switching states:

- Inductor-charging state such as t_1–t_2: Current i_O is stepped up at t_1; Q_3 is turned ON and i_{L2} increases linearly.
- Inductor-discharging state such as t_2–t_3: When i_{L2} reaches P_{env} at t_2, Q_3 turns OFF and i_{L2} decreases and freewheels through the body diode of Q_4. Switch Q_4 can be ON as a synchronous rectifier (SR) to reduce the conduction loss.
- Resonant state such as t_3–t_4: When i_{L2} reaches zero at t_3, C_{oss} and L_2 start resonating. Switch Q_3 turns ON again at t_4, when v_{ds3} is minimum. During this state, the fluctuation of v_O is assumed to be negligible.

These states repeat N_p times until the steady-state operation resumes and VMC regains control at t_5. The switching loss of Q_3 is minimized through valley switching. Switch Q_3 may turn ON with zero voltage if $V_{in} \leq 2V_O$.

When i_O is stepped down, the auxiliary converter operates as a PCM-controlled boost converter in CRM as shown in Fig. 2(b). Switch Q_4 acts as the main switch of the auxiliary boost converter to generate the triangular wave shapes of i_{L2} over a negative envelope, N_{env}. The switching period of the auxiliary converter also consists of three switching states:

- Inductor-charging state such as t_6–t_7: Current i_O decreases at t_6; Q_4 then turns ON, and i_{L2} linearly decreases from zero. Note that the negative i_L represents that the auxiliary converter works like a boost converter.
- Inductor-discharging state such as t_7–t_8: When i_{L2} reaches N_{env} at t_7, Q_4 turns OFF and i_{L2} increases and freewheels through the body diode of Q_3. Switch Q_3 can be ON as the SR to reduce the conduction loss.
- Resonant state such as t_8–t_9: When i_{L2} becomes zero at t_8, C_{oss} and L_2 resonate. Switch Q_4 turns ON again at t_9, when v_{ds4} is zero. During this state, the v_O variation is assumed to be negligible.

These states are repeated N_n times until the steady-state operation resumes and VMC recovers the control at t_{10}. Switch Q_4 turns ON with ZVS if $V_{in} > 2V_O$, while Q_1 is fully OFF and Q_2 is fully ON.

The main switches are assumed to be OFF when the transient period begins, i.e., Q_1 and Q_2 are OFF at t_1 and t_6, respectively, for the simple explanations. However, shaping i_{L2} by the proposed control technique is unaffected by the switching states of Q_1 and Q_2 at the beginning of the transient period. For example, if Q_1 has been ON until t_1 as shown in Fig. 3, Q_1 keeps its ON-state by the proposed control though i_O changes at t_1. Note that the waveform v_{gs1} in Fig. 3 is described by different patterns: the hashed area means that Q_1 is turned ON and OFF by the VMC block in Fig. 1(b); the shaded area indicates that Q_1 is controlled by the proposed control or the red blocks in Fig. 1(b). Similarly,

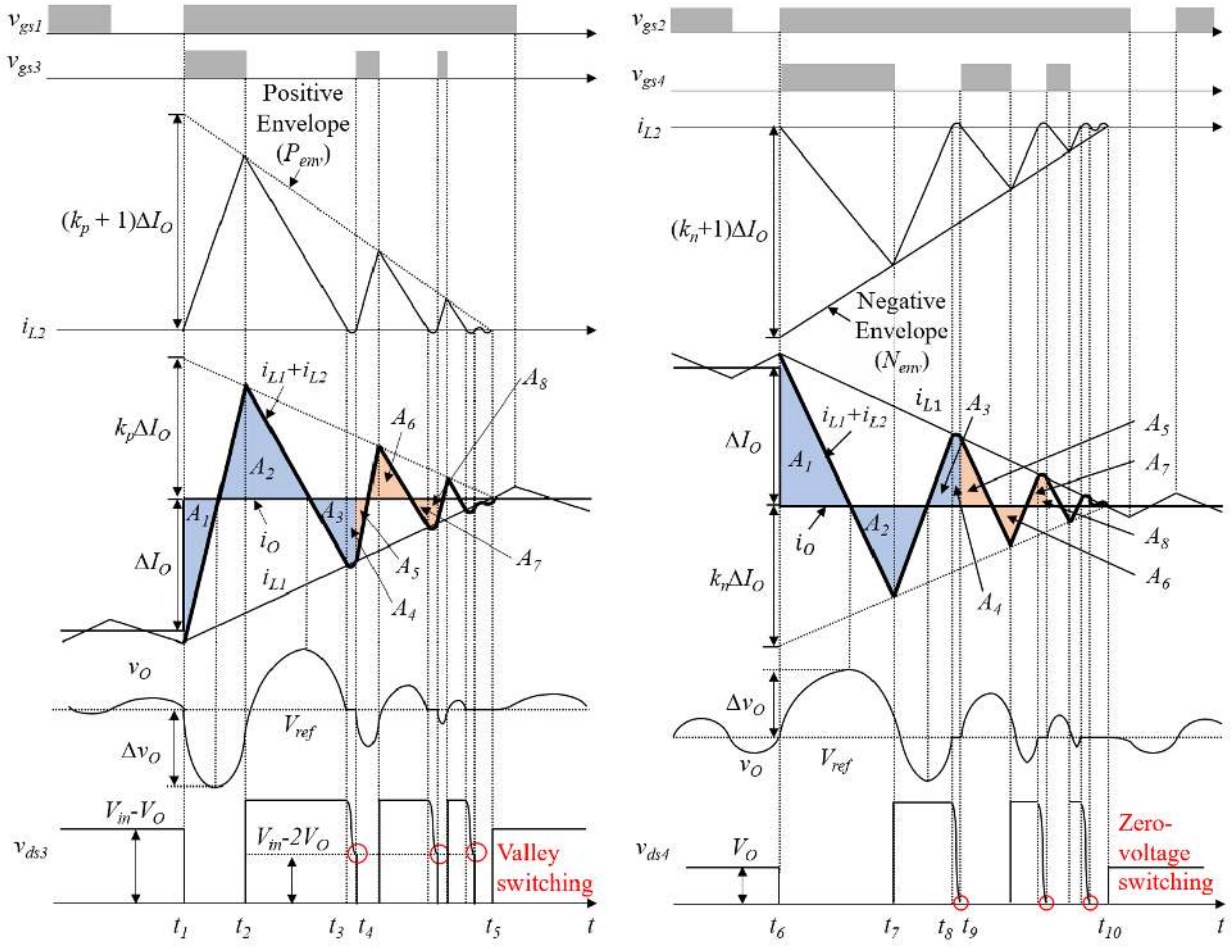

FIGURE 2. Key voltages and currents of proposed auxiliary current control: (a) when i_O is stepped up and $N_p = 3$; (b) when i_O is stepped down and $N_n = 3$.

Q_1 is kept OFF and Q_2 is kept ON regardless their previous ON/OFF state at the instant when i_O is stepped down.

Limiting switching cycles N_p and N_n are required to avoid an excessive switching frequency and switching loss of Q_3 and Q_4. If the voltage gain of the main buck converter is less than 0.5, the negative transient period t_6-t_{10} is longer than the positive period t_1-t_5, and thus N_n is larger than N_p. In this study, N_p and N_n were empirically set to 4 and 10, respectively, when ΔI_O step-changes between 4 A and 15 A.

The cycle-by-cycle CCB of the proposed control is explained with Fig. 4. Area A_i represents the amount of charge that is charged to or discharged from C_O, to which the v_O deviation is proportional. The coefficient k_p is set to maintain the CCB of C_O in each switching cycle, as follows:

$$A_i + A_{i+2} = A_{i+1} \quad (i = 1,\ 5,\ 9,\ \cdots) \tag{1}$$

The area A_{i+3} is not included in (1) because it is smaller enough than A_i, A_{i+1}, and A_{i+2} in practical implementation. Section III presents the derivation of k_p in detail. The undershoot Δv_O is solely determined by A_1 as in (2).

$$\Delta v_O = \frac{A_1}{C_O} = \frac{\Delta I_O^2 L_1 L_2}{2C_O\,(L_1 + L_2)\,(V_{in} - V_O)} \tag{2}$$

In practice, the overshoot or undershoot of v_O also depends on the instant of load change within the switching period of the main converter. For example, if i_O steps up while Q_1 is ON as illustrated in Fig. 3, Δv_O' is added to Δv_O to induce larger undershoot than shown in Fig. 2(b). However, Δv_O' is generally smaller enough than Δv_O and thus negligible thanks to the large capacitance of C_O.

The proposed technique is realizable in the multi-phase buck converters connected in parallel. The operation of the auxiliary converter can be emulated by idle-state phase converters, modulating the amplitude of envelopes along with the corresponding auxiliary inductance.

III. ANALYSIS OF PROPOSED AUXILIARY CURRENT CONTROL TECHNIQUE

A. HEIGHT OF ENVELOPE FOR CAPACITOR CHARGE BALANCE

As discussed in Section II, the amplitude of i_{L2} when i_O steps up is modulated by P_{env} as shown in Fig. 2(a). The height of P_{env} is equal to $(k_p{+}1)\Delta I_O$, and k_p is derived from the geometry of the $i_{L1} + i_{L2}$ and i_O shown in Fig. 4 to satisfy the cycle-by-cycle CCB or (1). The slopes $m_1 - m_4$ and lengths j_1,

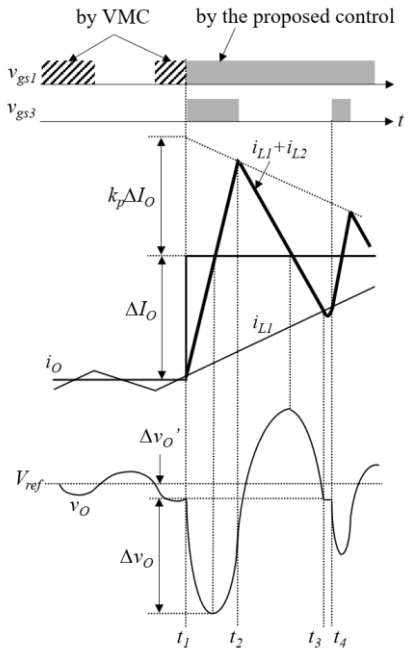

FIGURE 3. When i_O is stepped up while Q_1 is ON at t_1.

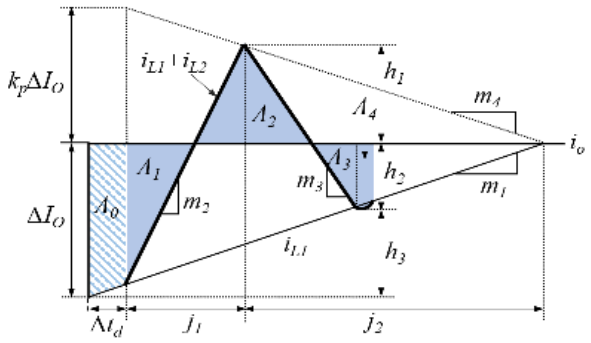

FIGURE 4. Current waveforms when i_O is stepped up to derive k_p; time Δt_d and area A_4 are inflated for clarity.

j_2, and h_1 satisfy (3)-(6) if the time delay Δt_d is zero. During the transient, the output voltage v_O is assumed to be constant with no ripple and denoted as V_O.

$$m_1 = \frac{V_{in} - V_O}{L_1} = \frac{\Delta I_O}{j_1 + j_2} \tag{3}$$

$$m_2 = \frac{V_{in} - V_O}{L_2} + m_1 = \frac{\Delta I_O + h_1}{j_1} \tag{4}$$

$$m_3 = -\frac{V_O}{L_2} + m_1 \tag{5}$$

$$m_4 = -k_p m_1 = -\frac{h_1}{j_2} \tag{6}$$

By manipulating (3)–(6), the height of A_2, h_1, is derived as (7).

$$h_1 = \frac{k_p \Delta I_O L_1}{L_1 + (1 + k_p) L_2} \tag{7}$$

Eq. (8) is also true based on the geometry of Fig. 4.

$$h_3 = \Delta I_O - h_2 = \left(\frac{\Delta I_O + h_1}{m_2} - \frac{h_1}{m_3} + \frac{h_1}{m_3} \right) m_1 \tag{8}$$

Substituting (7) into (8) yields (9).

$$h_2 = \frac{\Delta I_O}{V_O} \frac{L_1 V_O - (V_{in} - V_O)(1 + k_p) L_2}{L_1 + (1 + k_p) L_2} \tag{9}$$

Combining (3)-(6), (8), and (9) find that k_p is a function of V_{in}, V_O, L_1, and L_2, and is independent from ΔI_O as in (10).

$$k_p = \frac{L_1 V_O - L_2 (V_{in} - 2V_O)}{L_1 V_O + L_2 (V_{in} - 2V_O)} \tag{10}$$

The other constant k_n that determines the height of N_{env} when i_O is stepped down is obtained by similar manner as shown in (11).

$$k_n = \frac{L_1 (V_{in} - V_O) + L_2 (V_{in} - 2V_O)}{L_1 (V_{in} - V_O) - L_2 (V_{in} - 2V_O)} \tag{11}$$

B. ENVELOPE CONSIDERING TIME DELAY

In practical implementation, the first turn-on of Q_3 may be delayed by the time Δt_d from the instant that i_O steps up as shown in Fig. 4. The area of the trapezoid A_0 in Fig. 4 is expressed by (12).

$$A_0 = \left(\Delta I_O - \frac{\Delta t_d}{2} m_1 \right) \Delta t_d \tag{12}$$

The condition to meet the CCB in the first switching cycle becomes as in (13), neglecting A_4.

$$A_0 + A_1 - A_2 + A_3 = 0 \tag{13}$$

Eqs. (7) and (9) are rederived with nonzero Δt_d as (14) and (15), respectively.

$$h_1 = \frac{k_p (\Delta I_O - \Delta t_d m_1) L_1}{L_1 + (1 + k_p) L_2} \tag{14}$$

$$h_2 = \frac{(\Delta I_O - \Delta t_d m_1)}{V_O} \frac{L_1 V_O - (V_{in} - V_O)(1 + k_p) L_2}{L_1 + (1 + k_p) L_2} \tag{15}$$

For nonzero Δt_d, k_p does depend on ΔI_O. Fig. 5(a) shows the plot of k_p and k_n for various V_O under the conditions presented in Table 1. The plots are symmetric with respect to the vertical line $V_O = V_{in}/2$ (7.5 V in this study) when $\Delta t_d = 0$, because m_2 and m_3 are interchanged between the step-up and step-down cases of the load transient. Fig. 5(b) shows k_p and k_n versus ΔI_O when the parameters in Table 1 are employed. When $\Delta t_d = 0$, k_p and k_n are constant because they are independent of ΔI_O, as expressed by (10) and (11). The nonzero Δt_d increases both k_p and k_n. This increase becomes considerable when ΔI_O is relatively small, and negligible when ΔI_O is sufficiently large.

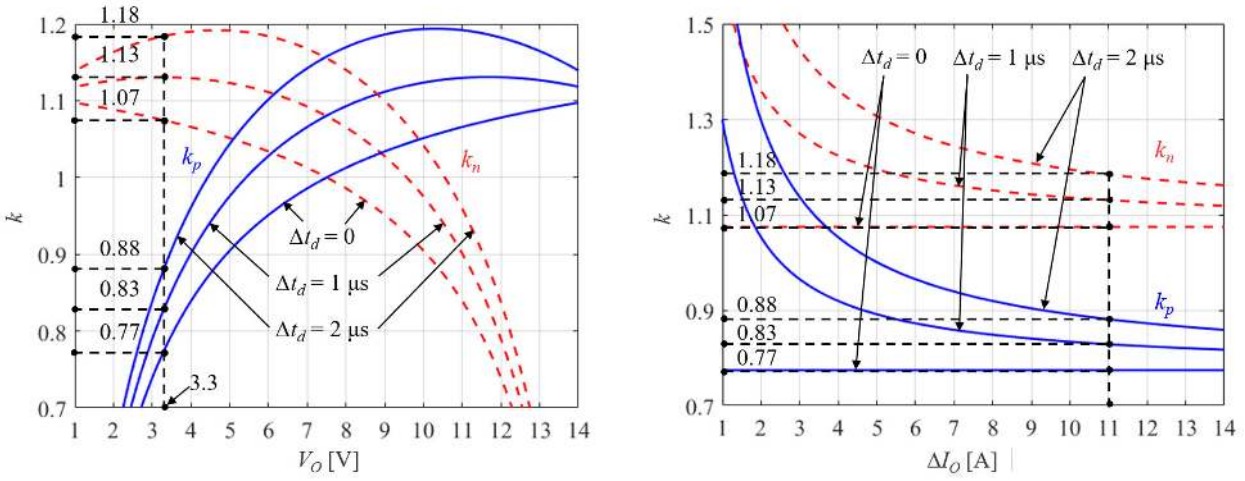

FIGURE 5. k_p (solid curves) and k_n (dotted curves) under conditions defined in Table 1: (a) versus v_O; (b) versus ΔI_O.

TABLE 1. Circuit parameters of simulation and experiment.

Parameter	Description
V_{in}	15 V
v_O	3.3 V
i_O	4 A-15 A
Switching frequency of Q_1 and Q_2	200 kHz
L_1	10 µH (74435581000 from Wurth Electronics)
L_2 and L_3	500 nH and 100 nH (both are air core)
C_O	220 µF
Q_1-Q_4	STP140N6F7 from STMicroelectronics (R_{on}=3.5 mΩ, C_{oss}=1.5 nF)
Gate drivers	IR2111SPBF from Infineon for Q_1 and Q_2 (typical propagation delay=750 ns), IRS2011SPBF from Infineon for Q_3 and Q_4 (typical propagation delay=60 ns)
Op-amp	LT1818CS5#TRPBF from Analog Devices (typical propagation delay=1 ns)
Comparator	LT1720IS8#PBF from Analog Devices (maximum propagation delay=1 ns)
Logic inverter	SN74LVC2G14DBVR from Texas Instruments (maximum propagation delay=4.7 ns)
NAND gate	74LVC2G00DP from Nexperia (maximum propagation delay=4.2 ns)
Set-reset latch	MC14043BDG from ON Semiconductor (maximum propagation delay=350 ns)
Single-pole-double-throw switch	ADG1633BRUZ from Analog Devices (maximum propagation delay=151 ns)

C. SIMULATION

Fig. 6 shows v_O, i_O, and $i_{L1} + i_{L2}$ of the proposed auxiliary current control with various Δt_d simulated by LTspice XVII under the conditions defined in Table 1. The minimum time step of 5 ns and an alternate solver were used in the simulation. According to Fig. 5(a), k_p should be 0.77, 0.83, and 0.88 when Δt_d is zero, 1 μs, and 2 μs, respectively. Similarly, k_n should be 1.07, 1.13, and 1.18 for zero, 1-μs, and 2-μs Δt_d, respectively, as marked in Fig. 5(b). However, k_p and k_n were set to be slightly smaller than these values to avoid the overcompensation of v_O.

Fig. 7 compares Δv_O of the VMC, TOC, and proposed control. The closed loop of the was designed to have 78.6° phase margin at the 12-kHz cutoff frequency by the PID type-3 compensator. When $\Delta I_O = 11$ A (4 A to 15 A) and $\Delta t_d = 1.2$ μs as shown in Fig. 7(a), the proposed control presented a 64-mV Δv_O. This value is much smaller than the those by TOC (211 mV) and VMC (321 mV). The settling time of the proposed method was as small as 14.5 μs, which is equivalent to 48% of that achieved by TOC (28.3 μs) and 78% of that achieved by VMC (68.2 μs). When i_O is stepped down ($\Delta I_O = 11$ A, 15 A to 4 A) and $\Delta t_d = 0.5$ μs, the proposed control technique, TOC, and VMC achieved 62-mV, 666-mV, and 731-mV Δv_O, respectively. The settling time of the proposed control was 29.4 μs while TOC and VMC showed 57.2 μs and 77 μs, respectively.

The dynamic performance of the proposed control was qualitatively compared with that of conventional auxiliary converter control methods. Fig. 8 shows the waveform of the stepping-up i_O and corresponding $i_{L1} + i_{L2}$ of the proposed method, controlled auxiliary current (CAC) scheme [19]–[21], and current-programmed mode (CPM) scheme [22]–[24] with the same L_2 and Δt_d. Obviously, the area A_1 determines Δv_O. The proposed and CPM schemes are expected to have the same Δv_O, while the CAC control should exhibit larger Δv_O.

D. ESTIMATED POWER LOSS OF THE AUXILIARY CONVERTER

In this section, the estimated power losses of the auxiliary converters are compared. The CAC [19]–[21] and CPM [22]–[24] schemes were again selected as the

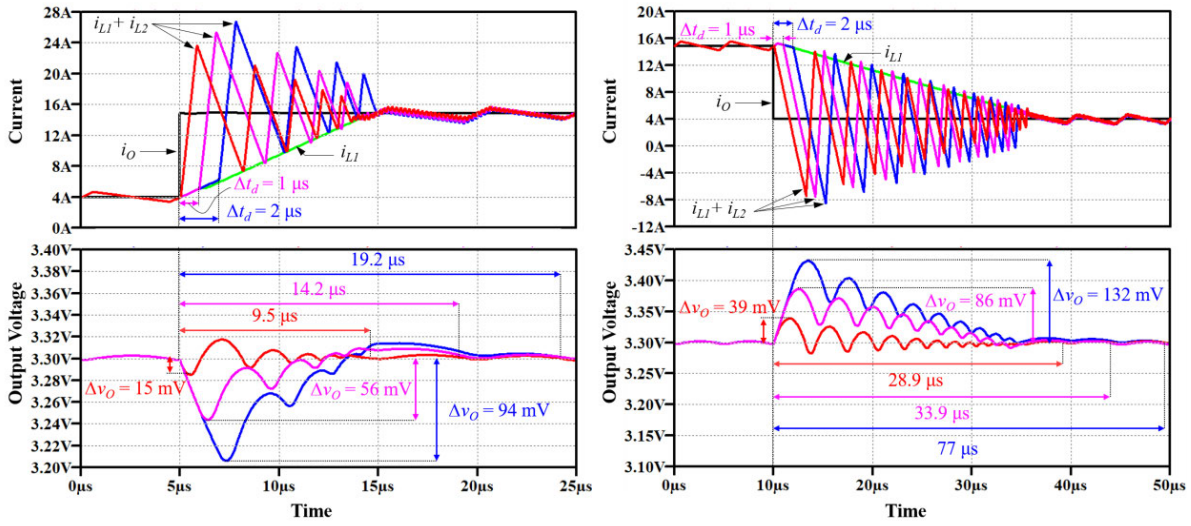

FIGURE 6. Simulated response of proposed control when the parameters in Table 1 are employed: (a) when i_O increases from 4 to 15 A, $N_p = 4-5$, and $\Delta t_d = 0$, 1 μs, and 2 μs; (b) when i_O decreases from 15 to 4 A, $N_n = 10$-12, and $\Delta t_d = 0$, 1 μs, and 2 μs.

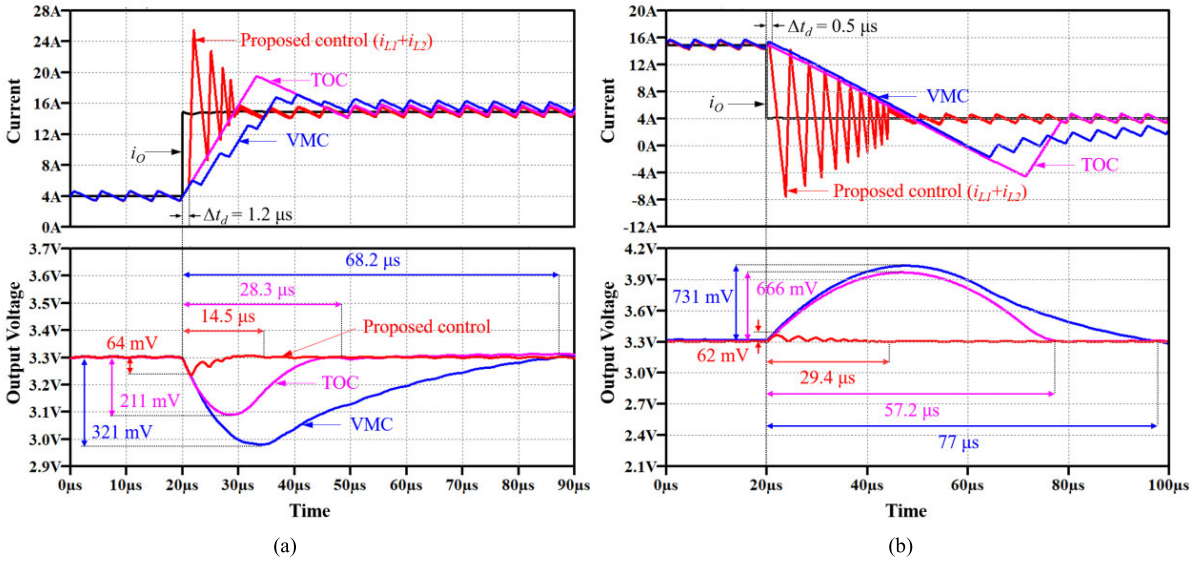

FIGURE 7. Simulated responses of proposed control, TOC, and VMC when the parameters in Table 1 are employed: (a) when i_O increases from 4 to 15 A, $N_p = 4$, and $\Delta t_d = 1.2$ μs; (b) when i_O decreases from 15 to 4 A, $N_n = 10$, and $\Delta t_d = 0.5$ μs.

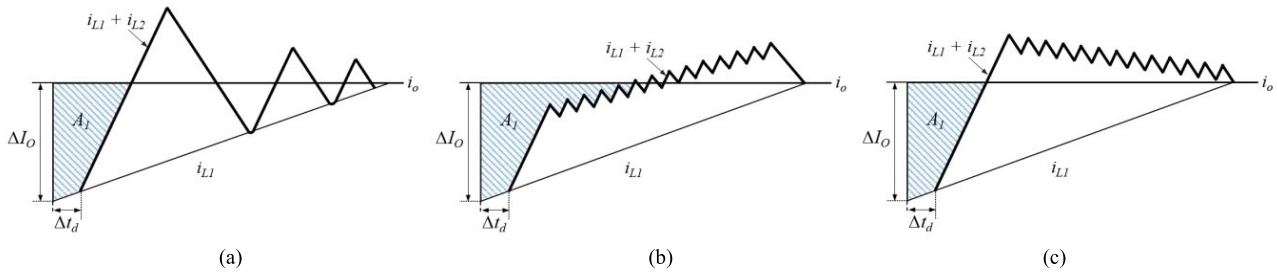

FIGURE 8. Comparison of current waveforms: (a) proposed control; (b) CAC control [19]–[21]; (c) CPM control [22]–[24].

conventional counterparts due to their similarity to the proposed control: nonresistive auxiliary circuits and the auxiliary current that is controlled to satisfy CCB. All conditions except that the constant switching frequency of the CAC and CPM is 2 MHz were held the same with the proposed method for a fair comparison.

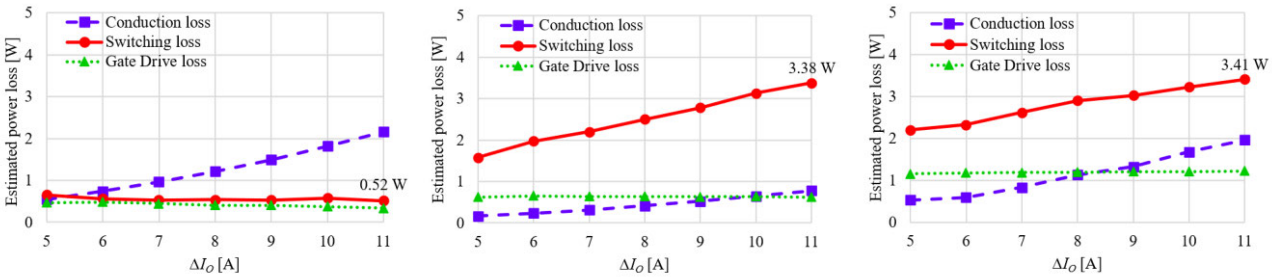

FIGURE 9. Comparison of estimated total power loss of auxiliary circuit versus magnitude of current load variation; conduction loss of lines (blue dashed curves); switching loss (red solid curves); gate drive loss (green dotted curves): (a) proposed control; (b) CAC control [19]–[21]; (c) CPM control [22]–[24].

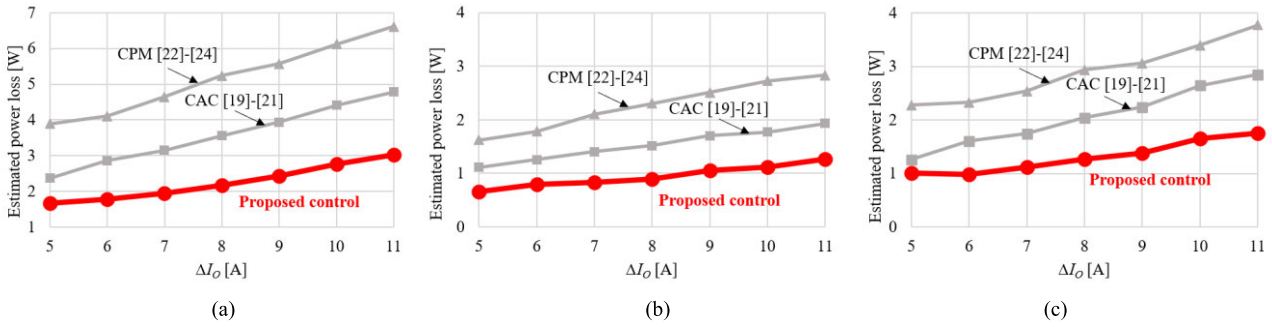

FIGURE 10. Comparison of estimated power loss of auxiliary circuit associated with proposed, CAC [19]–[21], and CPM control [22]–[24]: (a) total power loss when the load current steps up and down by the same magnitude, ΔI_O. (b) when i_O is stepped up; (c) when i_O is stepped down.

Fig. 9 shows that the conduction (blue dashed curves), switching (red solid curves), and gate drive loss (green dotted curves) of the investigated control methods under variable loading. The losses depend on the control scheme, ΔI_O.

- Gate drive loss: The gate drive loss of the proposed control was approximately half the gate drive loss of CPM owing to the lower number of switching cycles. To compare the proposed scheme to CAC, the number of active auxiliary MOSFETs should first be counted. Two MOSFETs operate during the transient in the proposed scheme, while only one MOSFET operates in CAC. However, the proposed scheme had a slightly smaller gate driver loss because the number of switching cycles of the proposed control, N_p or N_n, was much less than that of CAC.
- Switching loss: The proposed control achieves the lowest power loss among the control schemes thanks to its zero-voltage or soft switching and the limited number of switching cycles of the auxiliary converter. Regardless of ΔI_O, the proposed method maintained switching loss around 0.5 W, which is smaller than those of CAC and CPM. The switching loss reduction becomes more evident as ΔI_O increases. In the case of 11-A ΔI_O, the estimated switching loss of the proposed control was 0.52 W while those of CAC and CPM were 3.38 W and 3.41 W, respectively.
- Conduction loss: The proposed control presents the larger conduction loss than CAC and CPM. This is analogous to the feature of CRM and continuous-conduction-mode operations of general DC-DC converters. However, the comparison of the total loss reveals that the soft switching saved more power than this increased conduction loss.

The total loss of the control methods for various ΔI_O is plotted in Fig. 10(a), and broken down into Fig. 10(b) and 10(c) to show the losses at step-up and -down of i_O separately. Again, the proposed control scheme exhibited the lowest loss owing to the soft switching of Q_3 and ZVS of Q_4. The equations used to estimate the auxiliary circuit loss are presented in Appendix.

IV. IMPLEMENTATION OF THE PROPOSED CONTROL

The proposed control can be realized in various ways. In this study, the analog control circuit shown in Fig. 11 was built for experimental verification. The names of the IC parts are listed in Table 1. The currents i_O, i_{L1}, and i_{L2} were sensed by 2-mΩ shunt resistances, R_s. The AND and OR logics were realized by combining multiple NAND gates presented in Table 1. The signal processing in Fig. 11 is explained block-by-block.

A. VOLTAGE MODE CONTROLLER

In the steady-state operation, the auxiliary converter is idle and only the main converter works. The VMC was implemented for the steady-state control of the main converter by TL5001 and its peripheral circuits. The dynamic response of the closed-loop gain was the same as that in the simulation described in Section III-C.

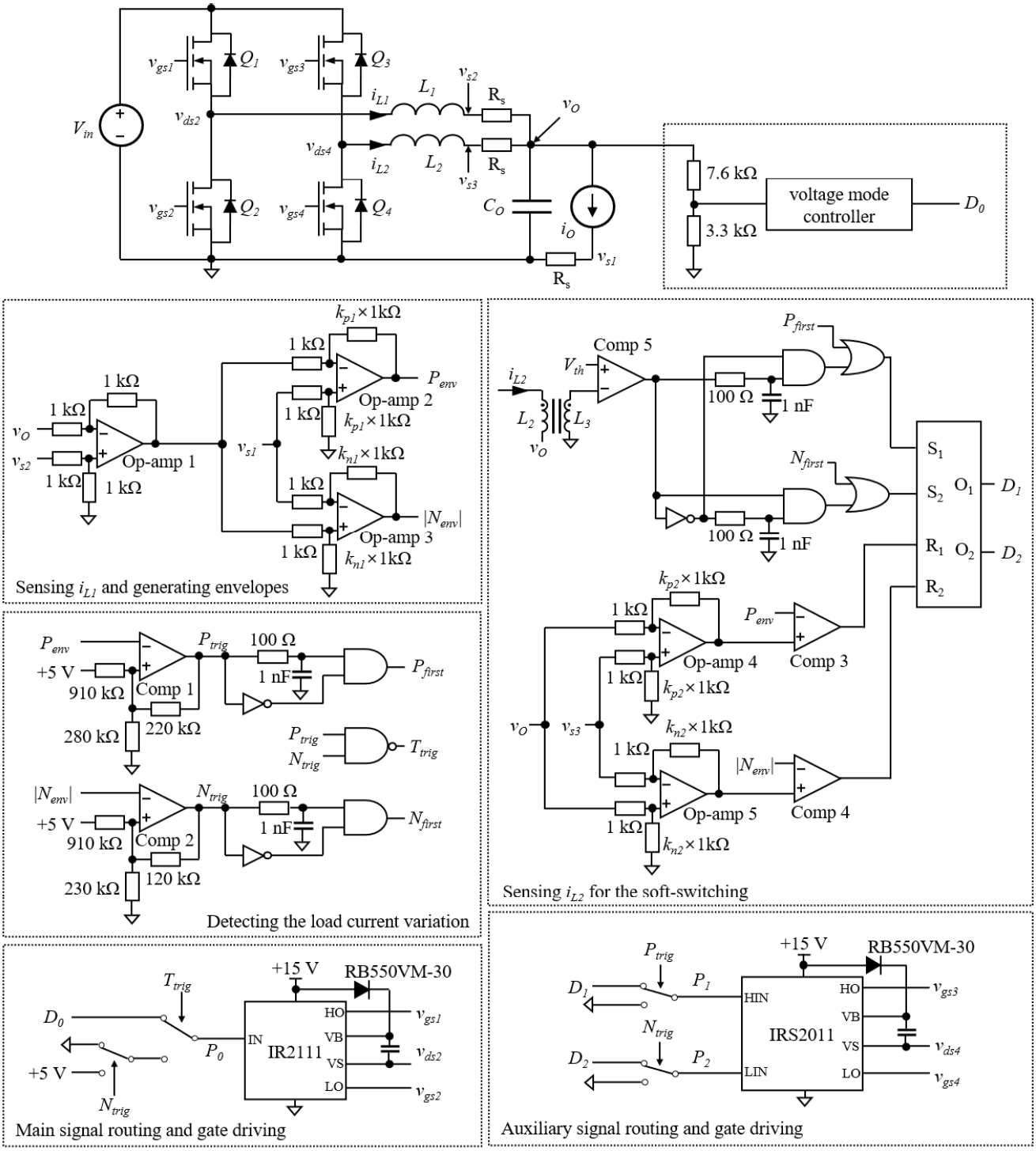

FIGURE 11. Prototype circuit to realize the proposed control technique.

B. SENSING i_L AND GENERATING ENVELOPES

The gains of op-amps 2 and 3 are denoted as k_{p1} and k_{n1} and expressed in (16) and (17), respectively.

$$k_{p1} = (1 + k_p)\, k_{p2} \tag{16}$$

$$k_{n1} = (1 + k_n)\, k_{n2} \tag{17}$$

In (16) and (17), k_{p2} and k_{n2} are the gains of op-amps 4 and 5, respectively.

With the unity gain, the output of op-amp 1 is equal to $i_{L1}R_s$. The voltage v_{s1}, which is equal to $i_O R_s$, is the input to op-amps 2 and 3 to generate P_{env} and $|N_{env}|$. The currents in the power stage and the envelopes have the relationship as

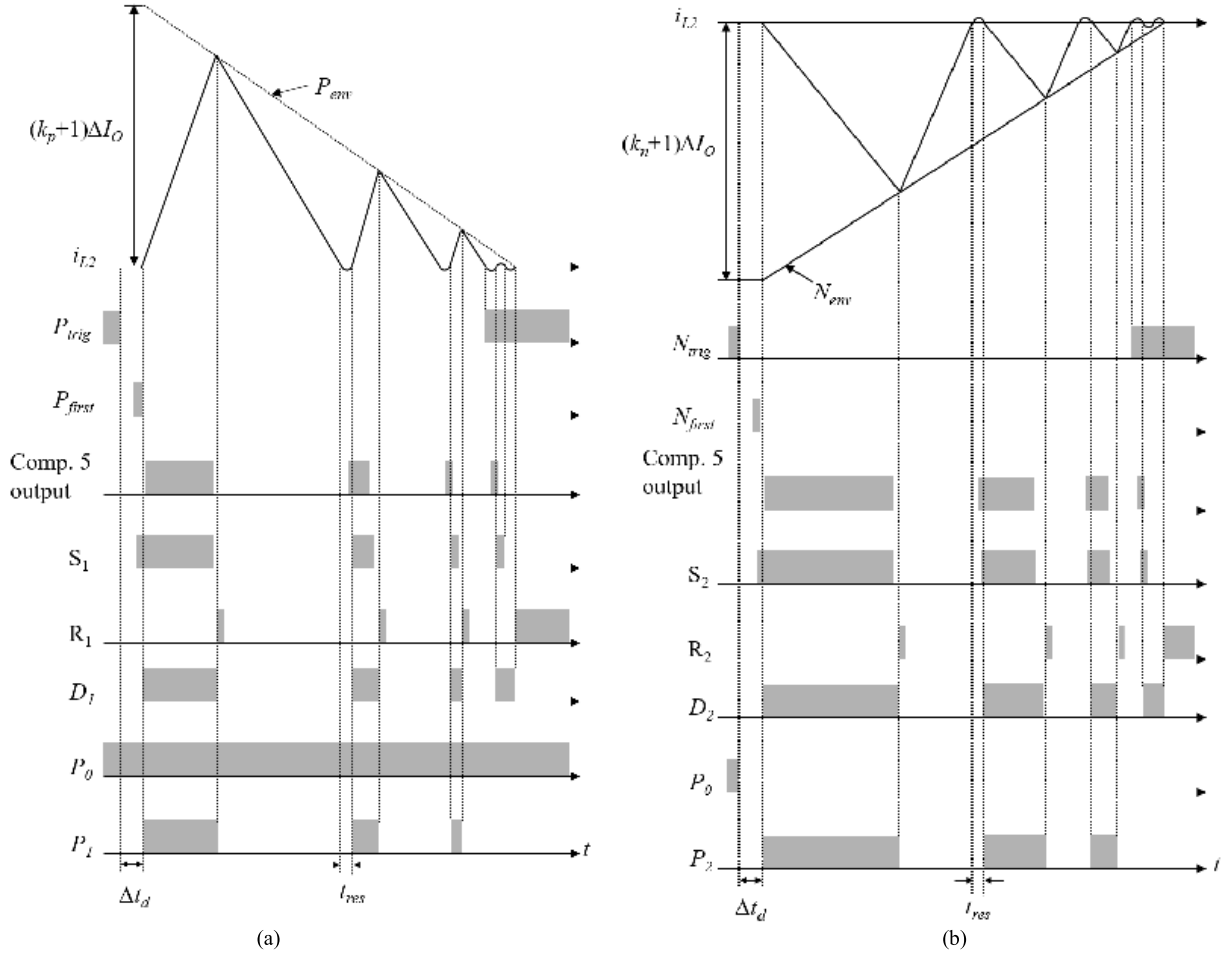

FIGURE 12. Control signal waveforms of proposed control scheme: (a) when i_O is stepped up ($N_p = 3$); (b) when i_O is stepped down ($N_n = 3$).

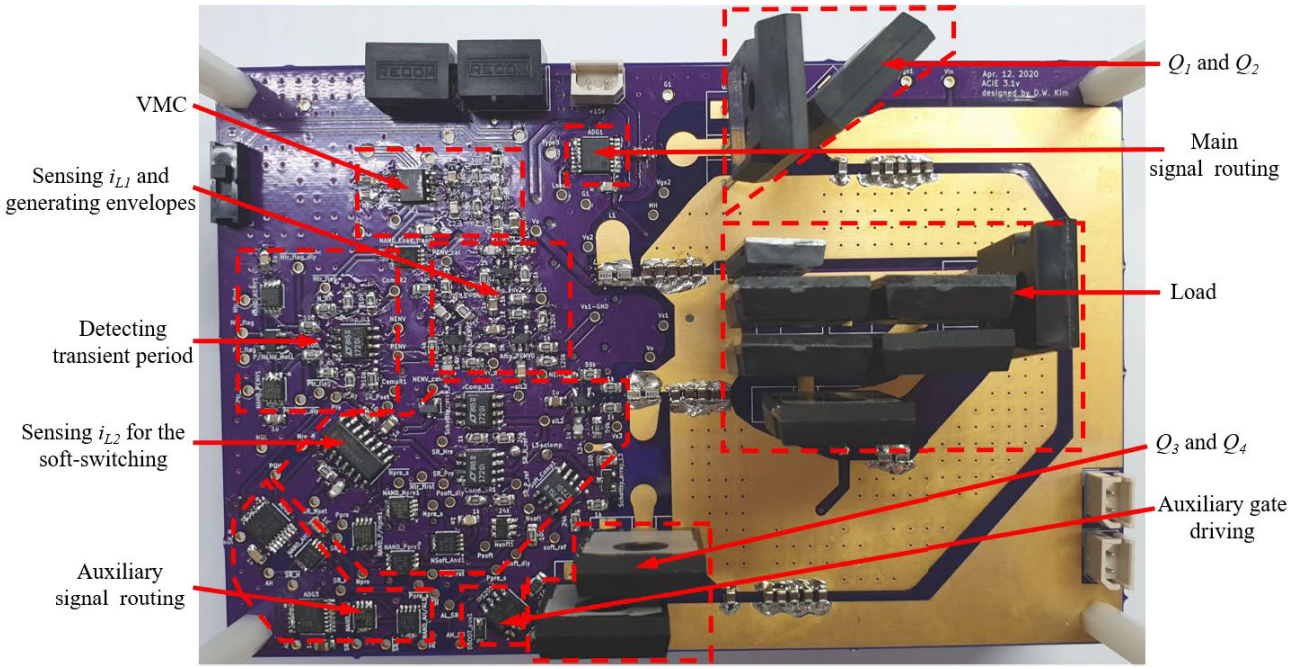

FIGURE 13. Photograph of experimental prototype circuit.

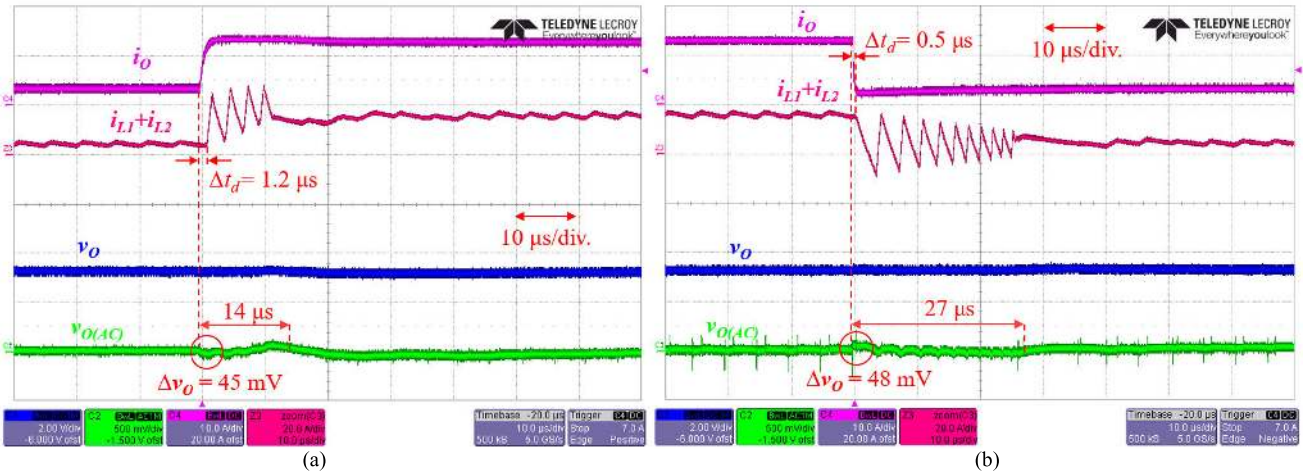

FIGURE 14. Response of proposed control technique; trace i_O (magenta) is in 10 A/div.; trace $i_{L1} + i_{L2}$ (red) is in 20 A/div.; trace v_O (blue) is in 2 V/div.; trace $v_{O(AC)}$ (green) is in 500 mV/div. With AC coupling; time scale is 10 μs/div. (a) When i_O was stepped up from 4 A to 15 A with $N_p = 4$. (b) when i_O was stepped down from 15 A to 4 A with $N_n = 10$.

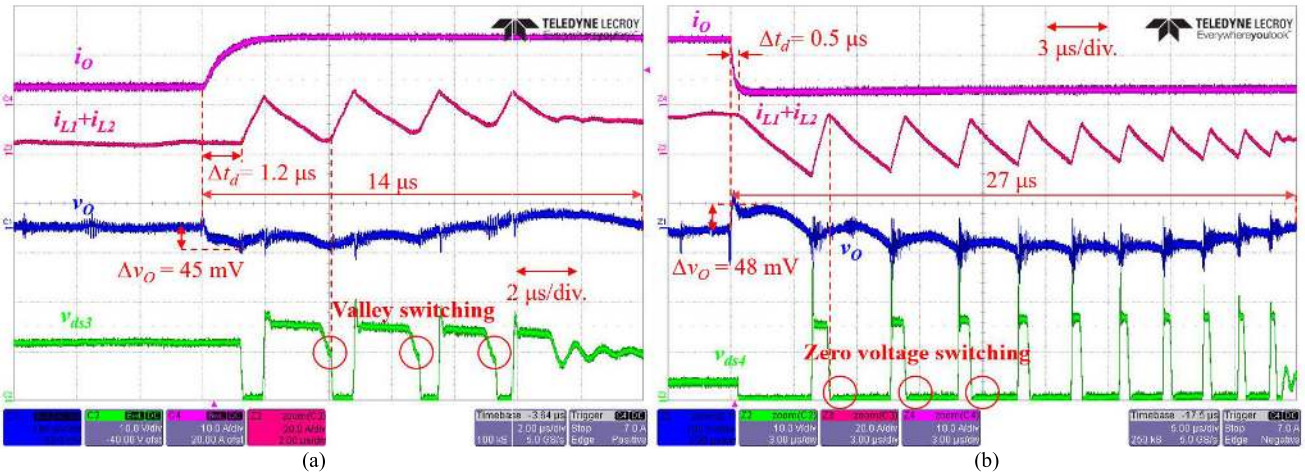

FIGURE 15. Experimental waveforms of proposed control technique; trace i_O (magenta) is in 10 A/div.; trace $i_{L1} + i_{L2}$ (red) is in 20 A/div.; trace v_O (blue) is in 100 mV/div. With AC coupling; trace v_{ds3} or v_{ds4} (green) are in 10 V/div. (a) when i_O was stepped up from 4 A to 15 A with $N_p = 4$; time scale is 2 μs/div. (b) when i_O was stepped down from 15 A to 4 A with $N_n = 10$; time scale is 3 μs/div.

shown in (18) and (19).

$$P_{env} = (i_O - i_{L1})\, R_s k_{p1} \tag{18}$$

$$|N_{env}| = (i_{L1} - i_O)\, R_s k_{n1} \tag{19}$$

C. DETECTING THE LOAD CURRENT VARIATION

Envelopes P_{env} and $|N_{env}|$ are fed into the hysteresis comparators 1 and 2, respectively. The feedback resistors of the comparators were tuned to set the number of switching cycles of the auxiliary converter, N_p and N_n. The outputs of the comparators, P_{trig} and N_{trig}, are active-low: the auxiliary converter is activated when P_{trig} or N_{trig} is low.

The first turn-on of Q_3 when i_O stepped up is triggered by P_{first} which is generated by P_{trig}. The RC filter and AND gate connected to the output terminal of comparators 1 and 2 form a falling-edge-triggered monoflop. Similarly, the first turn-on of Q_4 when i_O stepped down is realized by N_{first}.

It is important to generate P_{first} and N_{first} as quickly as possible to minimize Δt_d and thus Δv_O as mentioned in Section III-B. In the analog implementation described in this paper, Δt_d depends on the dynamic characteristics of the op-amps, comparators, and logic gates.

The signal T_{trig} is made by NANDing P_{trig} and N_{trig} and used in the signal routing and gate driving block.

D. SENSING i_{L2} FOR THE SOFT-SWITCHING

The second and subsequent turn-ons of the auxiliary switches are controlled to enable the soft switching. For example, turning ON Q_3 begins by sensing i_{L2} through a coupled inductor L_3. The output signal of comparator 5 is fed into a logic inverter and RC filters that compose another monoflops. The resistors and capacitors were tuned as 100 Ω and 1 nF, respectively, to generate the delay t_{res} in (20) to ensure the

soft switching of Q_3 or Q_4.

$$t_{res} \cong \pi\sqrt{L_2 C_{oss}} \tag{20}$$

Turning OFF Q_3 and Q_4 during the transient period was realized by op-amps 4 and 5 and comparators 3 and 4. The output of the op-amps 4 and 5 is proportional to i_{L2}, as expressed by (21) and (22).

$$(\text{output of op-amp 4}) = i_{L2} R_s k_{p2} \tag{21}$$

$$(\text{output of op-amp 5}) = -i_{L2} R_s k_{n2} \tag{22}$$

The output of op-amp 5 is positive because i_{L2} is negative during the transient caused by stepping-down i_O in (22). If the output of op-amp 4 exceeded P_{env}, Q_3 is turned OFF. Similarly, Q_4 turns OFF when the output of the op-amp 5 touches $|N_{env}|$.

E. MAIN SIGNAL ROUTING AND GATE DRIVING

During the steady-state operation, the gate signals for Q_1 and Q_2 are produced by the output of VMC, D_0. When the load transient is detected, fully-OFF command (0 V) or fully-on command (5 V) overrides D_0 by the single-pole-double-throw switches controlled by T_{trig} and N_{trig}. This overridden signal, P_0, which is 5 V when i_O is stepped up or 0 V when i_O is stepped down, is transmitted to the gate driver IR2111. Voltages v_{gs1} and v_{gs2} are complementary with a fixed dead time of 650-ns of IR2111.

F. AUXILIARY SIGNAL ROUTING AND GATE DRIVING

Voltages v_{gs3} and v_{gs4} are generated during the transients only. The outputs of the SR latch, D_1, and D_2, are routed to the gate driver by P_{trig} and N_{trig}. Unlike v_{gs1} and v_{gs2}, v_{gs3} and v_{gs4} are not complementary but rather independent of each other. For example, the time interval t_{res} in (20) should exist between the falling edge of v_{gs4} and the rising edge of v_{gs3} for the valley switching of Q_3 when i_O steps up. A high-side gate driver IRS2011 was used to produce v_{gs3} and v_{gs4}.

Fig. 12 shows the key signal waveforms of the control circuit in Fig. 11 during the transient. The low state of the signals is 0 V. The high state of the signals, except P_1 and P_2, represents 5 V, while those of P_1 and P_2 are 15 V.

The top view of the experimental prototype circuit is shown in Fig. 13. The prototype was configured using discrete analog ICs, such as op-amps, comparators, and logic gates, as presented in Table 1. The main gate driver was assembled on the bottom surface of the 4-layer PCB. Digital processors or complicated arithmetic ICs were not used. Realization of the variable load current is explained in the Appendix.

Note that Q_3 and Q_4 merely affect the power density. Generally, the power density of a converter is degraded not by the semiconductor devices themselves but by their cooling devices such as bulky heat sinks and fans. In the proposed control technique, the operating temperature of Q_3 and Q_4 is limited by two rationales: one is the low-loss soft switching, and the other is the limited number of switching cycles within a short time interval, i.e., transient operation. This allows Q_3 and Q_4 to have small or even no heat sinks to minimize the impact on the power density.

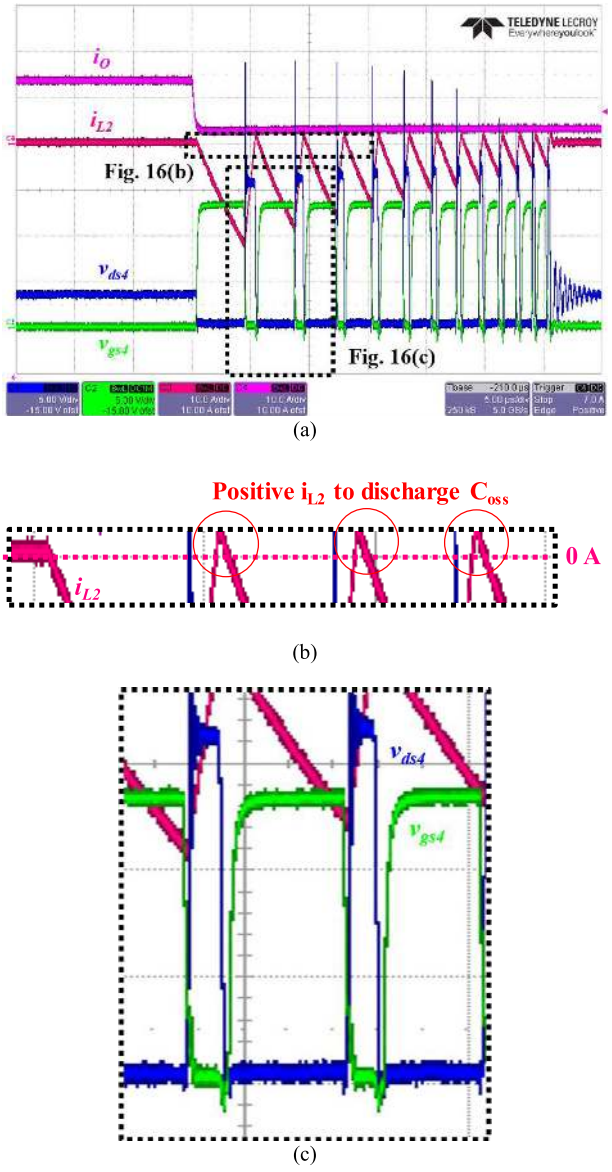

FIGURE 16. Experimental waveforms of proposed control technique to investigate the operation of Q_4. (a) Transient operation when i_O was stepped down from 15 A to 4 A. Traces i_O (magenta) and i_{L2} (red) are in 10 A/div.; traces v_{ds4} (blue) and v_{gs4} (green) are in 5 V/div. (b) Zoomed-in waveform of i_{L2}. (c) Zoomed-in waveform of v_{ds4} and v_{gs4}.

The main MOSFETs Q_1 and Q_2 may need heat management for the continuous operation, unlike the Q_3 and Q_4. However, Q_1 and Q_2 in Fig. 13 did not employ any cooling devices such as heat sinks because the operation of the prototype was limited less than a couple of seconds, which are enough to test the load transient.

V. EXPERIMENTAL RESULTS

Fig. 14 shows the experimental results for i_O (magenta trace), $i_{L1} + i_{L2}$ (red), and v_O (blue) of the proposed control scheme when i_O was stepped up (Fig. 14(a)) and down (Fig. 14(b)), respectively. The waveforms of the

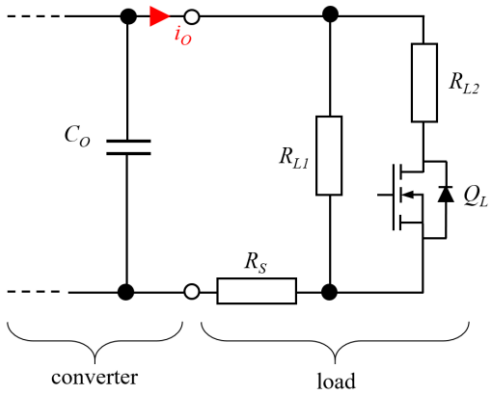

FIGURE 17. Switched resistor to realize i_O.

output voltage were approximately constant during the load transient.

Fig. 15 shows the experimental waveform of i_O (magenta trace), $i_{L1} + i_{L2}$ (red), v_O (blue), and v_{ds3} and v_{ds4} (green) of the proposed control scheme when i_O was stepped up or down, respectively. The delay Δt_d was 1.2 μs at step-up and 0.5 μs at step-down as in the simulation discussed in Section III-C. The waveshapes are analogous to the simulated ones shown in Figs. 7(a) and 7(b) with $N_p = 4$ and $N_n = 10$, respectively. The measured undershoot of 45 mV in Fig. 15(a) is smaller than the simulated undershoot of 64 mV in Fig. 7(a), because i_O did not transition in a perfect step. The settling time was 14 μs, which is similar to the simulated time of 14.5 μs in Fig. 7(a). As can be seen, Q_3 valley-switched to reduce the switching loss and noise. In Fig. 15(b), the measured overshoot of 48 mV and settling time of 27 μs were also smaller than the 62 mV and 29.4 μs in Fig. 7(b), for the same reason as when i_O was stepped up. The Q_4 was zero-voltage-switched, which reduced the switching loss and noise during the load step-down transient.

The lossless turn-on of Q_4 when i_O steps down is further verified by Fig. 16. Traces of Fig. 16(a) are i_O (magenta trace), i_{L2} (red), v_{ds4} (blue), and v_{gs4} (green). One can observe the positive i_{L2} in the zoomed-in waveform shown in Fig. 16(b). This positive current discharges C_{oss} to enable the ZVS of Q_4. Another clue of ZVS is that v_{ds4} becomes zero before the rising edge of v_{gs4} occurs as shown in Fig. 16(c).

VI. CONCLUSION

Control technique of the auxiliary buck/boost converter was implemented to improve the load transient response of the main buck converter. The proposed scheme shapes the auxiliary inductor current by PCM in CRM. It minimizes both the overshoot/undershoot of the output voltage and the power loss of the auxiliary circuit through the zero-voltage- or soft-switching auxiliary switches. The calculated power loss of the proposed method is 45%-60% of those of conventional control methods such as CAC and CPM.

A control circuit was built by combining op-amps, comparators, logic gates, and other passive peripheral components. No digital ICs or complicated arithmetic analog ICs were used for the simplicity of the hardware. This control circuit was tested with the prototype buck converter of which input voltage, output voltage, and the switching frequency (main buck converter) is 15 V, 3.3 V, and 200 kHz, respectively. Experimental results were coherent with the simulation: when the load current was stepped up from 4 A to 15 A, the undershoot was 45 mV and the settling time was 14 μs; when the load current was stepped down from 15 A to 4 A, the overshoot was 48 mV and settling time was 27 μs. During the transition, all the auxiliary switches maintained the soft switching.

APPENDIX

As mentioned in Section III-D, the power losses of the auxiliary circuit can be categorized into three: conduction, switching, and gate drive loss.

A. CONDUCTION LOSS

Conduction loss, $P_{con(aux)}$, occurs at the junction of Q_3 and Q_4, and the winding of L_2 is express in (23).

$$P_{con(aux)} = I^2_{Q_1(rms)} R_{on1} + I^2_{Q_2(rms)} R_{on2} + I^2_{L_2(rms)} R_{L_2} \quad (23)$$

where $I_{Qi(rm)}$, and R_{oni} are the root-mean-square (RMS) current and ON-state resistances of i^{th} MOSFET, respectively. The conduction loss of the body diodes is assumed to be negligible because Q_3 during the step-down transient and Q_4 during the step-up transient operate as SR. Literals $I_{L2(rms)}$ and R_{L2} are the RMS current and equivalent series resistance of the auxiliary inductor, respectively.

B. SWITCHING LOSS

The switching losses ($P_{sw(aux\_high)}$ and $P_{sw(aux\_low)}$) for the auxiliary MOSFETs in the proposed control can be derived using (24) and (25). Because the first switching of the proposed control is a hard turn-on, the first terms on the right-hand side of (24) and (25) are explicitly expressed. The turn-on switching loss of the auxiliary high-side MOSFET turns ON with valley switching and appears as the second term in (24). The turn-on switching loss of the auxiliary low-side MOSFET is assumed zero owing to the ZVS. In the CAC and CPM, the auxiliary MOSFETs turn ON with hard switching and their switching losses can be obtained using (26) and (27).

In (24)-(27), as shown at the top of the next page, T_t, N, T_{on}, and T_{off} are the load transient period, number of switching cycles, time duration of ON-transition, and time duration of OFF-transition of the auxiliary MOSFET, respectively. Literals $V_{ds,on,n}$, $V_{ds,off,n}$, $I_{on,n(rms)}$, and $I_{off,n(rms)}$ denote the drain-source voltage during the ON-transition at the n^{th} switching, drain-source voltage during the OFF-transition at the n^{th} switching, RMS current during the ON-transition of the auxiliary MOSFET at the n^{th} switching, and RMS current during the OFF-transition of the auxiliary MOSFET at the n^{th} switching. According to (24)-(27), the estimated switching

$$P_{sw(aux\_high)} = \frac{1}{2T_t}\left[(V_{in} - V_O)\, I_{on\_1(rms)} T_{on} + \sum_{n=2}^{N}\left\{(V_{in} - 2V_O)\, I_{on\_n(rms)} T_{on}\right\} + \sum_{n=1}^{N}\left(V_{in} I_{off\_n(rms)} T_{off}\right)\right] \tag{24}$$

$$P_{sw(aux\_low)} = \frac{1}{2T_t}\left[V_O I_{on\_1(rms)} T_{on} + \sum_{n=1}^{N}\left(V_{in} I_{off\_n(rms)} T_{off}\right)\right] \tag{25}$$

$$P_{sw(aux\_high)} = \frac{1}{2T_t}\left[(V_{in} - V_O)\, I_{on\_1(rms)} T_{on} + \sum_{n=2}^{N}\left(V_{in} I_{on\_n(rms)} T_{on}\right) + \sum_{n=1}^{N}\left(V_{in} I_{off\_n(rms)} T_{off}\right)\right] \tag{26}$$

$$P_{sw(aux\_low)} = \frac{1}{2T_t}\left[V_O I_{on\_1(rms)} T_{on} + \sum_{n=2}^{N}\left(V_{in} I_{on\_n(rms)} T_{on}\right) + \sum_{n=1}^{N}\left(V_{in} I_{off\_n(rms)} T_{off}\right)\right] \tag{27}$$

loss of the proposed control was 0.52 W, and CAC and CPM were 3.38 W and 3.41 W when ΔI_O is 11 A, respectively.

C. GATE DRIVE LOSS

The gate drive loss ($P_{gd(aux)}$) is caused by the gate charge of MOSFET, as expressed by (28)

$$P_{gd(aux)} = \frac{NQ_g V_{gs}}{T_t} \tag{28}$$

where Q_g and V_{gs} are the gate electric charge and ON-state gate-source voltage of the MOSFET, respectively. The switching number N is either N_p or N_n.

D. IMPLEMENTATION OF VARIABLE LOAD CURRENT

Variable load current may be emulated by DC electronic loads if the required slew rate of the current or *di/dt* is a couple of amperes per microsecond or lower. However, this *di/dt* is not enough for the step-changing load current, such as i_O in this work. A switched resistor network shown in Fig. 17 was built to realize i_O. Resistors R_{L1} and R_{L2} were the non-inductive resistors integrated in TO-220 and TO-247 package by Caddock Electronics. Three semiconductor switches such as Si MOSFET, Si IGBT, and SiC FET were tried as the switch Q_L in Fig. 17. The SiC FET (C3M0065090D by Cree) showed the highest *di/dt* among these and was utilized in the experiment presented in Section V.

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DONGWOOK KIM received the B.S. degree in electrical engineering from Dong-Eui University, Busan, South Korea, in 2019. He is currently pursuing the M.S. degree in energy systems engineering with Chung-Ang University, Seoul, South Korea. His research interests include dc-dc converter, power conversion system and its control, and power semiconductor packaging.

JONGUN BAEK is currently pursuing the B.S. degree with the School of Energy Systems Engineering, Chung-Ang University, Seoul, South Korea. His research interests include power conversion, converter control, and power semiconductor.

JISU LEE is currently pursuing the B.S. degree with the School of Energy Systems Engineering, Chung-Ang University, Seoul, South Korea. His research interests include the modeling, control, and soft-switching of power converters.

JOONHO SHIN is currently pursuing the B.S. degree with the School of Energy Systems Engineering, Chung-Ang University, Seoul, South Korea. His research interests include digital power conversion and power factor correction.

JONG-WON SHIN (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2006 and 2013, respectively. From 2013 to 2015, he was a Postdoctoral Researcher with Virginia Tech, Blacksburg, VA, USA. From 2015 to 2018, he was a Senior Scientist with the Electronics Research Department, Toyota Research Institute of North America, Ann Arbor, MI, USA. He is currently an Assistant Professor with the School of Energy Systems Engineering, Chung-Ang University, Seoul. His research interests include power conversion, energy management, and power semiconductor packaging.