IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 5, Ver. I (Sep-Oct. 2014), PP 01-05
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Implementation of Transistor Stacking Technique in Combinational Circuits

Ankita Nagar, Vidhu Parmar

***Abstract*:** *This paper deals with the reduction of power dissipation in the basic logic circuit like NAND gate and NOR gate by using transistor stacking technique. The logic gates are designed using 130nm technology parameter and are simulated using PSPICE. The input vector combinations are compared with the simulated result on the basis of propagation delay and power consumption. It is found that when the number of low-input increases in case of NAND gate the power dissipation decreases but the delay increases and for NOR gate power dissipation decreases with the increase in high input vector combinations.*

Index Terms: *Low Power, Propagation Delay, Power Dissipation, Sub-threshold current, stacking effect.*

I. Introduction

With the rapid progress in semiconductor technology, chip density has increased. This scaling of transistor feature sizes has provided a remarkable advancement with the increase in speed and frequency of operation and hence higher performance is achieved but the power dissipation also increases. High power dissipation reduces the battery service life. Therefore, power dissipation has become critical concern in today's VLSI system design.

Lowering the supply voltage (V_{DD}) is the most effective way to reduce the power dissipation as it depends quadratically on $V_{DD.}$ But as V_{DD} reduces, circuit delay will increase and thus degrades its performance. At the same time it is possible to maintain the performance by decreasing the threshold voltage (V_{TH}) but then sub-threshold leakage power increases exponentially. Therefore, V_{DD} and V_{TH} have to be optimized to achieve the required performance and low power. As the feature size reduces shorter channel length results in sub threshold leakage current through a transistor when it is off. Thinner gate oxides have led to an increase in gate leakage current. Therefore, static power consumption i.e. leakage power dissipation becomes an important portion of total power consumption. In 180 nm and below technologies, leakage accounts for 30-40% of total power.

This paper is summarized as follows: Section II gives brief introduction about sources of power dissipation. Section III discusses stacking technique to reduce the power dissipation. Section IV consists of the proposed work and result comparison.

II. Sources Of Power Dissipation

IC power dissipation consists of different components depending on the circuit operating mode.

A. Active Component

Dynamic switching power and short circuit power are active component of power dissipation. These occurs due to transitions at gate terminals which is caused by charging and discharging of capacitors in the circuit.

$$P_{dynamic} = C_L V_{DD}^2 f$$

B. Standby Component

Static biasing power and leakage power are standby component of power dissipation. These occurs in weak inversion region when gate-to-source voltage is less than threshold voltage.

$$I_{SUB} = Ae^{\frac{q}{nkT}(V_{GS} - V_{THO} - \gamma V_{SB} + \eta V_{DS})}(1 - e^{\frac{-qV_{DS}}{kT}})$$

III. Circuit Techniques To Reduce Power Dissipation

There are various techniques to reduce power dissipation in a circuit. Some of them are: Body Biasing, Source Biasing, Voltage Scaling, Sleep Transistor and Transistor Stacking Technique. In this section we will discuss transistor stacking technique in detail.

A. Transistor Stacking Technique

Sub-threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the "stacking effect" or "self-reverse bias". Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four terminals of transistors. V_G is "0" thus increasing V_S of NMOS transistor reduces sub-threshold leakage current exponentially.

Let us consider a stack of two NMOS transistors as shown in the Fig.1.

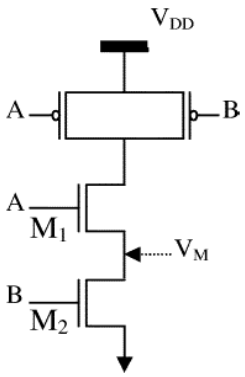

Fig.1. Effect of transistor stacking on source voltage.

When both transistors M1 and M2 are turned off, the voltage at the intermediate node (V_M) is positive due to small drain current. Positive potential at the intermediate node has the three following effects:

1) Due to the positive source potential V_M, gate to source voltage (V_{GS1}) of transistor M1 becomes negative; hence, the sub-threshold current reduces substantially.
2) Due to $V_M > 0$, body to source potential (V_{BS1}) of transistor M1 becomes negative, which results in an increase in the threshold voltage (larger body effect) of M1, and thus reducing the sub-threshold leakage.
3) Due to $V_M > 0$, the drain to source potential (V_{DS1}) of transistor M1 decreases, which results in an increase in the threshold voltage (less DIBL) of M1, and thus reducing the sub-threshold leakage.

If only one NMOS device is off, the voltage at the source node of off transistor would be virtually zero because all other on transistors will act as short circuit. Thus, there is no self reverse biasing effect, and the leakage across the off transistor is large. But if more than one transistor is off, the source voltages of the off transistor, except the one connected to ground by transistors, will be greater than zero, and the leakage will be determined by the most negatively self-reverse biased transistor (because sub-threshold leakage is an exponential function of gate-source voltage). The reverse bias makes the leakage across the off transistor very small.

B. Input Vector Dependence

Functional blocks such as NAND, NOR or other complex gates have a stack of transistors. Due to the stacking effect, the sub-threshold leakage through a logic gate depends on the applied input vector. By applying proper input vectors in a stack we can increase the number of off transistors and can reduce the standby leakage of a functional block.

IV. Proposed Work

Here, we have simulated basic logic gates like inverter, NAND and NOR gate using transistor stacking techniques. By varying the combination of input vectors of the NAND gate and NOR gate the delay and power dissipation have been calculated. All the analysis are done by considering the threshold voltage $V_{TO} = 0.39V$ and by using 130nm technology.

A. NAND Gate

When all the inputs are low (all NMOS transistors are OFF) the power dissipation is minimum and when all the inputs are high (all NMOS transistors are ON) the power dissipation is maximum. As we can see from the Table I and Table II, if the number of low input increases, the power dissipation decreases because the sub threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off.

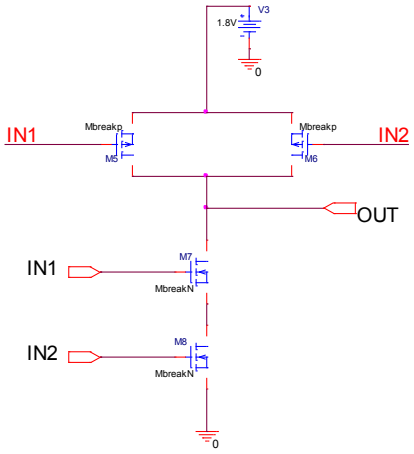

Fig.2 2 – Input NAND gate.

Table I. Estimated power dissipation and delay by varying input vector combination of 2-input NAND gate.

A	B	NAND Output	Power Dissipation (W)	Delay (ps)
0	0	1	$1.10x10^{-9}$	52.64
0	1	1	$2.27x10^{-9}$	45.38
1	0	1	$2.24x10^{-9}$	40.97
1	1	0	$3.38x10^{-9}$	50.25

Table II. Estimated power dissipation and delay by varying input vector combination of 3-input NAND gate.

A	B	C	NAND Output	Power Dissipation (W)	Delay (ps)
0	0	0	1	$7.56x10^{-10}$	10.93
0	0	1	1	$1.10\ x10^{-9}$	14.95
0	1	0	1	$1.10x10^{-9}$	9.95
0	1	1	1	$2.27\ x10^{-9}$	29.97
1	0	0	1	$1.10x10^{-9}$	4.97
1	0	1	1	$2.24\ x10^{-9}$	14.95
1	1	0	1	$2.23\ x10^{-9}$	9.97
1	1	1	0	$5.07\ x10^{-9}$	0.045

B. NOR Gate

When all the inputs are low (all NMOS transistors are OFF) the power dissipation is minimum and when all the inputs are high (all NMOS transistors are ON) the power dissipation is maximum. As we can see from the Table III and Table IV, if the number of high input increases then power dissipation decreases.

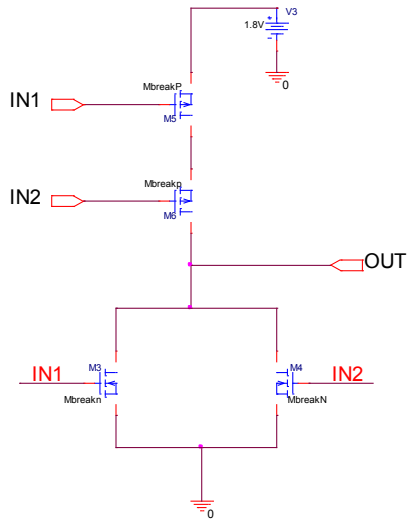

Fig.3. 2 – Input NOR gate.

Table III. Estimated power dissipation and delay by varying input vector combination of 2-input NOR gate.

A	B	NOR Output	Power Dissipation(W)	Delay (ps)
0	0	1	$4.54x10^{-9}$	47.96
0	1	0	$1.69x10^{-9}$	44.76
1	0	0	$1.67x10^{-9}$	48.87
1	1	0	$8.22x10^{-10}$	46.21

Table IV. Estimated power dissipation and delay by varying input vector combination of 3-input NOR gate.

A	B	C	NOR Output	Power dissipation (W)	Delay (ps)
0	0	0	1	$6.8x10^{-9}$	58.87
0	0	1	0	$1.69\ x10^{-9}$	50.29
0	1	0	0	$1.67x10^{-9}$	50.67
0	1	1	0	$8.22\ x10^{-10}$	54.2
1	0	0	0	$1.66x10^{-9}$	52.40
1	0	1	0	$8.22\ x10^{-10}$	43.42
1	1	0	0	$8.21\ x10^{-10}$	44.48
1	1	1	0	$5.66\ x10^{-10}$	48.28

C. 2-to-4 Decoders

We have also applied transistor stacking technique in the estimation of delay and power dissipation of static CMOS based decoders. The analysis is done on both the 2 – to – 4 decoders designed using static CMOS based NAND and NOR gates by considering supply voltage V_{DD} = 1.8V, threshold voltage V_{TO} = 0.39V and by using 130nm technology. The simulation is done with PSPICE. From the calculations depicted in the Table V and Table VI, it can be concluded that as the input goes high, the power dissipation decreases. In case of NAND based decoder the delay also decreases as the input goes high whereas in the case of NOR based decoder the delay increases as the input vector is high.

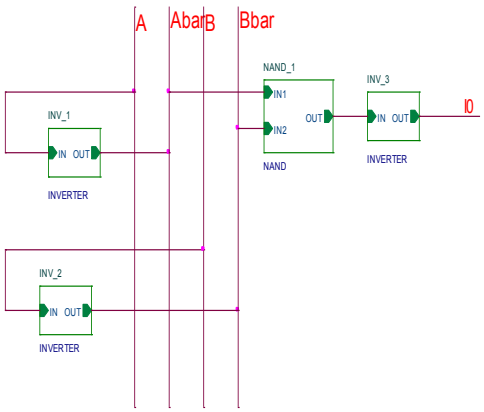

Fig. 4. 2-to-4 Decoder designed using static CMOS based NAND gates

Table V. Estimated delay and power dissipation by varying input vector combination of static CMOS NAND based 2-to-4 decoder.

A	B	OUTPUT				Delay (ps)	Power Dissipation (W)
		I0	I1	I2	I3		
0	0	1	0	0	0	31.08	2.37E-09
0	1	0	1	0	0	28.87	2.31E-09
1	0	0	0	1	0	27.42	2.31E-09
1	1	0	0	0	1	27.13	2.26E-09

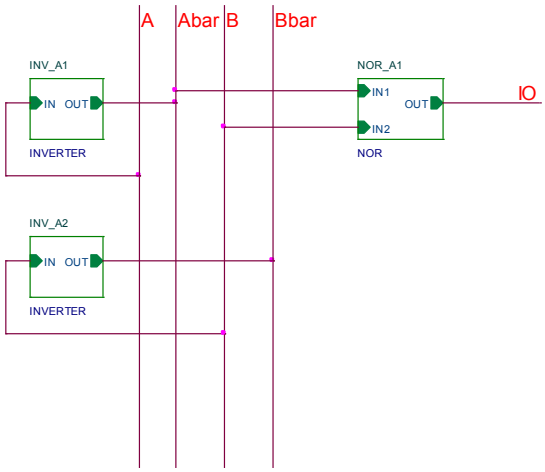

Fig. 5. 2-to-4 Decoder designed using static CMOS based NOR gates

Table VI. Estimated delay and power dissipation by varying input vector combination of static CMOS NOR based 2-to-4 decoder.

A	B	OUTPUT				Delay (ps)	Power Dissipation (W)
		I0	I1	I2	I3		
0	0	1	0	0	0	48.35	1.98E-09
0	1	0	1	0	0	50.65	1.92E-09
1	0	0	0	1	0	46.72	1.92E-09
1	1	0	0	0	1	55.27	1.87E-09

V. Conclusion

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. We have applied transistor stacking technique to the NAND gate, NOR gate and 2-to-4 decoders and estimated their delay and power dissipation. From all the simulation and calculations we have come to a conclusion that by varying the input vector combination we can reduce the power dissipation. There is a tradeoff between power and delay. So, to optimize the circuit we need to have minimum delay and power dissipation without degrading the performance.

References

[1]. Sylvester, Dennis and Srivatava, Ashish "Computer Aided design for Low- Power Robust Computing in Nanoscale CMOS", Proceedings of the IEEE, Vol. 95, No. 3, pp 507-529, March 2007.
[2]. Kuroda, Tadahiro "Optimization and Control of VDD & VTH for Low Power, High Speed CMOS Design", 2002, department of electrical engineering, Keio University.
[3]. Kuroda, Tadahiro "Variable Supply Voltage Scheme for Low Power High Speed CMOS Digital Design", IEEE Journal Solid States Circuit, Vol. 33-No. 3, pp. 454-462, March 1998.
[4]. Deepak Subramanyan, B.S & Adrian Nunez "Analysis of Sub Threshold Leakage Reduction in CMOS Digital Cirtuits", Proceedings of the 13th NASA VLSI Symposium, June 2007, IDAHO, USA.
[5]. Sreenivasa Rao Ijjada, B. Ramparamesh, "Reduction of Power Dissipation in Logic Circuits", International Journal of Computer Applications, Vol. 29-No. 6, June 2011.
[6]. Roy, K. & Mukhopadhaya Saibal "Leakage Current Mechanism and Leakage Reduction Techniques in Deep-Sub Micrometer CMOS Circuit", Proceedings of IEEE, Vol. 91-No. 2, pp.305-327, Feb 2003.
[7]. Mi-Chang, Chang "Transistor and Circuit Design Optimization for Low Power CMOS", IEEE Transactions on Electronic Devices, Vol. 55-No. 1, Jan 2008.
[8]. Bharadwaj, S. A. and Mark, A. H. "Fast Low-Power Decoders for RAMs", IEEE Journal of Solid State Circuits, Vol. 36, No. 10, October 2001.
[9]. Chandrakasan, A. P., Sheng, S. and Broderson, R. W. "Low-Power CMOS Digital Design", IEEE Journal of Solid State Circuits, Vol. 27, No. 4, April 1992.
[10]. S S. M. Kang and Y. Leblebici (2003), "CMOS Digital Integrated Circuits and its Analysis and Design", Third Edition, McGraw-Hill, New Delhi.
[11]. Jan M. Rabey, Anantha Chandrakasan and Borivojc Nikolic, "Digital Integrated Circuits – A Design perspective, Second edition", PHI publication.
[12]. Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design – A circuit and systems perspective, Third edition", Pearson education, South Asia.