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Implementing Logic Functions Using Independently-Controlled Gate in Double-Gate Tunnel FETs: Investigation and Analysis

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ABSTRACT Recently, a compact realization of logic gates using double-gate tunnel field effect transistors (DGTFETs) with independently-controlled gate has been proposed. The key elements in the proposed implementation are the suppression of the tunneling at the surface using gate-source overlap and enable tunneling inside the TFET body by choosing appropriate silicon body thickness. Though these implementations are compact, our study reveals that there are a few critical problems: high average subthreshold swing (SS_{avg}), low ON-state current (I_{ON}) and large propagation delay (t_{pd}). In this paper, we examine the root cause of these problems and explore solutions to tackle them. It is demonstrated that the techniques that boost the I_{ON} in a TFET do not necessarily increase the I_{ON}/I_{OFF} ratio in the proposed implementations. The efficacy of these techniques in improving the I_{ON}/I_{OFF} ratio depends on whether the gate-source overlap is able to suppress the tunneling at the surface and restrict the OFF-state current (I_{OFF}). Furthermore, it is demonstrated that, for the AND functionality, compared to a purely silicon-based DGTFET (Si-TFET) employing silicon-germanium heterojunction DGTFET (HJ-TFET) results in an increase in the I_{ON} by 143×, an increase in the I_{ON}/I_{OFF} ratio by two orders of magnitude and an improvement in the SS_{avg} by 45%, at $V_{DD} = 0.6\ V$. Moreover, a compact NAND gate realized using the proposed HJ-TFETs exhibits two orders of magnitude lower t_{pd}, compared to the NAND gate realized using Si-TFET.

INDEX TERMS Heterojunction, logic function, ON-state current, subthreshold swing, tunnel FET.

I. INTRODUCTION

Tunnel field-effect transistor (TFET) has emerged as a possible alternative to the well-established metal-oxide field-effect transistor (MOSFET). A TFET is able to deliver a subthreshold swing lower than 60 mV/dec at room temperature in contrast to a MOSFET [1]–[5]. Therefore, a TFET seems to be a good candidate to be employed in low-voltage and energy-efficient circuits [6]–[10].

In past, different digital circuits such as logic gates, memories, arithmetic circuits such as adders etc. have been realized using TFETs demonstrating interesting characteristics [11]–[13]. Recently, a single double-gate TFET (DGTFET) with independently-controlled gate terminals has been proposed to realize different logic functions in [14]. The key elements in the proposed implementation of the AND logic are as follows:

1) Biasing the two gates of a DGTFET independently in contrast to a conventional DGTFET where both the gates are tied together.
2) Employing a gate-source overlap in the device to suppress the tunneling at the surface. This reduces the current when only one of the gate terminals is biased to logic "1". Thus, a low OFF-state current (I_{OFF}) is obtained when the gate terminals are at logic "00", "01" and "10".
3) The tunneling inside the silicon body is enabled by choosing appropriate silicon body thickness (t_{si}). This results in a high ON-state current (I_{ON}) when the gate terminals are at logic "11".

Further, a compact realization of two input logic gates such as two-input AND, OR, NAND, NOR logic gates can be

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obtained using only two DGTFETs that realizes complimentary logic functions. In contrast, conventional CMOS-based AND/NAND gate implementations require six/four transistors. Therefore, the DGTFET-based realizations are compact, offers lower load capacitance and reduced number of stages, which eventually can lead to a reduction in the delay of a TFET-based circuit [14]. Considering the promising characteristics of the implementations in [14], we carry out a detailed investigation of the proposed technique in this paper. Our study reveals that the proposed implementation suffers from degraded average subthreshold swing (SS_{avg}) and lower I_{ON}. Therefore, we assess the efficacy of some of the techniques such as use of high-k dielectric, using a Si/Ge heterojunction and using strained material systems in improving the electrical characteristics of a DGTFET that realizes logic functions [10]. It is found that some of these techniques result in a degraded I_{ON}/I_{OFF} ratio despite increased I_{ON}. Further, using 2-D simulations, we demonstrate that a silicon-germanium heterojunction DGTFET (HJ-TFET) based logic circuit implementation can achieve a lower SS_{avg}, a higher I_{ON} and a higher I_{ON}/I_{OFF} ratio compared to a purely Si-based implementation.

It is worth mentioning that in this work, we have analyzed AND logic function in detail since realizing AND function is more difficult compared to other logic functions such as OR and NAND. Moreover, the observations of NOR logic function is similar to the AND logic function. Therefore, we have not described the NOR logic function in this paper.

The rest of the paper is organized as follows: Section II describes the device structure, simulation model and the basic terminology used in this paper. In section III, the electrical characteristics of AND logic function are investigated and the challenges faced in obtaining a high I_{ON}/I_{OFF} ratio in different types of DGTFETs are examined. Section IV demonstrates the implementation of AND logic function using HJ-TFET and compares the characteristics of the NAND gate realized using HJ-TFETs with the NAND gate proposed in [14].

II. DEVICE STRUCTURE, SIMULATION MODEL AND BASIC TERMINOLOGY

Fig. 1 shows the cross-sectional view of a silicon-based DGTFET (Si-TFET) that realizes AND logic function, as proposed in [14]. The important device parameters are: supply voltage (V_{DD}) = 1.2 V, channel length (L_C) = 100 nm, gate-source overlap (L_{ov}) = 20 nm, source doping (p-type) (N_S) = 1×10^{20} $atoms/cm^3$, drain doping (n-type) (N_D) = 1×10^{18} $atoms/cm^3$ and channel doping (p-type) (N_C) = 1×10^{17} $atoms/cm^3$.

In this paper, simulations are carried out using 2-D device simulator Atlas version 5.22.1.R [15]. Non-local band-to-band tunneling (BTBT) model has been used. This model takes into account the spatial profile of the energy bands for the computation of the tunneling current in TFETs. Other important models that are invoked in our simulation are Shockley-Read-Hall recombination, bandgap narrowing and

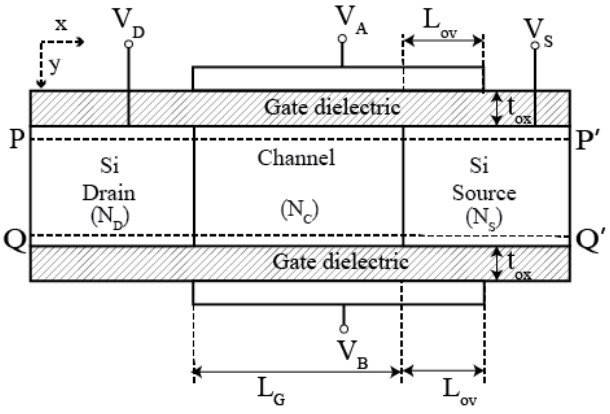

FIGURE 1. Cross-sectional view of Si-TFET that realizes AND logic function [14].

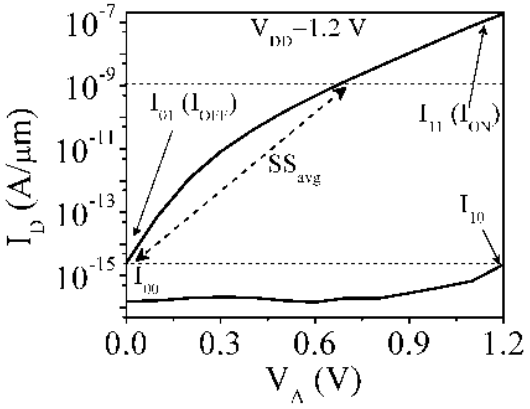

FIGURE 2. Transfer characteristics of the Si-TFET that realizes AND logic function at V_{DD} = 1.2 V [14].

Fermi-Dirac statistics. The simulation model is calibrated using [16] and the same simulation setup has been used in previous works [14], [17]–[20]. Quantum confinement effects (QC) have not been considered in this work. Though, it is known that QC effects can impact the electrical characteristics of a TFET, it has been reported in [14] that the QC effects have no adverse impact on the performance of the logic realizations using DGTFETs. Therefore, to keep the simulation model simple, we have not considered the QC effects in this paper.

In this work, V_{DD} and Gnd represent logic "1" and logic "0", respectively. V_A and V_B represent the input voltages applied to the top gate and the bottom gate of the device, respectively, as shown in Fig. 1. The input to the device, when the top gate is biased at logic A and the bottom gate is biased at logic B is denoted as "AB" and the corresponding drain current (I_D) is denoted as I_{AB}. For example, when V_A = 0 (logic "0") and V_B = V_{DD} (logic "1"), then the input is denoted as "01" and the corresponding drain current is denoted as I_{01}.

Fig. 2 shows the transfer characteristics of the AND logic function realized using Si-TFET [14]. In Fig. 2, I_{11} represents

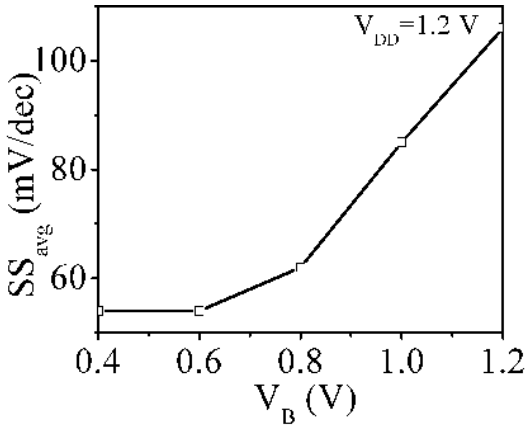

FIGURE 3. Variation of SS_{avg} with respect to V_B. The SS_{avg} is extracted from the transfer characteristics of I_D vs. V_A.

the ON-state current and is reported to be $10^{-7}A/\mu m$. The OFF-state current=$MAX(I_{00}, I_{01}\ and\ I_{10})$ is reported to be $10^{-15}A/\mu m$. The SS_{avg} is calculated as the inverse slope extracted from the transfer characteristics from $V_A = 0$ to the point at which $I_D = 10^{-9}A/\mu m$ and is extracted to be $106\ mV/dec$ for the AND-gate realized using Si-TFET [14].

III. ELECTRICAL CHARACTERISTICS OF AND LOGIC IMPLEMENTATION

A. AVERAGE SUBTHRESHOLD SWING (SS_{AVG})

SS_{avg} is an important parameter for digital applications since lower SS_{avg} allows low voltage and energy-efficient operations [6], [10]. For Si-TFET-based AND logic realization as shown in Fig. 2, the $SS_{avg} = 106\ mV/dec$. On the other hand, when both the gate terminals are tied together such that $V_A = V_B$, the average subthreshold swing is found to be $SS_{avg} = 37\ mV/dec$. Therefore, the degraded SS_{avg} in the AND logic realization can be attributed to the independently-controlled gate.

To study the effect of independently-controlled gate, SS_{avg} is extracted from the transfer characteristics (I_D vs. V_A) at different V_B, as shown in Fig. 3. It can be inferred from Fig. 3 that as V_B increases, the SS_{avg} increases. The degradation of SS_{avg} with increase in V_B can be explained by examining the device under different bias-conditions, as explained below.

Fig. 4(a) and 4(b) show the tunneling rate in the body of DGTFET at two different V_B (0.6 V and 1.2 V). In these figures, appropriate V_A is chosen such that the drain current just starts to take off in the transfer characteristics. The drain current starts to take off in the transfer characteristics when the BTBT gets initiated due to alignment of the valence band and the conduction band. It is worth pointing out that at different V_B, BTBT gets initiated at different V_A. For instance, when $V_B = 0.6\ V$ BTBT gets initiated at $V_A = 0.9\ V$ and when $V_B = 1.2\ V$ BTBT gets initiated at $V_A = 0.2\ V$. Therefore, in the Fig. 4(a) and 4(b) different V_A are chosen to determine the regions where BTBT initiates. From Fig. 4(a) it is evident that BTBT is initiated in the upper half of the device

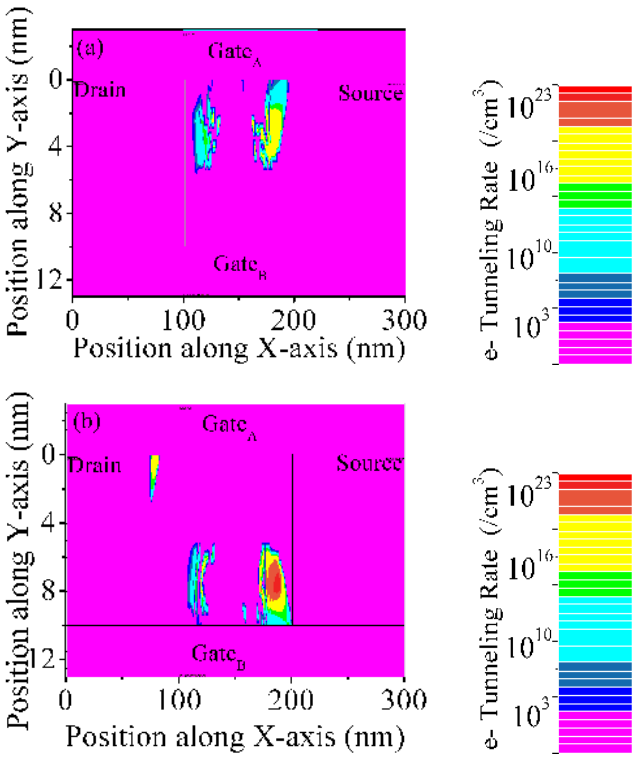

FIGURE 4. Tunneling rate in the TFET at $V_{DS} = V_{DD}$ (a) For $V_A = 0.9\ V$ and $V_B = 0.6\ V$ (b) For $V_A = 0.2\ V$ and $V_B = 1.2\ V$.

when $V_B = 0.6\ V$. It illustrates that when $V_B << V_{DD}$, the control of the top gate is dominant. However, when $V_B \approx 1.2\ V$, BTBT initiates in the lower half of the device as shown in Fig. 4(b), illustrating the dominant control of the bottom gate at higher V_B. In Fig. 4(b) it can be observed that there is a small BTBT occurring in the drain side closer to the top-gate. However, it is worth pointing out that the contribution of the above mentioned BTBT on the drain current is negligible.

Fig. 5(a) and 5(b) compare the band diagrams of the device for $V_B = 0.6\ V$ (across the cutline PP') and $V_B = 1.2\ V$ (across the cutline QQ'), keeping the same $\Delta V_A = 0.2\ V$. We take ΔV_A as the increase in the voltage V_A above the bias point at which the BTBT initiates. Different cutlines are chosen since BTBT initiates in different regions at different bias conditions, as explained above. The band diagrams show that, for the same ΔV_A, the increase in the band alignment is more when $V_B = 0.6\ V$ compared to when $V_B = 1.2\ V$. This results in a change in the drain current ($\Delta(log\ I_D)$) by two decades and four decades, respectively, for $V_B = 1.2\ V$ and $V_B = 0.6\ V$ (for the same $\Delta V_A = 0.2\ V$). Since $SS_{avg} = \Delta V_A/\Delta(log\ I_D)$, and $\Delta(log\ I_D)$ is higher for $V_B = 0.6\ V$, a smaller SS_{avg} is exhibited at $V_B = 0.6\ V$ compared to $V_B = 1.2\ V$. Further, our simulations show that the architectural modifications such as gate-source overlap do not contribute to the degradation in the SS_{avg} of the DGTFET. Using 2-D simulations, the SS_{avg} for the conventional TFET with and without gate-source overlap was extracted and found to be same. Therefore, the degradation in the SS_{avg} can solely be

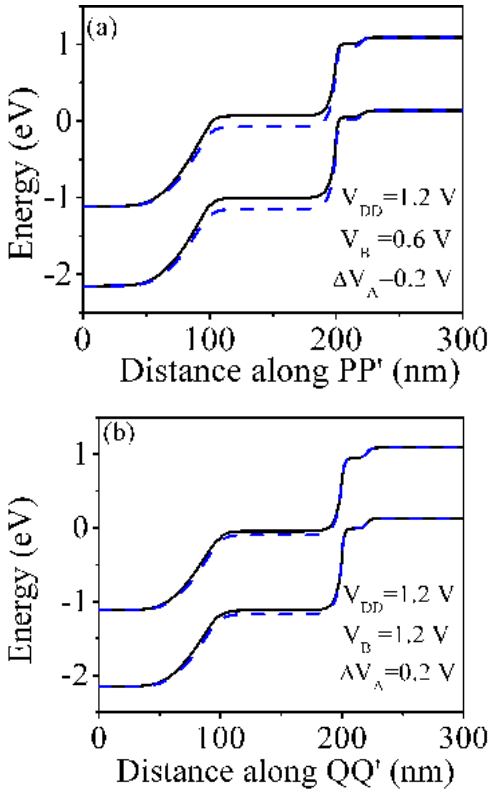

FIGURE 5. Band diagram at $V_{DS} = V_{DD}$. (a) For $\Delta V_A = 0.2$ V and $V_B = 0.6$ V, the extracted band overlap $B_{ov} = 0.15$ eV. (b) For $\Delta V_A = 0.2$V and $V_B = 1.2$ V, the extracted band overlap is $B_{ov} = 0.05$ eV.

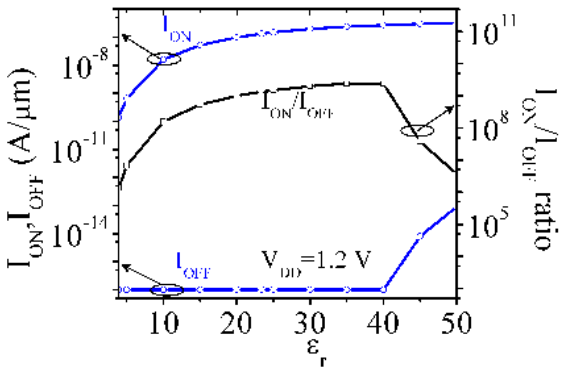

FIGURE 6. Variation of I_{ON}, I_{OFF} and I_{ON}/I_{OFF} with respect to ϵ_r.

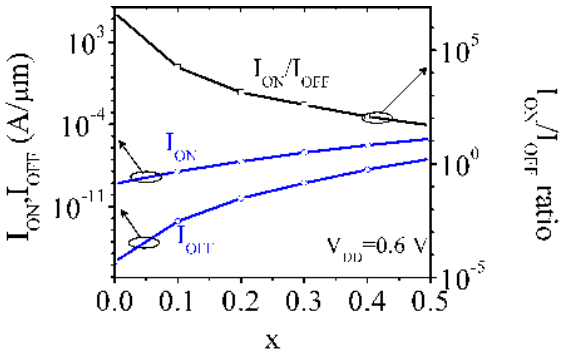

FIGURE 7. Variation of I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio at different germanium mole fractions (x) in sS-DGTFET.

attributed to the independently-controlled gate and is prominent when the voltage at one of the terminals is fixed at a value close to the supply voltage.

B. ON-STATE CURRENT TO OFF-STATE CURRENT RATIO

It is desirable to have a higher I_{ON}, lower I_{OFF} and higher I_{ON}/I_{OFF} ratio for digital circuits. A higher I_{ON} leads to lower delays and a lower I_{OFF} reduces the static power consumption. Our simulations show that, in general, the gate-source overlap employed to suppress the I_{OFF} adversely affects the I_{ON} in the DGTFETs. For example, it is found that the I_{ON} obtained with gate-source overlap is 40% lower as compared to the I_{ON} obtained without gate-source overlap in a DGTFET when both the gate terminals are tied together. Therefore, techniques that can boost the I_{ON} in a TFET are critical in the proposed logic realizations. However, boosting I_{ON} in a TFET that realizes a logic function is challenging, since the techniques that boost the I_{ON} can adversely impact the functionality itself (by delivering a lower I_{ON}/I_{OFF} ratio). It is important to note that the proposed implementation of AND logic works well only when the gate-source overlap is able to turn-OFF the device when the inputs are "10" and "01".

1) GATE DIELECTRIC

When the dielectric constant (ϵ_r) of the gate insulator in a TFET is increased, the tunneling current increases [10], [16]. However, the application of high-k dielectric in a TFET that realizes AND logic function is complicated. Fig. 6 shows the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio at different ϵ_r. As ϵ_r increases, for a fixed oxide thickness (t_{ox}), the control of the gate becomes more prominent resulting in a sharper band-bending and increased I_{ON}. However, as the dielectric constant increases beyond a certain limit ($\epsilon_r > 40$), it becomes difficult to suppress the BTBT at the surface of the device using gate-source overlap. As a result, with the increase in ϵ_r, the I_{OFF} starts increasing rapidly when $\epsilon_r > 40$. Therefore, a lower I_{ON}/I_{OFF} ratio is obtained for a high value of ϵ_r.

2) STRAINED SILICON DGTFET

Strain has been exploited in TFETs to achieve a higher I_{ON} [14], [20]–[23]. In this section, the applicability of a strained silicon DGTFET (sS-DGTFET) in realizing AND logic has been analyzed. An sS-DGTFET is composed of strained silicon body rather than normal silicon. In strained silicon, the amount of strain is controlled by varying the Ge mole fraction (x) in the SiGe buffer layer that is used during its fabrication. The introduction of strain in silicon results in a decrease in the bandgap and the effective mass of carriers and an increase in the electron affinity and can be modelled as in previous works [19], [20].

Fig. 7 shows the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio at different Ge mole fraction (x) in sS-DGTFET. It can be seen that

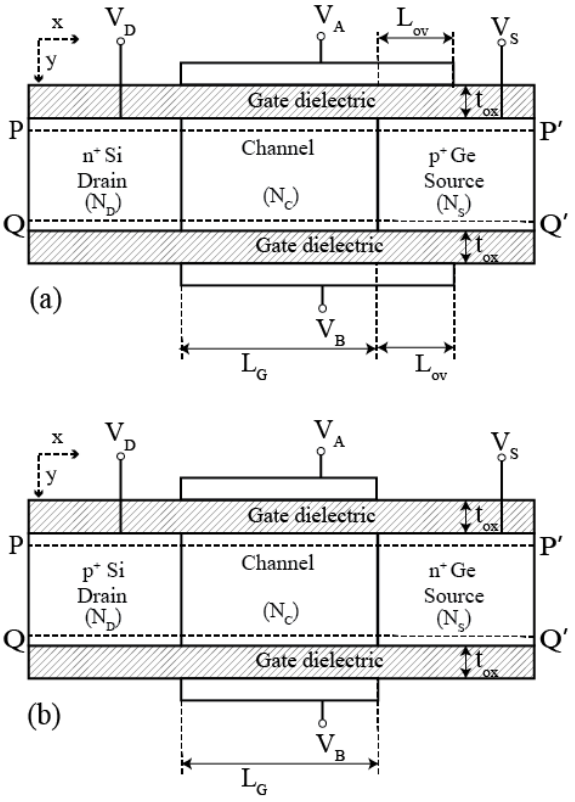

FIGURE 8. Cross-sectional view of an HJ-TFET that realizes (a) AND (b) NAND logic function.

although I_{ON} increases with increasing x, I_{OFF} also increases leading to a degraded I_{ON}/I_{OFF} ratio at higher Ge mole fractions. The I_{OFF} increases at higher Ge mole fraction because the device cannot be effectively turned-OFF as explained in the following section.

In the next section, heterojunction TFET (HJ-TFET) that employs germanium source is proposed for realizing a high performance AND logic.

IV. AND AND NAND LOGIC FUNCTION USING SI/GE HETEROJUNCTION DGTFET

Silicon-Germanium heterojunction TFET with germanium as the source material has been proposed and widely studied in literature [24]–[27]. Using a Si-Ge heterojunction helps in obtaining a higher I_{ON}/I_{OFF} ratio due to smaller effective bandgap [25]. Therefore, in this section, we have investigated the application of silicon-germanium heterojunction TFET (HJ-TFET) for realizing AND and NAND logic functions. The HJ-TFET realizing AND and NAND logic function are shown in Fig. 8(a) and 8(b), respectively. For HJ-TFET based logic implementation, a small body thickness (t_{si}) is desirable [14]. Therefore, $t_{si} = 10\ nm$ is taken. The tunneling parameters of germanium used in this work are calibrated using Fig. 4 of ref. [28]. The other simulation models and parameters used in the simulations are as described in section-II. The relevant device parameters used for Si-TFET and HJ-TFET are listed in Table-I. For simplicity, we have not included trap-assisted tunneling in our simulations. However, it should be noted that trap-assisted tunneling can increase SS_{avg} or I_{OFF} [29], [30]. It is important to point out that the focus of this work is to demonstrate the relative improvement in electrical characteristics of the AND logic realized using an HJ-TFET compared to an Si-TFET, rather than reporting the exact current values in these devices. It is also important to highlight that, in general, heterostructures suffer from interface states and scattering, and techniques to obtain defect-free interfaces are important [24], [31]–[33].

TABLE 1. Device parameters used in simulation.

Parameter	Value
Supply voltage (V_{DD})	0.6 V
Gate work function (ϕ_m)	4.65 eV
Silicon film thickness (t_{si})	10 nm
Gate dielectric constant (ϵ_r)	23.4
Gate oxide thickness (t_{ox})	3 nm (Effective Oxide Thickness EOT= 0.5 nm)
Channel length (L_C)	30 nm
Gate-Source Overlap (L_{ov})	20 nm
Drain doping (N_D) (n-type)	$1 \times 10^{18} atoms/cm^3$
Channel doping (N_C)	$1 \times 10^{17} atoms/cm^3$
Source doping (N_S) (p-type)	1×10^{20} $atoms/cm^3$ (Si-TFET) 4×10^{19} $atoms/cm^3$ (HJ-TFET)

Fig. 9(a) compares the transfer characteristics of AND logic function realized using Si-TFET and HJ-TFET at $V_{DD} = 0.6\ V$. It can be inferred from Fig. 9a that the I_{ON} improves from $8.4 \times 10^{-10} A/\mu m$ in Si-TFET to $1.2 \times 10^{-7} A/\mu m$ in HJ-TFET. The I_{ON}/I_{OFF} improves from $\sim 10^7$ in Si-TFET to $\sim 10^9$ in HJ-TFET. The SS_{avg} improves from $86\ mV/dec$ in Si-TFET to $48\ mV/dec$ in HJ-TFET, at $V_{DD} = 0.6\ V$. Similarly, the I_{ON} improves from $9.7 \times 10^{-10} A/\mu m$ in Si-TFET based NAND function to $1.8 \times 10^{-7} A/\mu m$ in HJ-TFET based NAND function, as shown in Fig. 9(b).

Next, we investigate why an sS-DGTFET-based AND logic implementation is unable to deliver a high I_{ON}/I_{OFF} ratio in contrast to the HJ-TFET-based AND logic implementation. The band diagrams for the sS-DGTFET and the HJ-TFET for different values of gate-source overlap (L_{ov}) in the OFF-state ($V_{DS} = V_B = V_{DD}$ and $V_A = 0\ V$) are shown in Fig. 10(a) and Fig. 10(b), respectively. It can be seen that in the both cases, the tunneling width increases as the L_{ov} increases. However, the initial band overlap is comparatively high in sS-DGTFET compared to HJ-TFET. In a TFET, tunneling width as well as band overlap between the valence band of the source and conduction band of the channel, are important factors in deciding the tunneling current [10]. Since, the gate-source overlap is unable to decrease the band overlap sufficiently in an sS-DGTFET, the I_{OFF}

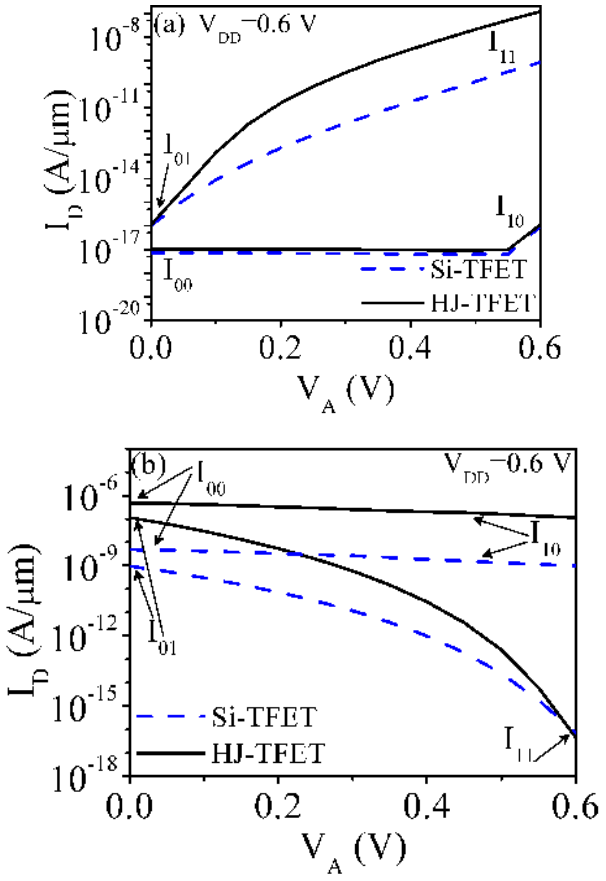

FIGURE 9. Comparison of transfer characteristics of Si-TFET and HJ-TFET-based (a) AND (b) NAND logic at $V_{DD} = 0.6\ V$ and $L_G = 30\ nm$.

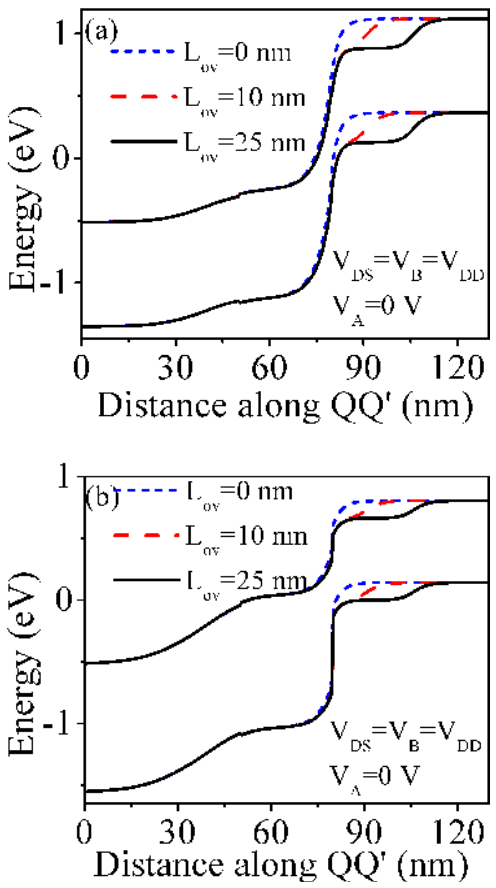

FIGURE 10. Band diagram at $V_A = 0\ V$ and $V_{DS} = V_B = V_{DD}$ for different L_{ov} (a) sS-DGTFET (b) HJ-TFET.

cannot be suppressed beyond a certain limit in its AND logic implementation. This demonstrates that the proposed technique of realizing AND logic requires greater attention in TFETs with high band overlaps.

A. VOLTAGE SCALABILITY ANALYSIS OF HJ-TFET-BASED AND LOGIC IMPLEMENTATION

Considering future applications, it becomes important to analyze the behaviour of the realized AND logic function for $V_{DD} < 0.6\ V$. To compare the voltage scalability of the Si-TFET and the HJ-TFET-based AND logic implementation, the I_{ON}/I_{OFF} ratio vs. V_{DD} is plotted in Fig. 11. It is found that in the HJ-TFET-based AND logic implementation the I_{ON}/I_{OFF} ratio is 9×10^6 at $V_{DD} = 0.3\ V$, while in the Si-TFET-based AND logic implementation the I_{ON}/I_{OFF} ratio drops to 7×10^4.

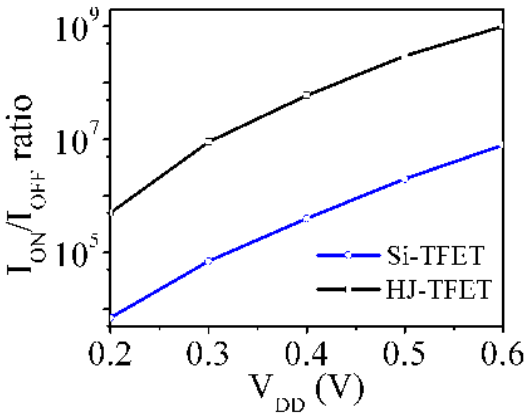

FIGURE 11. I_{ON}/I_{OFF} ratio vs. V_{DD} for Si-TFET and HJ-TFET-based AND logic implementation.

B. IMPLEMENTATION OF A NAND GATE

A 2-input NAND gate can be implemented using a DGTFET that realizes the NAND logic function as the pull-up network and a DGTFET that realizes AND logic function as the pull-down network, as shown in Fig. 12 [14]. Fig. 13(a) shows the input waveform V_A and Fig. 13(b) compares the transient behaviour of the Si-TFET and HJ-TFET-based NAND gates at $V_{DD} = 0.6\ V$. Fig. 14 shows the extracted propagation delay (t_{pd}) for Si-TFET and HJ-TFET-based NAND gates, at different supply voltages. It can be inferred from Fig. 14, that the HJ-TFET-based NAND gate offers two orders of magnitude lower t_{pd} compared to the Si-TFET-based NAND gate. However, t_{pd} is in the range of nano-seconds is still a few orders of magnitude larger than the t_{pd} in MOSFET-based

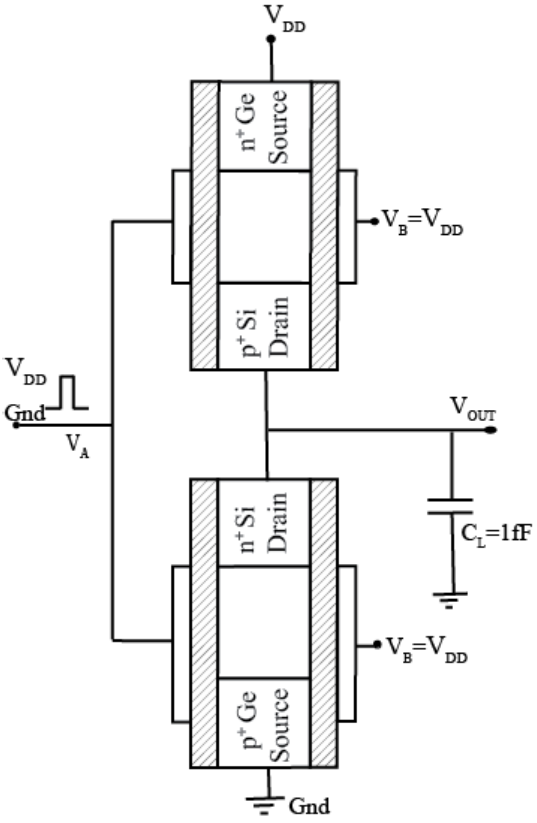

FIGURE 12. Schematic of NAND gate implementation using HJ-TFET.

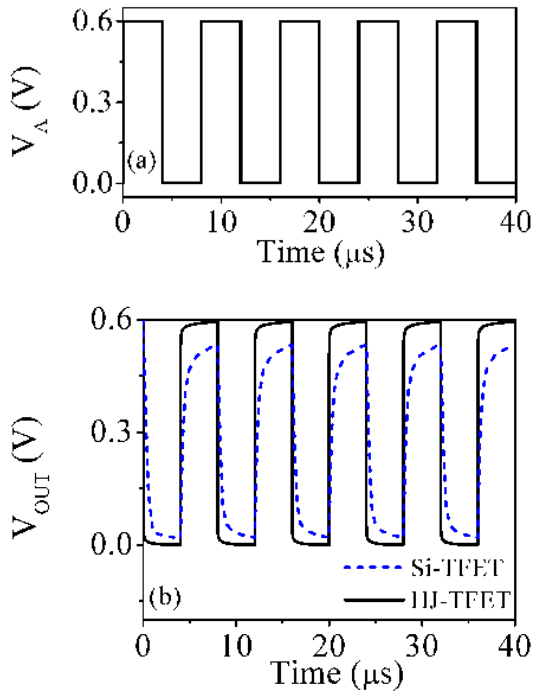

FIGURE 13. Transient response of the NAND gates. (a) Input waveform (V_A) (b) output waveform (V_{OUT}) at $V_B = 0.6\ V$ and $V_{DD} = 0.6\ V$ for Si-TFET and HJ-TFET.

gates which have delays in the range of pico-seconds [34]. The higher delay can be attributed to lower ON-state

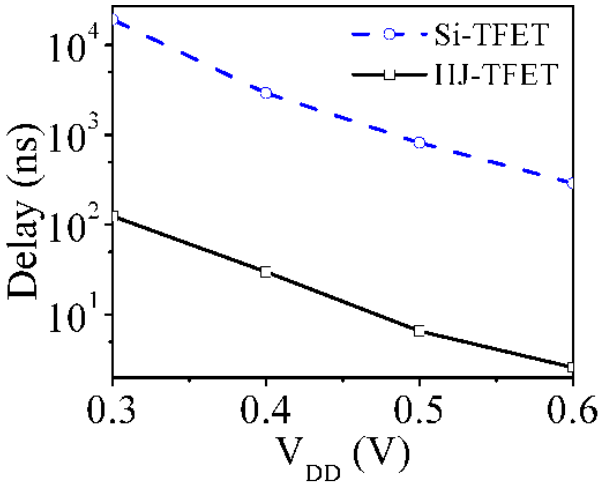

FIGURE 14. Propagation delay vs. V_{DD} for Si-TFET and HJ-TFET-based NAND gate.

current and higher miller capacitance of TFETs compared to MOSFETs [35]. Therefore, to outperform MOSFET-based circuits, there is a need of further increase in the I_{ON} and a reduction in the capacitance.

Further, it is worth mentioning that the gate-source overlap, used in these implementations increases the gate-to-source capacitance (C_{gs}) in the proposed device, however the gate-to-drain capacitance (C_{gd}) remains unaffected [14]. It has been shown that in TFETs, C_{gd} is dominant and determines overall gate capacitance [35]. In the proposed implementations, though the gate-to-source overlap increases the C_{gs}, it is still lower than the C_{gd}. Therefore, the impact of increased C_{gs} do not adversely affect the transient response of the proposed logic implementations. Moreover, it is shown in the literature that the architecture having independent double gate leads to the reduction in the area/capacitance when compared to the conventional single gate transistors used in conventional 4T-NAND gate, by reducing the number of transistors and their stages [34], [36]. Therefore, some of the demerits of TFETs can be offset by the architecture described in this paper that reduces the capacitance compared to the conventional CMOS-based logic gates by reducing the number of transistors and their stages.

It is important to compare the characteristics of the proposed HJ-TFET based NAND gate with the conventional four-transistor (4T) implementation of the NAND gate. Therefore, firstly we compare the pull down networks of both implementations, as shown in Fig. 15. In the conventional 4T-NAND gate, the pull down network consists of two series connected DGTFETs. The current flowing in a single DGTFET (with same device parameters as shown in Table-I) is found to be $3.3 \times 10^{-6} A/\mu m$ when $V_A = V_B = V_{DD}$. However, when two such DGTFETs are connected in series in a NAND gate, the increased tunnel resistance results in a smaller current of $0.8 \times 10^{-7} A/\mu m$ flowing through the pull down network when $V_A = V_B = V_{DD}$. On the other hand,

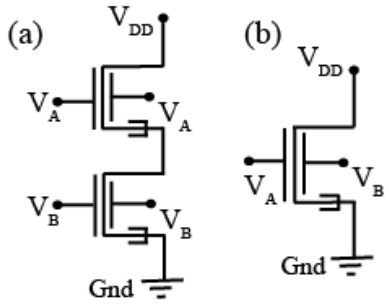

FIGURE 15. Schematic of pull-down network of (a) conventional 4T-NAND implementation (b) proposed HJ-TFET based NAND gate implementation.

in the HJ-TFET based NAND gate implementation, the pull down network consists of a single HJ-TFET performing the AND-function. In this case, a current of $1.1 \times 10^{-7} A/\mu m$ flows in the pull-down network when $V_A = V_B = V_{DD}$. Therefore, the current flowing in the pull-down network in the proposed implementation is similar to the current flowing in the pull-down network of the conventional implementation. A similar observation is made regarding the pull-up network. Therefore, although the proposed implementation consumes less area and requires less number of transistors in implementing logic functions, it is not expected to suffer in performance compared to conventional implementations.

V. CONCLUSION

In this paper, the logic function implementations proposed in [14] have been investigated in detail and the reasons for a degraded SS_{avg} and a low I_{ON} have been examined. It is demonstrated that compared to the implementation proposed in [14], an HJ-TFET-based AND logic implementation exhibits an increase in the I_{ON} by 143×, an increase in the I_{ON}/I_{OFF} ratio by two orders of magnitude and an improvement in the SS_{avg} by 45% at $V_{DD} = 0.6\,V$. Moreover, HJ-TFET-based NAND gate exhibits two orders of magnitude lower t_{pd} at $V_{DD} = 0.6\,V$ compared to the implementation in [14]. It is worthy to mention that HJ-TFET-based logic gates also exhibit compactness, low load capacitance (due to halved transistor count) and reduced number of stages in realizing these gates. However, further improvement in propagation delay is required to match the performance of CMOS-based logic gates and obtain comparable energy-efficiency. Nevertheless, the results presented in this paper could provide further motivation to explore TFETs for future energy-efficient applications.

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