# Imprint lithography for integrated circuit fabrication

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The escalating cost for next generation lithography (NGL) tools is driven in part by the need for complex sources and optics. The cost for a single NGL tool could exceed $50M in the next few years, a prohibitive number for many companies. As a result, several researchers are looking at low cost alternative methods for printing sub-100 nm features. In the mid-1990's, several research groups started investigating different methods for imprinting small features. Many of these methods, although very effective at printing small features across an entire wafer, are limited in their ability to do precise overlay. In 1999, Colburn *et al.* [Proc. SPIE 379 (1999)] discovered that imprinting could be done at low pressures and at room temperatures by using low viscosity UV curable monomers. The technology is typically referred to as step and flash imprint lithography. The use of a quartz template enabled the photocuring process to occur and also opened up the potential for optical alignment of the wafer and template. This article traces the development of nanoimprint lithography and addresses the issues that must be solved if this type of technology is to be applied to high-density silicon integrated circuitry. © *2003 American Vacuum Society.*
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## I. INTRODUCTION

In the fields of micro- and nanolithography, major advancements in resolution have historically been achieved through use of shorter wavelengths of light. Using phase shift mask technology, it has already been demonstrated that 193 nm photolithography can produce sub-100 nm features. Along this path, such improvements come with an ever-increasing cost for photolithographic tools. As conventional projection lithography reaches its limits, Next generation lithography (NGL) tools may provide a means to further pattern shrinks, but are expected to have price tag that is prohibitive for many companies.

The development of both light sources and optics to support the sources are primarily responsible for the rise in the cost of an NGL tool. 157 nm lithography, for example, requires the use of $CaF_2$ as a lens material. In the case of extreme ultraviolet lithography, no source with sufficient output has yet been identified that will meet the industry's throughput requirements.

Imprint lithography is essentially a micromolding process in which the topography of a template defines the patterns created on a substrate. Investigations by this group and others in the sub-50 nm regime indicate that imprint lithography resolution is only limited by the resolution of the template fabrication process. It possesses important advantages over photolithography and other NGL techniques since it does not require expensive projection optics, advanced illumination sources, or specialized resist materials that are central to photolithography and NGL technologies.[1] There are three basic

approaches to imprint lithography. Each technique is depicted in Fig. 1 and is briefly described below.

Soft lithography generally refers to the process of transferring a self-assembled monolayer using a flexible template [see Fig. 1(a)]. Whitesides *et al.*[2] have formed a template by applying a liquid precursor to polydimethylsiloxane over a master mask produced using either electron beam or optical lithography. The liquid is cured, and the particle desorption mass spectrometry (PDMS) solid is peeled away from the original mask. The PDMS template can then be coated with a thiol solution, which is subsequently transferred to a substrate, coated with a thin layer of gold. To prevent adhesion between the master and daughter masks, the master surface is passivated by the gas phase deposition of a long-chain fluorinated alkylchlorosilane [$CF_3(CF_2)_6(CH_2)_2SiCl_3$].

Because the PDMS is easily deformable, the technology is not well suited for devices requiring precise pattern placement. Nanoimprint lithography (NIL), developed by Chou *et al.*[3] uses a solid mold, such as silicon or nickel. The imprint process is accomplished by heating a resist above its glass transition temperature and imparting a relatively large force to transfer the image into the heated resist [see Fig. 1(b)]. Features as small as 10 nm have been imaged using NIL. In addition, a variety of different devices have been fabricated by a number of different researchers using this approach. The elevated temperatures and pressures needed for this approach may limit its use for applications requiring tight overlay, however.

Devices that require several lithography steps and precise overlay will need an imprinting process capable of addressing registration issues. A derivative of NIL, ultraviolet

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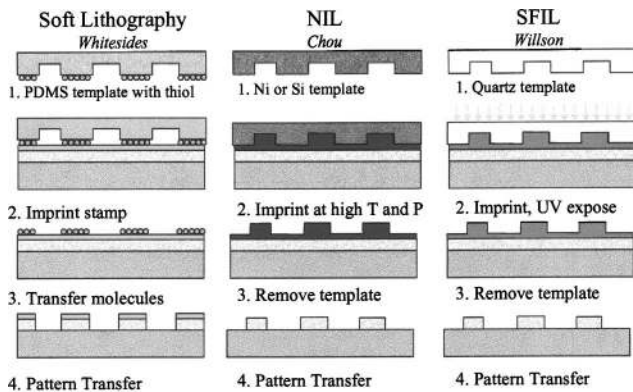
FIG. 1. Fabrication sequence for three different varieties of imprint lithography.
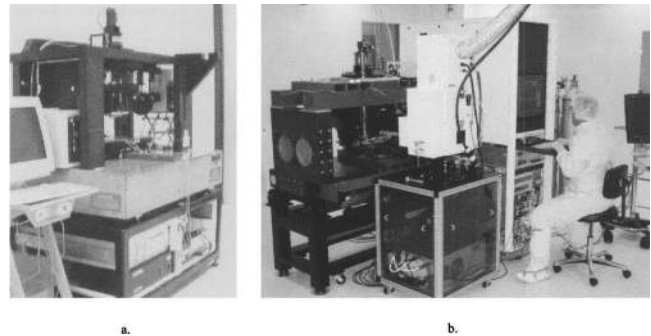


FIG. 2. (a) First step and repeat UV-based nanoimprint tool. (b) The Imprio 100, from Molecular Imprints, Inc. The system is designed to pattern wafers as large as 200 mm in diameter.

nanoimprint lithography (or UV-NIL) addresses the issue of alignment by using a transparent template, thereby facilitating conventional overlay techniques [see Fig. 1(c)]. In addition, the imprint process is performed at low pressures and at room temperature, which minimizes magnification and distortion errors. Two types of approaches are being considered for UV-NIL. The first method uses conventional spin-on techniques to coat a wafer with a UV curable resist.[4] Although it is possible to uniformly coat the wafer, there are concerns that the viscosity of the resist will be too high to facilitate the formation of very thin residual layers. If the residual layer is too thick, the critical dimension (CD) uniformity may suffer as a result of the subsequent pattern transfer process. This problem is addressed by locally dispensing a low viscosity resist in a single stepper field. This second approach was first disclosed by Colburn *et al.*[5] in 1999 and is generally referred to as step and flash imprint lithography, or S-FIL.

S-FIL appears to be the most suitable imprint technique for fulfilling the stringent requirements of silicon integrated circuit (IC) fabrication. The purpose of this article is to summarize the progress made in S-FIL. Because a tool, a template, and a resist are necessary for the fabrication process, each of these subjects is discussed in detail. Following this discussion, open issues, such as defects and overlay, are explored.

## II. STEP AND FLASH IMPRINT LITHOGRAPHY TOOL

Imprint lithography relies on the parallel orientation of imprint template and substrate. Inaccurate orientation may yield a layer of cured etch barrier that is nonuniform across the imprint field. Thus, it is necessary to develop a mechanical system whereby template and substrate are brought into coparallelism during etch barrier exposure. This was originally achieved in S-FIL by way of a two-step orientation scheme. In step one, the template stage and wafer chuck are brought into course parallelism via micrometer actuation. The second step uses a passive flexure-based mechanism that takes over during actual imprint.[6,7]

The step and repeat system was built at the University of Texas in Austin by modifying a 248 nm Ultratech stepper that was donated by IBM [see Fig. 2(a)]. Key system attributes include a microresolution $z$ stage that controls the imprint force, an automated $x-y$ stage for step and repeat positioning, a precalibration stage that enables parallel alignment between the template and substrate, a fine-orientation flexure stage that provides a highly accurate automatic parallel alignment of the template and wafer, an exposure source that is used to cure the etch barrier, and an automated fluid delivery system that accurately dispenses known amounts of the liquid etch barrier.

A commercialized version of an S-FIL tool is now available from Molecular Imprints Inc. (MII). It is interesting to note that although nanoimprint lithography is still in the early stages of development, there are several vendors that are now offering imprint tools. In addition to Molecular Imprints, EVGroup (Austria), Nanonex (U.S.), Obducat (Sweden), and Suss Microtec (Germany) have systems ready for purchase. This is quite different from previous NGL development efforts in which a vendor only becomes interested in building a system after the technology matures to some degree.

Although the Imprio 100 from MII is a substantial improvement relative to the first University tool, it has neither the throughput nor the overlay specifications necessary for silicon IC fabrication. Instead, the system was primarily designed and manufactured to address the compound semiconductor and photonics markets. These markets require high-resolution features but are typically less sensitive to defects. They also operate at low volumes of wafers and are hence more sensitive to costs; particularly tool costs. The tool has a throughput capacity of approximately six 200 mm wafers per hour. As a result, it will be possible to collect enough statistical information of performance characteristics of S-FIL to allow the design of a fully engineered high volume-manufacturing tool in the future.

The Imprio 100 was developed in partnership with several key original equipment manufacturer suppliers for the stage technology, the UV source, and the control architecture. The extremely complicated and costly imaging optics, source, and step and scan mechanical systems associated with other
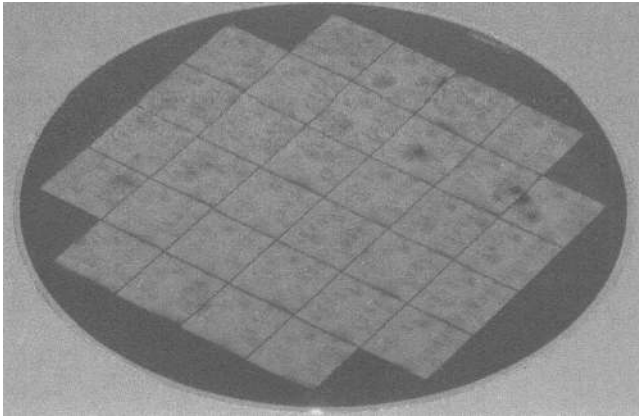
FIG. 3. Residual layer thickness and uniformity in a printed die.

NGL techniques are not required in S-FIL technology. It is essentially a precise mechanical system with specialized fluid mechanics subsystems and a mercury arc lamp as its source. Therefore, it is a much simpler system with significantly smaller footprint, and its cost structure has the potential to be an order of magnitude lower than high-end lithography tools.

Of particular interest is the resist delivery system, which incorporates a microsolenoid nozzle capable of dispensing drops less than 5 nl in volume. This type of control is essential for the control of the residual layer formed during the imprint process. When integrated with a well designed flexure stage and wafer chuck it is possible to print an etch barrier with residual layers well under 100 nm. Figure 3(a) depicts the data for residual layer uniformity in a single die. In this case, a mean thickness of 70 nm was achieved, with a 30 nm $3\sigma$ variation.

## III. STEP AND FLASH IMPRINT LITHOGRAPHY S-FIL TEMPLATE

Early template fabrication schemes started with a 6 in. × 6 in. × 0.25 in. conventional photomask plate and used established Cr and phase shift etch processes to define features in the glass substrate.[8] Although sub-100 nm geometries were demonstrated, CD losses during the etching of the thick Cr layer etch make the fabrication scheme impractical for 1X templates. It is not unusual, for example, to see etch biases as high as 100 nm.[9]

More recently, two methods have been employed to fabricate templates.[10,11] The first method uses a much thinner (15 nm) layer of Cr as a hard mask. Thinner layers still

suppress charging during the electron-beam exposure of the template, and have the advantage that CD losses encountered during the pattern transfer through the Cr are minimized. Because the etch selectivity of glass to Cr is better than 18:1 in a fluorine-based process, a sub-20 nm Cr layer is also sufficient as a hard mask during the etching of the glass substrate. The second fabrication scheme attempts to address some of the weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, scanning electron microscopy (SEM) and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide (ITO) on the glass substrate, charging is suppressed during inspection, and the transparent nature of the final template is not affected. The experimental details of the processes have been covered in previous publications.[11,12]

The Cr-based template pattern transfer process consisted of an exposure in a Leica VB6 and development of the ZEP-520 positive resist, followed by an oxygen descum, Cr etch, resist strip, quartz etch, and a Cr wet etch. It is interesting to note that it was necessary to remove the resist prior to the quartz etch. If left in place during the $CHF_3$-based quartz etch, the amount of polymer deposited during the etch process is substantial enough to impact the fidelity of the quartz features. Additional amounts of oxygen may be necessary to minimize polymer formation. The process sequence for 30 nm features is depicted in Fig. 4.

Widespread use of imprint lithography will require that the template be both inspectable and repairable. For applications requiring sub-100 nm lithography, it will likely become necessary to inspect the templates using electron beams. If this is the case, the template will need a charge reduction layer to dissipate charge during the inspection process. A fabrication scheme that incorporates a transparent conducting oxide, such as ITO, into the final template addresses this problem. A thin layer of plasma enhanced chemical vapor deposition (PECVD) oxide is deposited over the ITO and defines the thickness of the imprinted resist layer. Features are formed on the template by patterning an electron-beam resist, transferring the pattern via reactive etching into the oxide, and stripping the resist.

The ITO must have sufficient conductivity to avoid charging effects first during resist exposure and later during template inspection. The resistivity of the as-deposited ITO film is on the order of $2.0 \times 10^6$ ohm/sq. The resistivity decreases substantially, however, after the films are annealed at a temperature of 300 °C. In its annealed state, the ITO film resis-
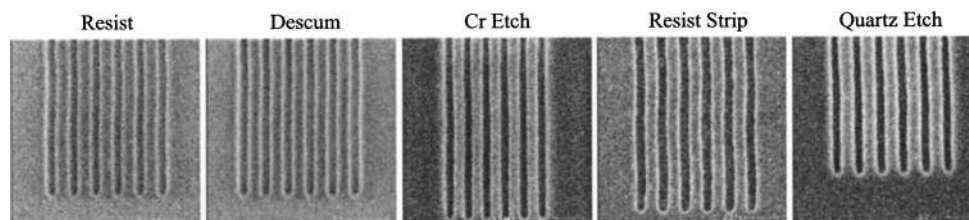


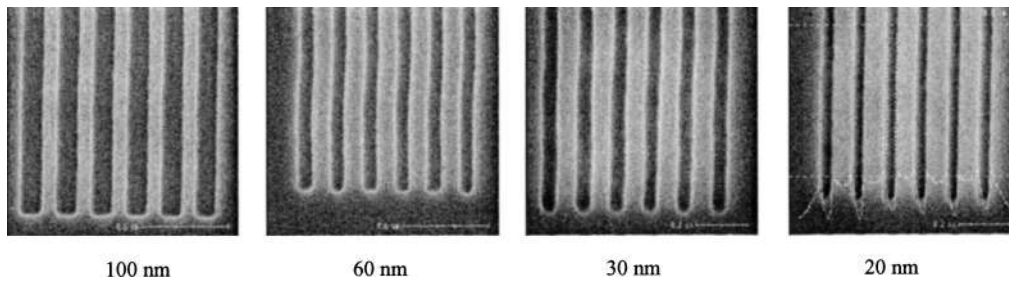FIG. 4. Template pattern transfer sequence for 30 nm features.

FIG. 5. 100, 60, 30, and 20 nm features defined using the ITO-based process.

tivity is about $3.5 \times 10^2$ ohms/sq. Charge dissipation during electron-beam writing and SEM inspection is realized at this conductivity level. The ITO must be also be very transparent at the actinic wavelength used during the S-FIL exposure process (365 nm). It is possible to achieve transmission well above 90% at 365 nm.[13] The ITO has the additional attribute of performing as an excellent etch stop during the pattern transfer of the PECVD oxide layer. Examples of final template features formed using this process are shown in Fig. 5.

An even simpler way to make a template is to use an electron-beam sensitive flowable oxide, such as hydrogen silsequioxane (HSQ). While the primary use of HSQ is as a low-*k* dielectric, several investigators have demonstrated its usefulness as a high-resolution electron-beam resist. In its cured state, HSQ becomes a durable oxide making it a very convenient material for direct patterning of S-FIL template relief structures. Processing of HSQ as an electron-beam resist is less complicated since it is not chemically amplified, and can be developed in the standard tetramethyl ammonium hydroxide-based developers used commonly for conventional resists. All that is required to make a template is to coat and bake the HSQ directly on the ITO layer, and then expose and develop the HSQ.[14]

It is interesting to note that the methods described in this section can also be used sequentially to form multilayer structures that can be used to fabricate devices such as T-gates or optical grating couplers.[15] SEM pictures depicting two-tiered and three-tiered structures are shown in Fig. 6. Figures 6(a) and 6(b) are tiered structures produced using alternating layers of ITO and PECVD oxide. Figure 6(c) was produced by patterning a bottom oxide film and subsequently coating, exposing, and developing an HSQ layer.

The final step in the template fabrication process is a treatment designed to lower the surface free energy. Alkyltrichlorosilanes form strong covalent bonds with the surface of fused silica, or $SiO_2$. In the presence of surface water, they react to form silanol intermediates that undergo a condensation reaction with surface hydroxyl groups, and adjacent silanols to form a networked siloxane monolayer. When this functional group is synthetically attached to a long fluorinated aliphatic chain, a bifunctional molecule suitable as a template release film, is created. The silane terminated end bonds itself to the surface of a template, providing the durability necessary for repeated imprints. The fluorinated chain, with its tendency to orient itself away from the surface, forms a tightly packed comblike structure and provides a low-energy release surface. Annealing further enhances the condensation creating a highly networked, durable, low surface energy coating.

## IV. RESIST

The resist stack typically consists of a silicon containing etch barrier over an antireflective coating (also referred to as the transfer layer). The etch barrier is patterned via the imprint process. The subsequent pattern transfer process involves an etch of the remaining residual layer ($\sim$100 nm in thickness), followed by an anisotropic etch of the transfer layer.

The etch barrier material is subject to several design constraints. The etch barrier liquid must be dispensable from an automatic fluid dispense system, and must not change significantly in composition between dispensing and imprinting by, e.g., component evaporation. It must be readily displaced
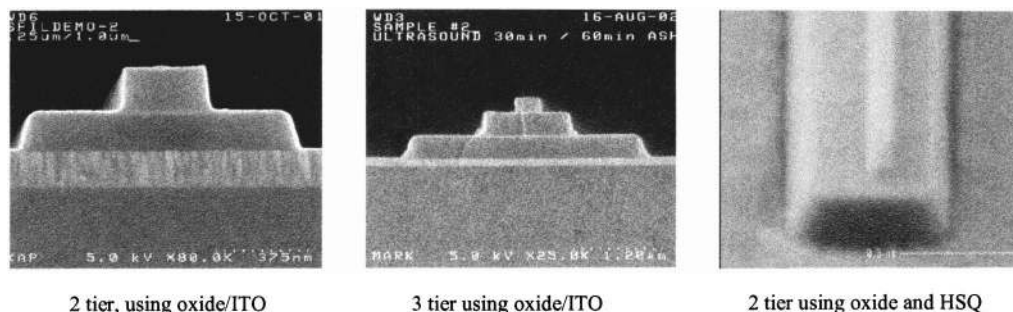


2 tier, using oxide/ITO          3 tier using oxide/ITO          2 tier using oxide and HSQ

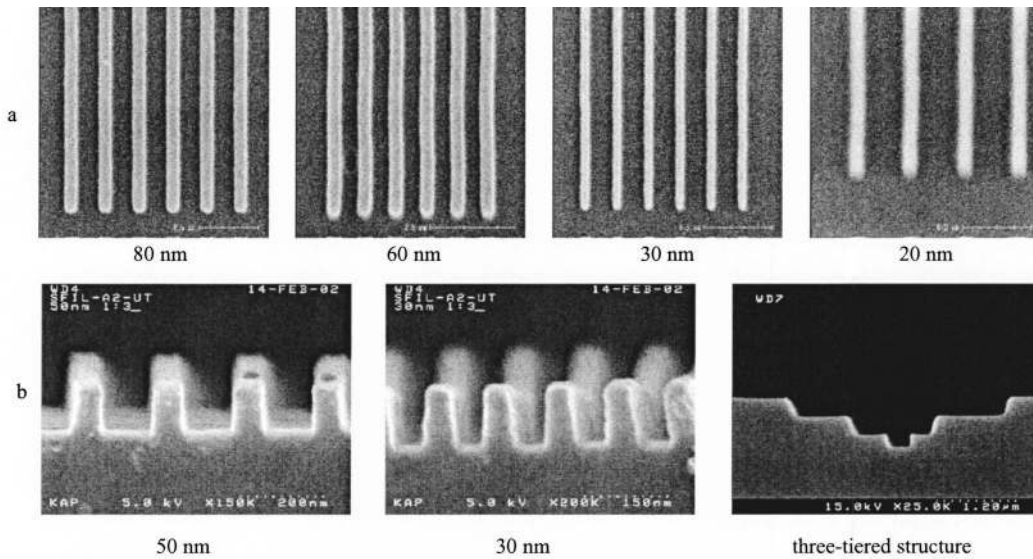FIG. 6. Multitiered structures formed by iterating the fabrication process.

FIG. 7. Printed features in the acrylate-based etch barrier. (a) Top-down SEMs. (b) Cross-sectional images of both single tier and multitiered features.

during the imprint step and photopolymerize rapidly during exposure. Shrinkage due to polymerization must be controlled. The polymer must release from the template while adhering to the transfer layer, and it must exhibit sufficient rigidity to avoid feature collapse. It must exhibit some level of temperature stability to withstand the etching temperatures, and it must exhibit sufficient etch selectivity during the $O_2$ reactive ion etching step to allow for high aspect ratios to be generated in the transfer layer.

The S-FIL process relies on photopolymerization of a low viscosity acrylate-based solution. Acrylate polymerization is known to be accompanied by volumetric shrinkage that is the result of chemical bond formation. Consequently, the size, shape, and placement of the replicated features may be affected. Volumetric shrinkage was found to be less than 10% (v/v) in most cases.[16]

The current etch barrier liquid is a multicomponent solution that has been previously been described in detail.[16] The silylated monomer provides etch resistance in the $O_2$ transfer etch. Crosslinker monomers provide thermal stability to the cured etch barrier and also improve the cohesive strength of the etch barrier. Organic monomers serve as mass-persistent components and lower the viscosity of the etch barrier formulation. The photoinitiators dissociate to form radicals upon UV irradiation, and these radicals initiate polymerization.

SEMs of this etch barrier are shown in Fig. 7(a) 20 nm features have been resolved with both types of templates described earlier. Cross sectional images are shown in Fig. 7(b). The profiles closely replicate the relief image in the template for both single and multitiered structures. CD uniformity studies have also been performed. In one study an $8 \times 8$ array of features were defined on a template. The template was then used to print a die on a wafer. The CD variation was measured using a Hitachi 7800 CD-SEM for both the template and the etch barrier. The results for 30 nm fea-

tures are shown in Fig. 8. As expected, there is only a small additional variance in the CD caused by the printing process.[17]

Prior to etching the underlying transfer layer, it is necessary to remove the residual etch barrier material formed during the imprint process. Because the silicon content is at least 12%, best selectivity between the etch barrier and the transfer layer is achieved by using a combination of $CF_4$ and oxygen. Once the transfer layer is exposed, the gas chemistry is comprised only of $O_2$. Recent studies indicate that selectivities greater than 6:1 may be possible for both etches. Figure 9 shows the pattern transfer sequence. More details on this process can be found in a previous publication.[18]

It is interesting to note that the presence of oxygen dissolved in the etch barrier and in the ambient environment causes two undesirable effects on the curing of the acrylate etch barrier. Oxygen dissolved in the etch barrier consumes photoinitiated radicals, resulting in an inhibition period before polymerization begins. Furthermore, oxygen diffusion into the etch barrier limits the curing reaction around the perimeter of the template. While it may be possible to modify the ambient, other chemistries, such as vinyl ethers
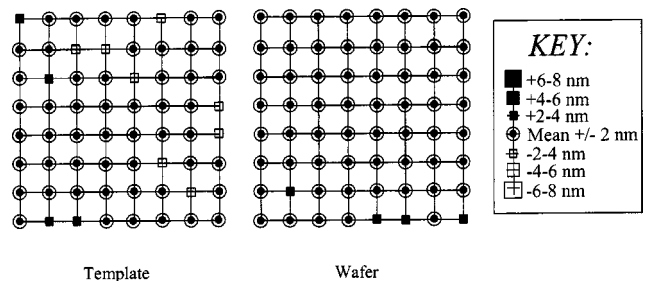


FIG. 8. CD variation plots of 30 nm features for both the template and the etch barrier. The $3\sigma$ values for the template and the printed field are 4.5 nm and 4.4 nm, respectively.
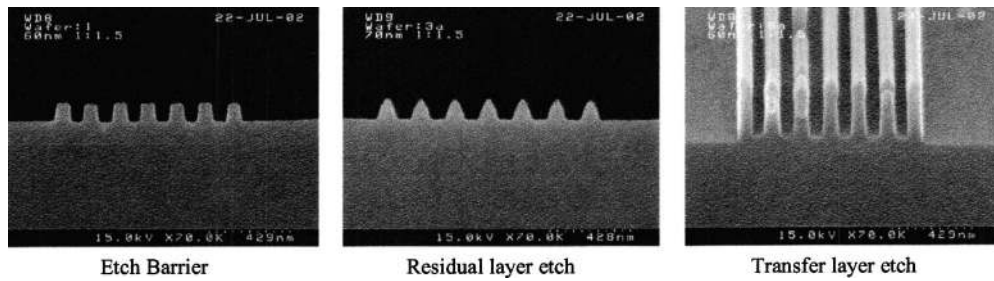
FIG. 9. Pattern transfer sequence showing the etch barrier over the transfer layer, the residual layer etch, and the etch of the transfer layer.

may be more suitable for the imprint process.[18] This approach eliminates the oxygen inhibition effect and may also further reduce the viscosity of the etch barrier, thereby further reducing the residual layer formed during the imprint process.

## V. ISSUES

Several other issues need to be addressed before S-FIL can be considered as a viable technology for silicon IC fabrication. The two biggest issues are defects and overlay. Because imprint lithography is a "contact" lithography, there are concerns associated with defects generated during the process. As a 1X technology, there are also concerns relative to template to wafer alignment. Each of these topics is discussed below.

### A. Defects

The low surface energy monolayer applied to the template acts effectively as a self-cleaning agent. This attribute has been reported in several publications.[5,8] A dirty template was used to imprint several die on a silicon wafer. The progression of pictures indicated that defects that start on the template embed themselves in the etch barrier, and by the seventh imprint, there were no detectable particles. It is also interesting to note that there does not appear to be any degradation of the release layer over time. Contact angles measurements show no change after more than two months.[5]

While the data clearly illustrate a self-cleaning effect, this is not sufficient evidence to prove that defects are not added after many imprints. A more convincing study involves printing wafers, and having the defects tracked using an inspection tool. To this end, a study of imprinted wafers was conducted on a KLA-Tencor 2139 wafer inspection tool in collaboration with KLA-Tencor.[18] Initial inspection of 96 consecutive imprints shows relatively high levels of detected defects, but no significant upward trend in defects over time, as shown in Fig. 10(a). Although the data are noisy and the number of defects is relatively large, there does not appear to be an increase in defects. Statistical analysis of these data has been performed. Figure 10(b) depicts the relationship between the number of defects added per imprint and the number of imprints. As the size of the data set increases, there is a change in the data that shifts the slope and its confidence downward to capture zero.

A more recent study examined the surface of a 320 $\mu m^2$ imprinted field containing 30 nm, 40 nm, and 50 nm lines with varying pitches. The results for the 50 nm features are shown in Fig. 11. Scanning electron micrographs depict the field after imprint numbers 1, 169, and 300. The results are nominally the same for each picture: The 50 nm lines remain intact, and no defects are visible in the field of view.

### B. Image placement and overlay

Two concerns are worth addressing. (1) Does the template fabrication process result in image placement errors that cannot be removed using conventional correction techniques
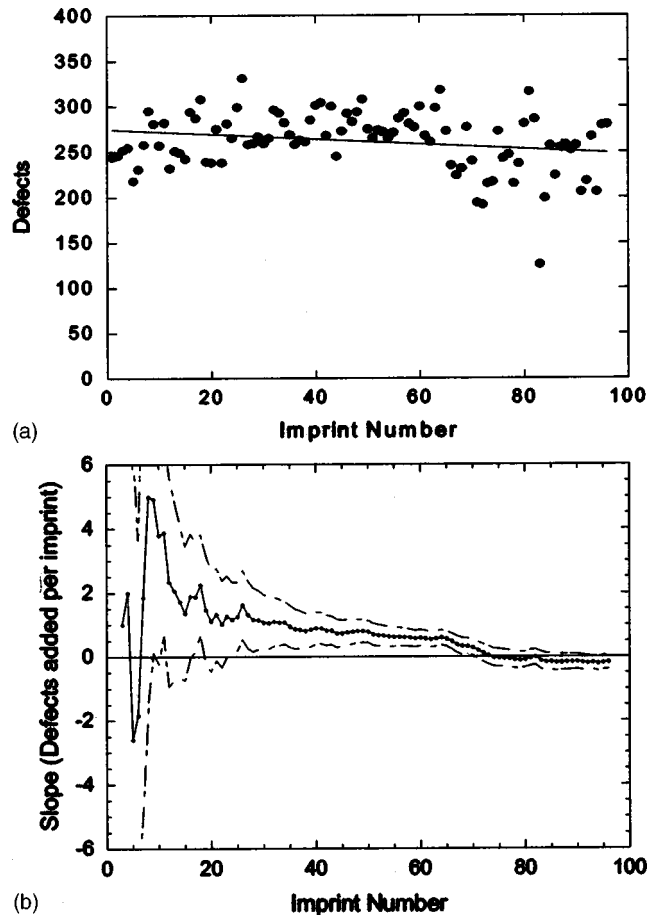


FIG. 10. (a) Defect levels vs imprint number. (b) Number of defects added per imprint as a function of imprint number.
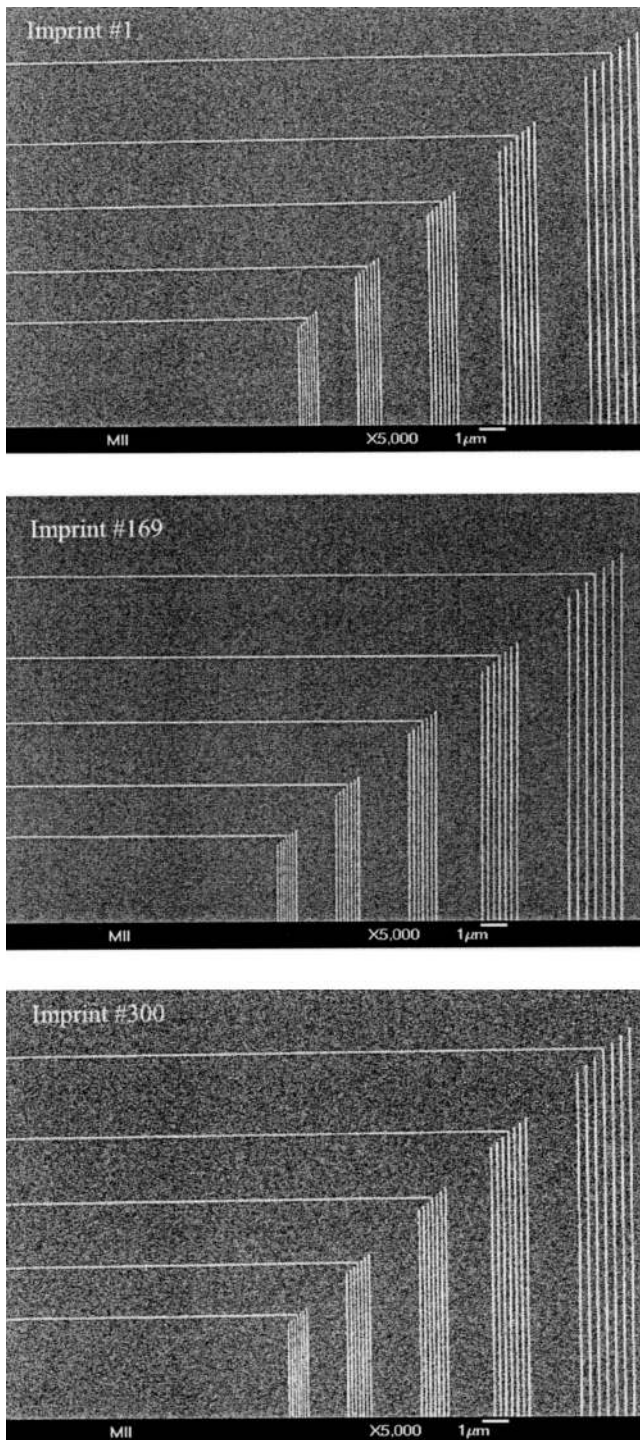
FIG. 11. Imprinted field containing 50 nm lines with varying pitches. Scanning electron micrographs depict the field after imprint number 1, 169, and 300. The results are nominally the same for each picture: the 50 nm lines remain intact, and no defects are visible in the field of view.

such scale and orthoganality corrections? (2) If image placement is good, can the imprint tool align and make the corrections necessary to meet the stringent requirements for silicon processing?

To examine image placement, a 6025 photoplate was patterned over a 5 in.×5 in. area with alignment marks. Image placement was measured using a Leica LMS 2020 during each step of the Cr/Quartz template fabrication process described in a previous publication.[10] The resultant image placement errors has a maximum error of approximately 15 nm. This error can be attributed to the stress of the chromium film. The image placement errors experimentally observed agree very well with finite element models.[19]

To determine what type of overlay error would result from the patterning process, a second plate was written, using an opposite tone resist. The center 1 in.×1 in. (a typical field size) areas of both plates were then compared. The result, after correcting for scale and orthoganality are shown in Fig. 12(a).[20] The displacement vectors are typically less than 10 nm and are randomly directed, indicating that the error vectors are mostly limited to the sensitivity of the LMS 2020.

The issue of overlay comes down to the capabilities of the imaging system and the method used for imprinting. Because S-FIL is a room-temperature and low-pressure (≤1 psi) process, the real concern becomes the ability of the tool to overlay different mask levels. Tool capability has two major components: The first is related to the alignment method and alignment optics. The second is the ability to correct for distortion errors such as magnification and orthoganality.

The current method of alignment on the Imprio 100 takes advantage of the transparent template, and a through the template alignment system is used to align marks on both the wafer and template. This type of system may actually be advantageous relative to reduction systems, since distortion errors from the lens elements are eliminated. It is important to note the differences between alignment in an S-FIL tool, such as the Imprio 100 and a typical contact aligner. First, alignment in the S-FIL tool is performed for each die, thereby minimizing runout errors. Second, alignment adjustments can be made with the template and wafer in contact. Across most of the die, the template and substrate are actually separated by the liquid etch barrier. In the area of the alignment mark, however, there is no etch barrier. This is important distinction, since the etch barrier and the template are closely index matched. If the etch barrier was allowed in the alignment mark area, it would not be possible to image the mark. Alignment adjustments are possible in this scheme, because the etch barrier is still a liquid. It should be a straightforward task, therefore, to align within a few hundred nanometers. An example of an aligned template and wafer is shown in Fig. 12(b).

The real challenge, then, is to be able to correct for distortion between the template and wafer. One possible way to accomplish this is to set a series of piezos around the template. To date, modeling[21] and preliminary experiments suggest that the use of a template whose thickness is substantially larger than the depth of the etched features allows for magnification corrections that are independent of the features etched into the template. Also, very uniform strain fields can be obtained using mechanical means. Experimental verification of these magnification systems as part of a complete imprinting step and repeat tool still remains to be done.
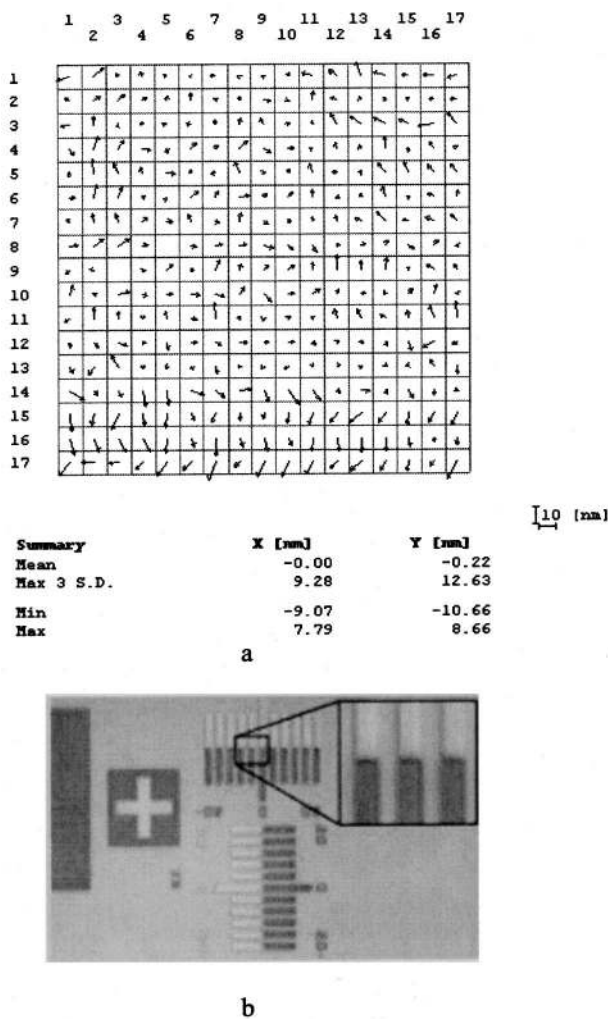
| Summary | X [nm] | Y [nm] |
|---|---|---|
| Mean | -0.00 | -0.22 |
| Max 3 S.D. | 9.28 | 12.63 |
| Min | -9.07 | -10.66 |
| Max | 7.79 | 8.66 |

a



b

FIG. 12. (a) Distortion map comparing the center 1 in.×1 in. areas from two different templates. (b) An example of aligned verniers for the S-FIL overlay process.

## VI. CONCLUSIONS

NIL has come a long way in a very short period of time. Resolution seems limited to the ability to form a relief image in the template and sub-10 nm printing has already been demonstrated. To be considered as a method for fabricating silicon ICs, several concerns still need to be addressed. UV-NIL, and in particular S-FIL, seem the best imprinting option for meeting the stringent requirements of future generations of silicon-based circuitry. Tools, templates, and resists are readily available to start exercising the technology and will be used to answer the open issues, such as defectivity and overlay. If these issues can be solved, imprint lithography may be the right NGL, since extendibility to at least 10 nm seems viable. The last consideration, then becomes the supporting infrastructure. Reduction lithography has been in the mainstream now for over 20 years, and the ability to write, inspect, and correct a IX template will need to be developed. Electron-based inspection and repair tools, as well as faster Gaussian-based electron-beam writing systems may provide the pathway for template fabrication in the future.

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