Improved Constant-Frequency Hysteresis Current Control of VSI Inverters with Simple Feedforward Bandwidth Prediction

Luigi Malesani, *Fellow, IEEE,* Paolo Mattavelli, *Associate Member, IEEE,* and Paolo Tomasin

***Abstract*— An improved implementation of the constant-frequency hysteresis current control of three-phase voltage-source inverters is presented. A simple, self-adjusting analog prediction of the hysteresis band is added to the phase-locked-loop control to ensure constant switching frequency, even at a high rate of output voltage change, such as required in active filters, fast drives, and other highly demanding applications. This provision also improves the relative position of phase modulation pulses, thus reducing the current ripple. The prediction method is robust and uses a small number of inexpensive components. It does not require trimming or tunings, giving the whole system the capability to adjust itself to different load conditions. Thus, the control becomes suitable to hybrid or monolithic integration. In this paper, the basic principles are described, and a detailed stability analysis is done. The control performance is illustrated, both by simulated and experimental results.**

***Index Terms*—Constant switching frequency, hysteresis current control, voltage-source inverters.**

I. Introduction

HYSTERESIS current control of voltage-source inverters (VSI's) offers an unsurpassed transient response in comparison with other analog and digital techniques, which makes it advisable to adopt this method in all cases where high accuracy, wide bandwidth, and robustness are required [1]–[5].

Hysteresis control is essentially an analogic technique. Despite the advantages given by the digital controls, in terms of interfacing, maintenance, flexibility, and integration, their accuracy and response speed are often inadequate for current control in highly demanding applications, such as active filters and high-precision drives [6]–[10]. Indeed, in these applications, current reference waveforms characterized by high harmonic content and fast transient must be followed by good accuracy. In these cases, the hysteresis method can be a good solution, provided some improvements are introduced to overcome its main limitations, which are the variations of the switching frequency and the sensitivity to phase commutation interferences. To this purpose, a variety of provisions, both analog and digital, have been proposed by several authors [11]–[18]. According to the actual trend, some proposals are almost completely digital, limiting the analog functions only to the band-crossing detection [19], [20].

However, when high switching frequency is demanded, analog solutions offer the fastest performance with a relatively simple implementation. A fully analog technique, which eliminates the interference and gives constant switching frequency, was presented some time ago in [11]. This technique was extensively used and proved to be robust and reliable. By means of a phase-locked-loop (PLL) control, it synchronizes the phase commutations to a clock, thus ensuring the control of the reciprocal positions of the phase pulses. In this condition, similarly to the vector modulation, ripple and noise in the load are reduced.

However, the synchronization becomes difficult in the presence of fast variations of the output voltage, which occur when fast transient or high-order harmonics are met. As a consequence, the switching frequency varies around its reference value, producing an increased ripple the spectrum of which extends appreciably below the average switching frequency. These effects, which can often be neglected in the usual drive applications, are of some importance in high-performance drives, ac/dc pulsewidth modulation (PWM) converters, and active filters. In these applications, the current error affects the accuracy. In active filters and ac/dc PWM converters, it represents the residual harmonic content of the current, which is limited by standards (e.g., IEC-555) and calls for suitable line input filters of nonnegligible size. If the PLL bandwidth is increased to improve the speed of response, reduced stability margins turn out in an increased sensitivity to supply voltage variations, which represent a serious cause of disturbance of the regular hysteresis control operation.

A substantial improvement in system response can be achieved, without affecting the stability, by adopting a feedforward calculation of the hysteresis band. The first idea based on this approach, has been recently proposed in [18]. This method solves the problem of obtaining constant switching frequency by a purely feedforward algorithm which calculates the hysteresis band as a function of system variables.

A further improvement of the feedforward calculation of the hysteresis band is proposed in the present paper. It is

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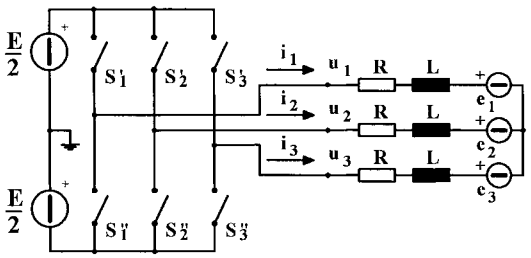

Fig. 1. Three-phase VSI with motor load.

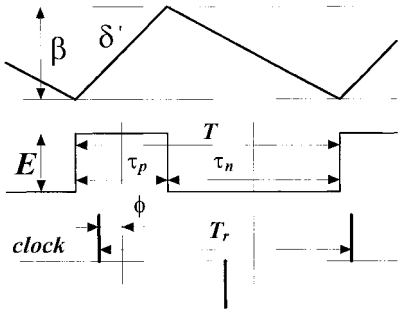

Fig. 2. Hysteresis comparator operation.

characterized by the use of both a feedback and feedforward control, which allows a noncritical estimation of the system parameters and even a self-adjusting capability to the parameter variations. Moreover, by the use of a proper estimation algorithm, operations such as multiplication and division, which are difficult to implement by analog components, are eliminated, so that a very limited number of conventional analog components is needed. Finally, the reciprocal pulse position is kept under control, while the feedforward action helps the PLL action; thus, the PLL bandwidth can be reduced, resulting in a better stability. The proposed method is well suited to high-frequency high-performance current controls.

II. Principles of Operation

A. Three-Phase Decoupled Hysteresis Control

In order to explain the proposed feedforward method, let us first recall the basic concepts of the constant-frequency interference decoupled hysteresis current control described in [11].

In Fig. 1, a three-phase VSI is shown with the equivalent scheme of a typical load. This represents equally well a motor or an output *LC* filter followed by a generic load.

The load equations are

$$\boldsymbol{u} = R\boldsymbol{i} + Ld\boldsymbol{i}/dt + \boldsymbol{e} + u_0\mathbf{1} \tag{1}$$

$$u_0 = (u_1 + u_2 + u_3)/3 \tag{2}$$

where $\boldsymbol{u}$ and $\boldsymbol{i}$ are vectors of the inverter output voltages and currents, respectively, u_0 is the load midpoint voltage, and $\mathbf{1}$ is the unity vector. All voltages are referred to the supply midpoint.

If $\boldsymbol{i}^*$ are the reference currents, the phase reference voltages may be defined as

$$\boldsymbol{u}^* = R\boldsymbol{i}^* + Ld\boldsymbol{i}^*/dt + \boldsymbol{e} \tag{3}$$

and the instantaneous current errors as

$$\boldsymbol{\delta} = \boldsymbol{i} - \boldsymbol{i}^*. \tag{4}$$

Due to the action of load midpoint voltage u_0, each phase current error is affected by the commutations in the other phases. This interference causes severe irregularities in the ordinary hysteresis operation. By introducing a decoupling term $\boldsymbol{\delta}''$ such as

$$Ld\boldsymbol{\delta}''/dt + R\boldsymbol{\delta}'' = -u_0\mathbf{1} \tag{5}$$

an interference-free modulation can be obtained if the hysteresis control is performed on the decoupled error terms

$$\boldsymbol{\delta}' = \boldsymbol{\delta} - \boldsymbol{\delta}'' \tag{6}$$

instead of total errors $\boldsymbol{\delta}$. Indeed, from (1)–(6), it results

$$Ld\boldsymbol{\delta}'/dt + R\boldsymbol{\delta}' = \boldsymbol{u} - \boldsymbol{u}^* \tag{7}$$

which shows that terms $\boldsymbol{\delta}'$ are independent from u_0.

B. Constant-Frequency Hysteresis Phase Current Control

Once decoupled, each phase control can be performed independently. The instantaneous phase voltage has a rectangular waveshape of amplitude $\pm E/2$, with duration τ_p of the positive pulse and τ_n of the negative one, for a total period T (Fig. 2). Usually, the effects of load resistance R can be neglected, and the phase reference voltage u^* can be considered constant during a modulation period; from (7), it results that current error δ' has a triangular behavior, as shown in Fig. 2. In these assumptions, from (7), it also results that the average of the phase voltage u over T is equal to u^*. By defining the normalized phase voltage

$$u_n = u^*/(E/2) \tag{8}$$

and with reference to Fig. 2, it can be derived

$$T = \frac{4\beta L}{E\left[1 - u_n^2\right]} \tag{9}$$

$$\tau_p = T\frac{1+u_n}{2} \quad \tau_n = T\frac{1-u_n}{2} \tag{10}$$

where β is the width of the hysteresis band.

Equation (9) shows that, if β is constant, a variable modulation frequency is produced. To obtain a constant period T_r, the ripple amplitude, like ramp-comparison control, must vary with the instantaneous value u_n. Accordingly, the variation of the hysteresis band is expressed by

$$\beta = \frac{ET_r}{4 \cdot L}\left[1 - u_n^2\right]. \tag{11}$$

The classic analogic tool to control β so as to obtain a fixed frequency is a PLL. This solution, proposed in [11], employs the hysteresis modulator as a nonlinear voltage controlled oscillator (VCO) (Fig. 3, except the part within the

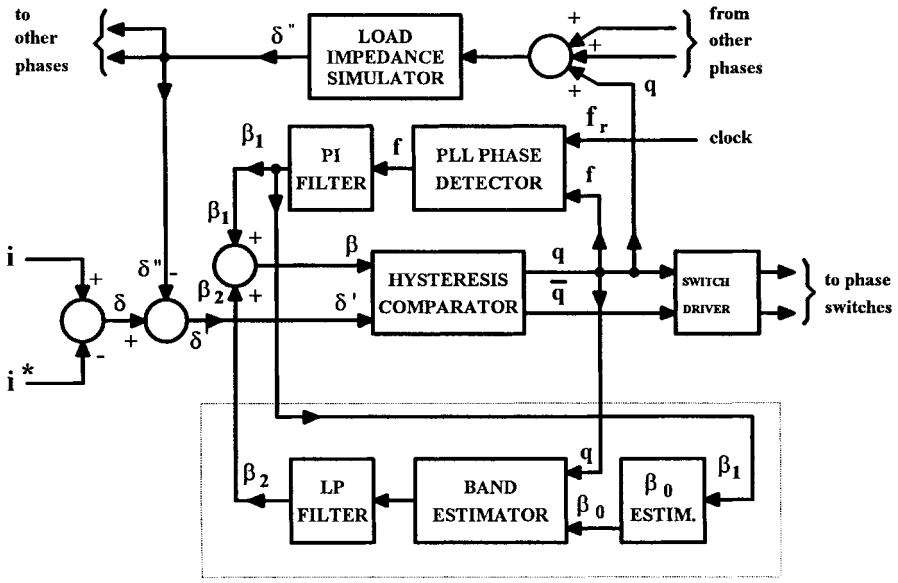

Fig. 3. Constant-frequency hysteresis current control.

dashed frame). It can also be adopted in three-phase systems, as the decoupling eliminates the phase mutual dependence and reduces the waveform irregularities of the error signal δ'.

An interesting feature of PLL is that it not only keeps under control the modulation frequency, but also the phase of the output voltage pulses. For three-phase systems, by using the same reference clock for all phases, it allows the system to approach the "centered pulses" condition which is characteristic of space-vector control and gives an optimal reduction of the current ripple [21].

Unfortunately, while the PLL is very effective in ensuring a stable lock to the clock frequency reference, it is only able to limit the phase displacements for quite slow variation rates of u_n, so as to give reduced current ripple. To make the bandwidth β fit fast variations of u_n with small displacement angle, a high PLL bandwidth is called for. This requirement, however, is in conflict with the stability conditions, mainly because of large loop gain variations which are produced by the changes of u_n, according to (11).

An alternative approach to the constant-frequency operation is proposed in (18), where an open-loop prediction of the proper bandwidth is adopted. This solution is able to ensure fast response, as it is not affected by stability problems. However, to be accurate, the method requires a precise estimation of the system parameters. Moreover, the centered condition is not ensured, since there is no direct control of the phase of modulation pulses.

C. Feedforward/Feedback Modulation Frequency Control

To overcome the limitations of the previous constant-frequency hysteresis controls, a combined approach can be adopted; a feedforward band prediction tracks the variations of the output voltage, leaving to the PLL the task of keeping the phase displacement under control and correcting for the estimation errors. The benefits of this approach are enhanced, if the prediction can be implemented in a simple way.

The basic scheme of such a control is shown in Fig. 3. The hysteresis band amplitude β is obtained by the sum of the PLL term β_1 and the feedforward term β_2.

The PLL loop has the same structure described in [11], with a three-state edge-triggered phase detector (like that of the comparator II available in the IC CD4046 of the CMOS logic series) followed by a PI filter. This type of detector guarantees a capture range equal to the lock range and gives a zero average phase error. The implementation of the detector/filter functions, including a lower limitation of the band amplitude and the centering of the pulses with respect to the clock reference, can be done in various ways [11], [22], but essentially results in the same transfer function.

The band estimator block calculates β_2 as a function of u_n, according to (9) and (10). Thus, it needs as its input only the signal q, while the reference period $T_r = 1/f_r$ is considered a datum.

The hysteresis comparator is common to the two loops. It has as inputs the error signal δ' and the band β, and produces the two complementary command signals q and $\bar{q}$, which carry the frequency and phase information.

With an ideal estimator performance, β_2 would be equal to the theoretical value of β given by (11), which is independent from the actual modulation frequency f. In this hypothesis, the PLL output β_1 would always be nul, resulting in a zero phase error.

In practice, in addition to the circuit errors and inaccuracies, some approximations may be introduced in the estimation process in order to allow a simple implementation of the estimation block. Thus, the PLL has to correct for these inaccuracies, requiring some amount of phase error.

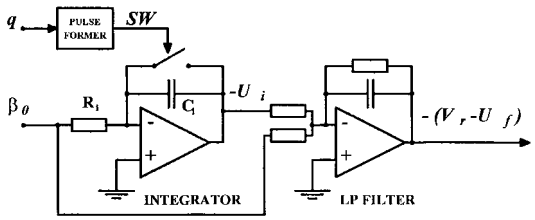

Fig. 4. Simplified estimator implementation.

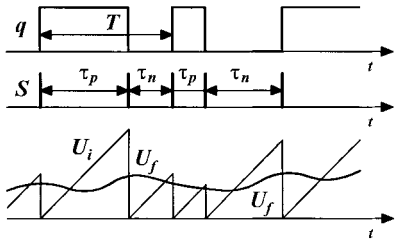

Fig. 5. Simplified estimator waveforms.

A simple implementation of the band estimator can be derived by rearranging (9)–(11):

$$\beta_2 = 4\beta_0 \frac{\tau_p \cdot \tau_n}{T^2} = 2\beta_0 \left[1 - \frac{\tau_p^2}{T^2} - \frac{\tau_n^2}{T^2}\right] \tag{12}$$

where the reference band β_0 is the hysteresis band needed for a fixed frequency at zero phase voltage, given by

$$\beta_0 = \frac{E \cdot T_r}{4L}. \tag{13}$$

The second expression of β_2 in (12) can be approximated as follows:

$$\beta_2 \cong 2\beta_0 \left[1 - \frac{\tau_p^2}{T_r \cdot T} + \frac{\tau_n^2}{T_r \cdot T}\right] \tag{14}$$

with a decreasing error as modulation frequency approaches f_r.

The implementation of (14) can be done in a simple way, as shown in Fig. 4. The reference band β_0 is integrated over time intervals τ_p and τ_n with a time constant $R_iC_i = T_r/4$. The integrated output U_i is nulled at every transition of the driving signal q, thus producing a series of triangles the area of which is proportional to τ_p^2 and τ_n^2, as shown in Fig. 5. A low-pass filter gives U_f, which follows the average value of U_i, calculated over the actual period T. Thus, U_f corresponds to the second addendum of (14). The approximated value of β_2 is obtained simply by adding the reference band β_0.

For constant system parameters (E, L, and T_r), β_0 is a constant quantity which can immediately be derived from (13). In this instance, β_0 coincides with its average value, and it is irrelevant to make the addition before or after the filter (Fig. 4). Like the PLL control, the feedforward prediction proved to be fairly tolerant of parameter variations. Indeed, a mismatch only increases the contribution β_1 given by the PLL.

If the load parameters are unknown, β_0 can be determined by adding a simple control loop. Indeed, according to (11), a correct value of β_0 gives the exact band prediction β_2 through (14) and reduces to zero the PLL output β_1. Even taking into account the presence of ripple, these conditions are met for the average values of β_1 and β_2. Thus, a closed-loop control can be set up by means of an integrating error amplifier with signal β_1 as input and β_0 as output. By a proper choice of the integrator constant, the loop response can be made slow enough in order not to affect the regular operation of the hysteresis control. This control also ensures a tracking of the system parameter variations, namely, supply voltage E and load inductance L, provided they are not too fast.

Moreover, it can be demonstrated that β_0 can also be employed in the calculation of decoupling term δ'', thus giving the control a full self-adjusting capability.

The implementation of the estimator of band β_2 described above is characterized by its simplicity, although the introduced approximations have some impact on the system stability, as shown later. Of course, more precise estimators may be devised, like that adopted in [18] or based on (12), instead of (14). They give an almost exact calculation of β_2, affected only by one modulation period delay, but they typically require at least one multiplier or divider per phase. When associated to the PLL loop, they would allow a tight control of the modulation phase displacement.

III. Stability Analysis

Stability analysis is performed, as usual, with reference to time average over the modulation period.

In principle, estimation of β_2 according to (11) does not depend on the actual frequency f. Thus, estimation is a feedforward path and the stability conditions are determined only by the PLL path.

As is known, the PLL phase detector can be modeled as an integrator

$$\text{PHD} = \frac{1}{s}. \tag{15}$$

The filter following the PLL typically has a PI structure

$$\text{PI} = K_p \frac{1 + sT_z}{sT_z} \tag{16}$$

K_p being the high frequency gain and T_z the zero of the filter.

The hysteresis comparator of Fig. 3 can be modeled according (9), which gives $f = 1/T$ as a function of u_n and β. Thus, u_n and β can be considered the input variables and by substituting in (9) $f = 1/T$ and making the partial derivatives versus u_n and β, the corresponding transfer functions HU and $H\beta$ are obtained:

$$HU = \frac{df}{du_n} = -\frac{E}{2L\beta} u_n \tag{17}$$

$$H\beta = \frac{df}{d\beta} = -\frac{E}{4L\beta^2}\left[1 - u_n^2\right]. \tag{18}$$

The PLL block scheme is represented in the upper part of Fig. 6. The loop gain GP, at the output of the hysteresis comparator, is obtained from (15), (16), and (18) and taking into account that, at the equilibrium, the condition (11) is

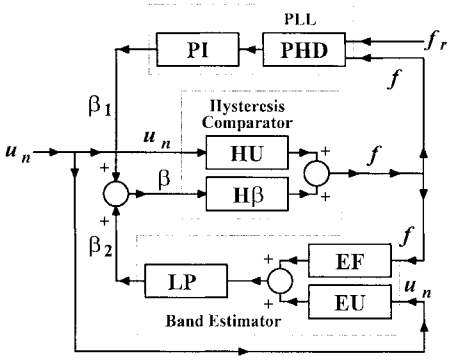

Fig. 6. Block scheme of the feedforward/feedback control.

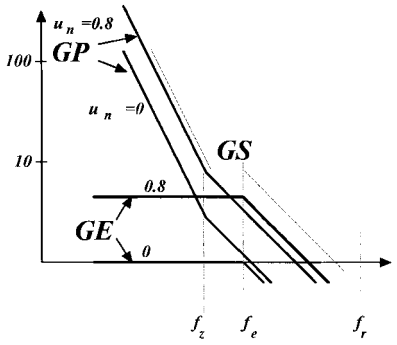

Fig. 7. PLL and estimator loop gains.

satisfied:

$$GP = -\frac{4\pi LK_p}{E}\frac{f_r^2}{\left[1-u_n^2\right]}\frac{1+sT_z}{s^2T_z}. \tag{19}$$

The GP gain varies appreciably with u_n. As an example, for a maximum modulation index of 95%, which corresponds to a range of u_n between ± 0.9, GP varies in a ratio of 1:5.3. To ensure stability in every condition, a suitable choice of the loop parameters must be done. In Fig. 7, the asymptotic Bode diagrams for the maximum and minimum gains, corresponding to the choice adopted for the experimental tests, are shown.

If an exact, truly feedforward estimation was performed, this limitation would not be of concern, as PLL has only the task of compensating for minor errors.

On the contrary, if an estimator approximated implementation, like that proposed above, is adopted, besides the feedforward action an additional feedback path is also generated. This acts in parallel to the PLL path, with the hysteresis comparator as a common block, as shown in Fig. 6. Indeed, in this case, β_2 is both a function of u_n and of f. By deriving (14) and taking into account (11), the corresponding transfer functions EF and EU are obtained:

$$EF = \frac{\beta_0}{T_r}\frac{1+u_n^2}{f^2} \tag{20}$$

$$EU = -\frac{2\beta_0}{T_r}\frac{u_n}{f} \tag{21}$$

while for the low-pass filter with time constant T_e, it results

$$LP = \frac{1}{1+sT_e}. \tag{22}$$

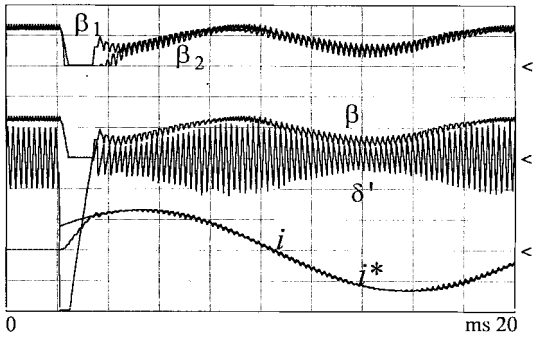

Fig. 8. Simulated behavior of hysteresis control with PLL only.

The loop gain GE of the estimation path, considered alone, is derived from (11), (13), (18), (20), and (22) and assuming that $f = f_r$

$$GE = -\frac{1+u_n^2}{1-u_n^2}\frac{1}{1+sT_e}. \tag{23}$$

GE varies with u_n even more than GP. For the same modulation index as above, the variation ratio becomes roughly 1:10. If β_0 has the proper value given by (13) and $u_n = 0$, GE has a low frequency amplitude equal to 1. At high values of u_n, near the unity, the low-pass filter reduces the feedback gain before the modulation frequency f_r. Typical Bode diagrams of GE are shown in Fig. 7.

The two feedback loops, acting in parallel, result in an overall loop gain GS given by their sum

$$GS = GP + GE. \tag{24}$$

To ensure the stability, for any value of u_n, the crossing of GS with the unity gain must be kept below f_r by a suitable margin.

The filter LP, needed to smooth the ripple and to ensure stability, also limits the feedforward action at high modulation frequencies. This mainly affects the effectiveness of the band estimation in reducing the phase displacements.

It should be pointed out that these limitations interest only the phase relationship between the phase pulses and affect only the current ripple. As in every hysteresis modulation, the average error over a modulation period remains essentially near zero.

IV. Simulation

The proposed control was extensively simulated to test its effectiveness and to evaluate the improvements with respect to the original constant-frequency hysteresis method [11], [22] and other current control methods [1]–[5]. The simulation was also employed for the choice of suitable parameters for the PLL and the band estimator, in order to optimize the response, while ensuring stability and robustness. As a results of this tradeoff process, it was found that it is advisable to keep the PLL bandwidth slightly lower than that of the estimator filter.

As an example of simulation results, in Fig. 8 the results obtained by the approximated hysteresis band estimation are shown; the behavior of the estimated band is compared with that given by the PLL acting alone.

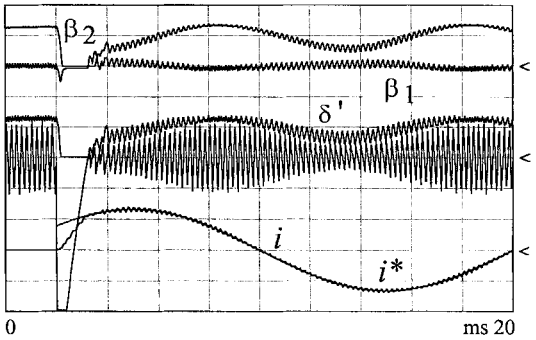

Fig. 9. Simulated behavior of hysteresis control with PLL and feedforward.

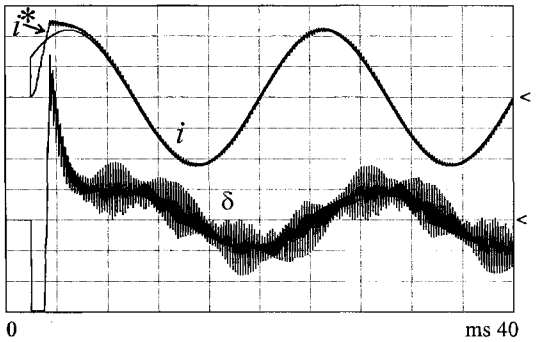

Fig. 12. Ramp-comparison current control simulated behavior.

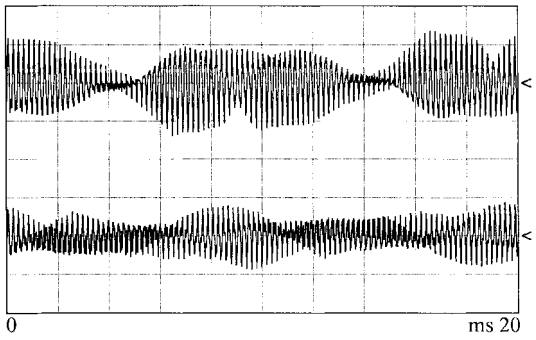

Fig. 10. Simulated total phase ripple δ. Top: with PLL only; bottom: with PLL plus feedforward.

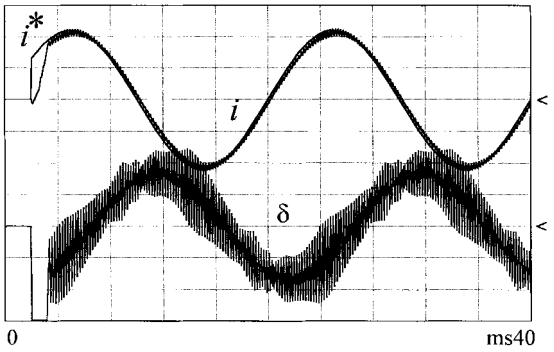

Fig. 13. Deadbeat current control simulated behavior.

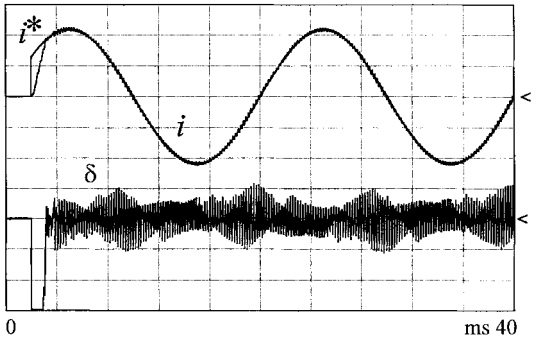

Fig. 11. Improved hysteresis current control behavior.

In Fig. 9, the results of the feedforward action are shown; the term β_2, given by the approximated estimator, almost coincides with the band β, while the mean value of the PLL output β_1 is kept near to zero.

In Fig. 10, the current error produced by the PLL control acting alone and that given by the proposed feedback/feedforward control are shown; noticeable improvement is obtained due to better phase pulse synchronization. These improvements were obtained notwithstanding a reduction of the PLL bandwidth and increased stability margin which passed from 12° to 35°.

In Fig. 11, the performance of the proposed control is illustrated, including the transient response. Phase current i and its reference i^*, together with the total error δ, are reported. The fast recovery after transient and the good accuracy can be appreciated.

For comparison, the same quantities obtained in the same conditions by a classic ramp-comparison control and by a deadbeat control (both tailored for an optimum response) are shown in Figs. 12 and 13, respectively.

In Fig. 12, the classic limitations of the ramp-comparison control are evident [1]–[5], [23]. Although the integral action keeps the average value of the output signal at zero, the proportional gain must be limited to ensure stability in the presence of current ripple. This gain cannot be made large enough to eliminate fluctuating components at line frequency and to respond to an appreciable transient. The maximum gain and the zero of PI control are related to the system parameters (namely, E and L) and must be derated in case of their variation. The above facts limit the analogy between ramp-comparison technique and the hysteresis [17].

Similarly, the intrinsic delay which is characteristic of deadbeat control, gives line frequency component in the current error, as shown in Fig. 13. Instead, the recovery after the transient is kept within good limits.

In Figs. 14–16, the corresponding error spectra, calculated in steady-state conditions, are reported. The reduced contents of the error component at the fundamental frequency, typical of the hysteresis control, is evident.

The above simulations were run assuming the same load and control parameters specified for the experimental tests.

V. Experimental Tests

The proposed control was tested on an insulated gate bipolar transistor (IGBT) inverter feeding a 2-kW induction motor. The measured motor parameters were: $L = 12.5$ mH, $R =$

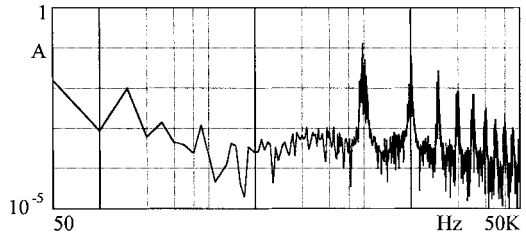

Fig. 14. Improved hysteresis simulated error spectrum.

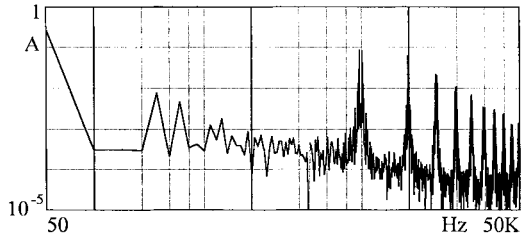

Fig. 15. Ramp-comparison simulated error spectrum.

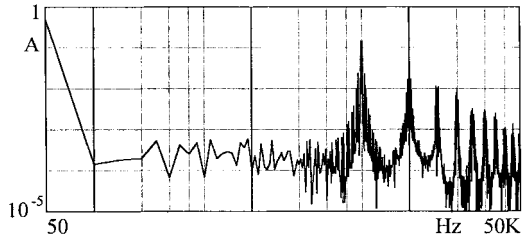

Fig. 16. Deadbeat simulated error spectrum.

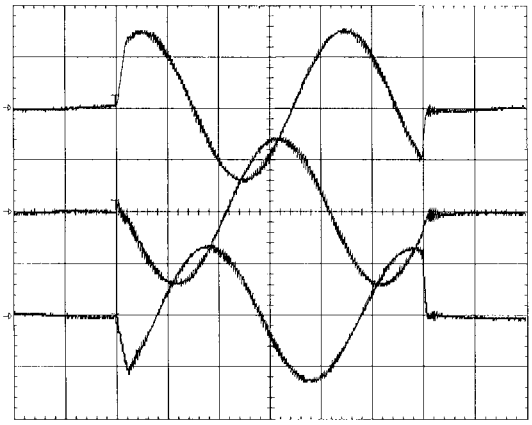

Fig. 17. Experimental transient response. Top to bottom: i_1, i_2, and i_3 (4 A/div, 5 ms/div).

2.2 Ω. The inverter modulation frequency was 5 kHz, with a dc-bus voltage $E = 300$ V.

The control parameters were: PLL zero frequency $f_z = 1/2\pi T_z = 186$ Hz, PLL filter gain $K_p = 0.75$, feedforward filter bandwidth $f_e = 1/2\pi T_e = 398$ Hz. The above parameters were the same as those assumed for simulation of Figs. 8–10.

The obtained system performance was accurate, robust, and stable for a wide range of output frequency, with fast response. A substantial improvement in sensitivity of the inverter operation and modulation frequency to the fluctuation of the supply voltage and to the variation of the loading conditions was experimented in comparison with those obtained by the simple PLL control.

In Fig. 17, the transient response is shown for three-phase symmetric currents of 4.7-A rms. The load EMF was estimated to be $e = 67$-V rms, corresponding to a maximum normalized

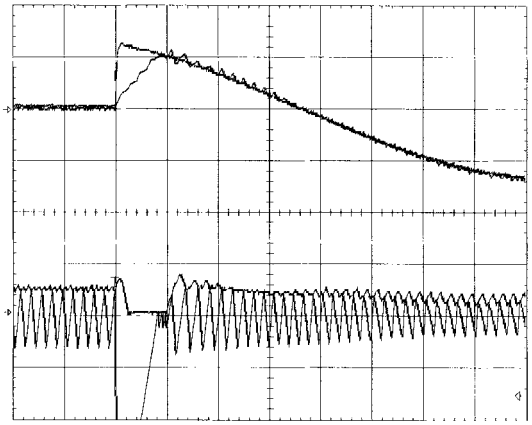

Fig. 18. Experimental transient response (expanded). Top to bottom: phase current reference (4 A/div, 1 ms/div), phase current (4 A/div), upper band limit $\beta/2$ (0.4 A/div), and decoupled current error δ' (0.4 A/div).

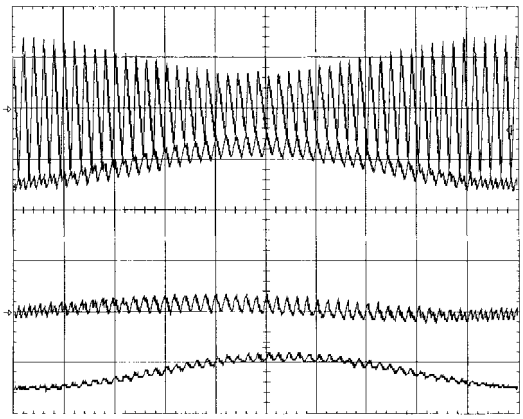

Fig. 19. Experimental feedforward control behavior. Top to bottom: decoupled error δ' (0.4 A/div, 1 ms/div), total band limit β (0.4 A/div), PLL output β_1 (0.4 A/div), and band estimator output β_2 (0.4 A/div).

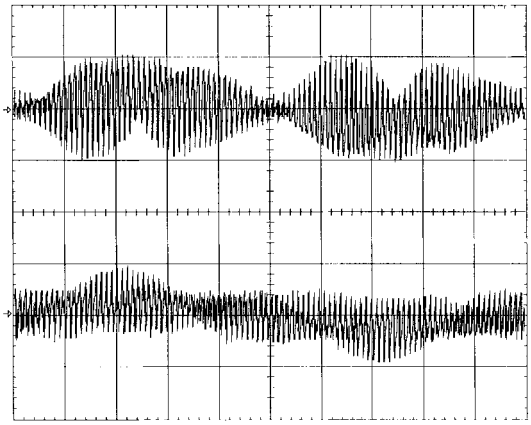

Fig. 20. Experimental total phase ripple δ. Top: with PLL only (0.4 A/div, 2 ms/div); bottom: with PLL plus feedforward (0.4 A/div).

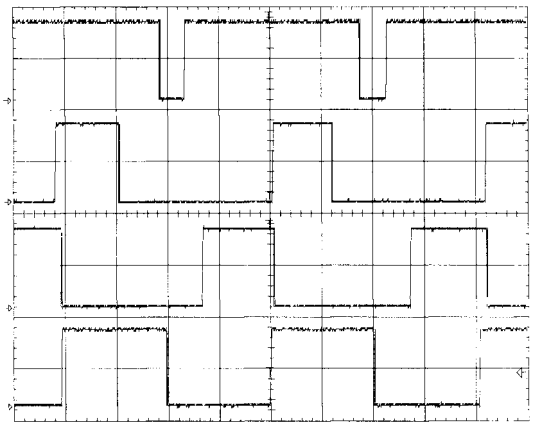

Fig. 21. Experimental phase pulses synchronization without feedforward. Top to bottom: phase 1 voltage u_1 (200 V/div, 50 μs/div), phase 2 voltage u_2 (200 V/div), phase 3 voltage u_3 (200 V/div), and clock (10 V/div).

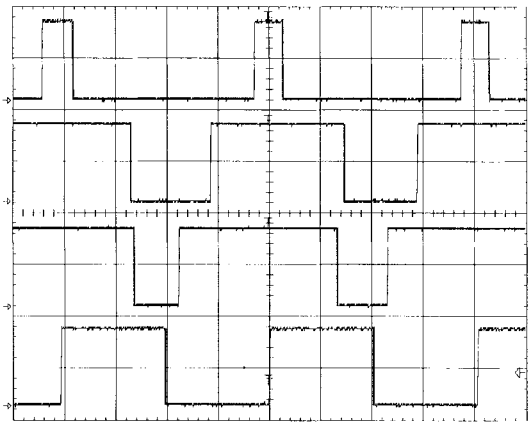

Fig. 22. Experimental phase pulses synchronization with feedforward. Top to bottom: phase 1 voltage u_1 (200 V/div, 50 μs/div), phase 2 voltage u_2 (200 V/div), phase 3 voltage u_3 (200 V/div), and clock (10 V/div).

voltage $u_n = 0.8$. In Fig. 18, a detail of a transient in the same conditions is shown, demonstrating the good transient recovery typical of the hysteresis controls.

In Fig. 19, the combined action of PLL and feedforward is shown, demonstrating that the feedforward gives almost the entire value of the total band β.

In Fig. 20, the effects of the feedforward action on the total ripple δ, due to the "centering" action on the phase pulses, is illustrated. The results can be compared with the ripple given by a control with the PLL alone.

In Figs. 21 and 22, the centering effect is directly proven. The voltage pulses of the three phases are shown, together with the clock signal synchronizing the phase PLL's (on its rising edge).

VI. Conclusion

An improved hysteresis current control technique for a VSI was proposed in this paper, which ensures good control of the position of voltage modulation pulses of the phase output voltages. This allows it to approach the optimal condition of "pulse centering," which characterizes the classic three-phase voltage vector control, resulting in a minimization of the current ripple.

The method is an improvement of a constant-frequency hysteresis control method already developed and applied in [11]. It can be implemented by a very simple scheme and inexpensive components. Due to its simplicity, self-adjusting capability, and robust performance, the method is suitable to an integrated implementation, by means of hybrid or application-specific integrated circuit (ASIC) units.

The technique offers all the advantages of the hysteresis controls in terms of accuracy, robustness, transient response, and bandwidth.

The proposed method was implemented and tested, demonstrating a reliable and high quality performance.

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References

[1] E. Gaio, R. Piovan, and L. Malesani, "Evaluation of current control methods for voltage source inverters," in *Conf. Rec. ICEM'88*, Pisa, Italy, 1988, pp. 345–350.
[2] J. Holtz, "Pulsewidth modulation—A survey," in *Conf. Rec. IEEE PESC'92*, Toledo, OH, 1992, pp. 11–18.
[3] M. P. Kazmierkowski and M. A. Dzieniakowski, "Review of current regulation methods for VS-PWM inverters," in *Proc. IEEE Int. Symp. Industrial Electronics*, Budapest, Hungary, June 1993, pp. 448–456.
[4] L. Malesani and P. Tomasin, "PWM current control techniques of voltage source converters—A survey," in *Conf. Rec. IEEE IECON'93*, Maui, HI, 1993, pp. 670–675.
[5] J. W. Dixon, S. Tepper, and L. Moran, "Analysis and evaluation of different modulation techniques for active power filters," in *Conf. Rec. IEEE APEC'94*, Orlando, FL, Feb. 13–17, 1994, pp. 894–900.
[6] A. Kawamura and K. Ishihara, "High frequency deadbeat control of three phase PWM inverter used for uninterruptible power supply," in *Conf. Rec. IEEE PESC'88*, 1988, pp. 644–649.
[7] M. Marchesoni, "High performance current control techniques for applications to multilevel high power voltage source inverters," in *Conf. Rec. IEEE PESC'89*, Milwaukee, WI, June 1989, pp. 672–682.
[8] T. G. Habetler, "A space vector based rectifier regulator for AC/DC/AC converters," in *Proc. EPE'91 Europ. Conf. Power Electronics and Applications*, Florence, Italy, Sept. 1991, pp. 2.101–2.107.
[9] H. Le-Huy, K. Slimani, and P. Viarouge, "A predictive current controller for synchronous servo drives," presented at the EPE'91 Europ. Conf. Power Electronics and Applications, Florence, Italy, Sept. 1991.
[10] D. C. Lee, S. K. Sul, and M. H. Park, "High performance current regulator for a field oriented controller," in *Conf. Rec. IEEE/IAS 1992 Annu. Meeting*, Houston, TX, Oct. 1992, pp. 538–544.
[11] L. Malesani and P. Tenti, "A novel hysteresis control method for current controlled VSI PWM inverters with constant modulation frequency," *IEEE Trans. Ind. Applicat.*, vol. 26, pp. 88–92, Jan./Feb. 1990.
[12] A. V. Anunciada and M. M. Silva, "A new current mode control process and applications," in *Conf. Rec. IEEE PESC'89*, 1989, pp. 683–694.
[13] J. A. Dente and J. Esteves, "Improved hysteresis controlled inverter for a three phase brushless servo motor," in *Conf. Rec. EPE'89*, Aachen, Germany, Oct. 1989, pp. 257–260.
[14] B. K. Bose, "An adaptive hysteresis-band current control technique of a voltage-fed PWM inverter for machine drive system," *IEEE Trans. Ind. Electron.*, vol. 37, pp. 402–408, Oct. 1990.
[15] L. Malesani, P. Tenti, E. Gaio, and R. Piovan, "Improved current control technique of VSI PWM inverters with constant modulation frequency and extended voltage range," *IEEE Trans. Ind. Applicat.*, vol. 27, pp. 365–369, Mar./Apr. 1991.
[16] K. Tungpimolrut, M. Matsui, and T. Fukao, "A simple limit cycle suppression scheme for hysteresis current controlled PWM-VSI with consideration of switching delay time," in *Conf. Rec. IEEE/IAS 1992 Annu. Meeting*, Houston, TX, Oct. 1992, pp. 1034–1041.

[17] R. B. Sepe, Jr., "A unified approach to hysteretic and ramp-comparison current controllers," in *Conf. Rec. IEEE/IAS 1993 Annu. Meeting*, Toronto, Ont., Canada, Oct. 2–8, 1993, pp. 724–731.
[18] Q. Yao and D. G. Holmes, "A simple, novel method for variable-hysteresis-band current control of a three phase inverter with constant switching frequency," in *Conf. Rec. IEEE IAS'93*, Toronto, Ont., Canada, Oct. 1993, pp. 1122–1129.
[19] M. P. Kazmierkowski, M. A. Dzieniakowski, and W. Sulkowski, "Novel space vector based current controllers for PWM-inverters," in *Conf. Rec. IEEE/PESC'89*, Milwaukee, WI, June 1989, pp. 657–664.
[20] L. Malesani, L. Rossetto, L. Sonaglioni, P. Tomasin, and A. Zuccato, "Digital, adaptive hysteresis current control with clocked commutations and wide operating range," in *Conf. Rec. IEEE IAS'94*, Denver, CO, Oct. 1994, pp. 1115–1121.
[21] H. W. Van Der Broek, H. C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. Ind. Applicat.*, vol. 24, pp. 142–150, Jan./Feb. 1988.
[22] C. Chiarelli, L. Malesani, S. Pirondini, and P. Tomasin, "Single-phase, three-level, constant frequency current hysteresis control for UPS applications," in *Proc. EPE'93 Europ. Conf. Power Electronics and Applications*, Brighton, U.K., Sept. 1993, pp. 180–185.
[23] T. M. Rowan and R. J. Kerkman, "A new synchronous current regulator and an analysis of current regulated PWM inverters," in *Conf. Rec. IEEE IAS'85*, pp. 487–495.

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