Improved DFT for Testing Power Switches

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Abstract—**Power switches are used as part of power-gating technique to reduce leakage power of a design. To the best of our knowledge this is the first study that analyzes recently proposed DFT solutions for testing power switches through SPICE simulations on a number of ISCAS benchmarks and presents the following contributions. It provides evidence of long discharge time when power switches are turned-off, when testing power switches using available DFT solutions. This may either lead to false test (false-fail or false-pass) or long test time. This problem is addressed through a simple and effective DFT solution to reduce the discharge time. The proposed DFT solution has been validated through SPICE simulation and shows an improvement in discharge time of at least 28-times, based on a number of ISCAS benchmarks synthesized with a 90-nm gate library.**

Index Terms—**Sleep transistor, power switch, leakage power management, test time overhead, DFT, design for test.**

I. INTRODUCTION

Power gating is a low-power design technique to reduce leakage power. It has gained popularity in sub 100-nm CMOS designs, where leakage power is a major contributor to the overall power consumption [1]. It utilizes power-switches (also called sleep transistors) to power-down the logic blocks during idle mode to reduce leakage power consumption [2]. Power switches are implemented as header switches or footer switches. This paper analyzes headers in detail but the results are equally applicable to footers. Power switches are usually implemented in either "fine grain" or "coarse-grain" design styles. Fine-grain style incorporates a power-switch within each standard logic cell with a control signal to switch on/off the power supply of the cell. In coarse-grain design style, a number of power-switches are combined to feed a block of logic. When comparing the two design styles, fine-grain design simplifies the incorporation of power-gating through existing EDA tools, but it has higher area overhead and it is more vulnerable to voltage drop fluctuations due to process, voltage and temperature variations [2]. Therefore coarse-grain design style is a more popular design choice in practice and is the focus of this work.

Recent research has reported a number of DFT solutions to test power-switches when considering the two possible type of faults: stuck-open and stuck-short [3], [4]. The first DFT solution is reported in [3], and is used to test power switches in both fine-grain and coarse-grain designs (Fig. 1). Recently, in [4] the problem of long discharge time (in available DFT

solutions) was highlighted without providing detailed analysis and implication on test quality. The first aim of this paper is to provide detailed analysis of available power gating DFT solutions and the second aim is to propose a simple and effective DFT solution (together with test vectors) for testing power switches to reduce the discharge time when they are turned-off.

The paper is organized as follows: Section II presents the shortcomings of available DFT methods for testing power switches leading to long test time. These shortcomings can be addressed by modifying the available DFT and associated test vectors, as discussed in Section III. Experimental results are reported in Section IV, and finally Section V concludes the paper.

II. ANALYSIS OF AVAILABLE DFT SOLUTIONS

In this section, we first analyze the imbalance in charging and discharging time of a power switch using HSPICE simulation, and then using a coarse-grain design, we demonstrate how it may either lead to false test (wrong identification of a switch as faulty or non-faulty) or long test time.

To quantize the charge (rise) and discharge (fall) time of a power switch, we constructed a test circuit (Fig. 1a) for testing a power-switch. The DFT of the circuit consists of a control register for controlling the test sequence, a multiplexer to enable the test mode, an AND gate and a comparator to detect a fault. The logic block in this example test circuit consists of five gates (two, 2-input NAND; two, 2-Input NOR and an inverter) from a 90-nm standard V_{th} CMOS gate library. The power switch used for this purpose is a high V_{th} PMOS transistor. IR-drop target of $\leq$ 5% [5] is achieved by using a power-switch with width of 1.1 μm and length of 150-nm. The logic block is powered by the virtual supply (V_{Vdd}) and operating V_{dd} is 1-V. The signal "TE" (Test Enable) is set to 1 (Fig. 1a) and the power switch is first turned-on (Test=0). The charge time is defined as the time it takes the voltage level to reach 90% of V_{dd} and at that point the power switch is switched-off (Test=1) to observe the discharge time. The discharge time is the time it takes the voltage level to reach 10% of V_{dd}. Through this experiment, it was found that the discharge time is significantly higher (5,068-times) than the charge time at room temperature (25 °C; first row of Table I).
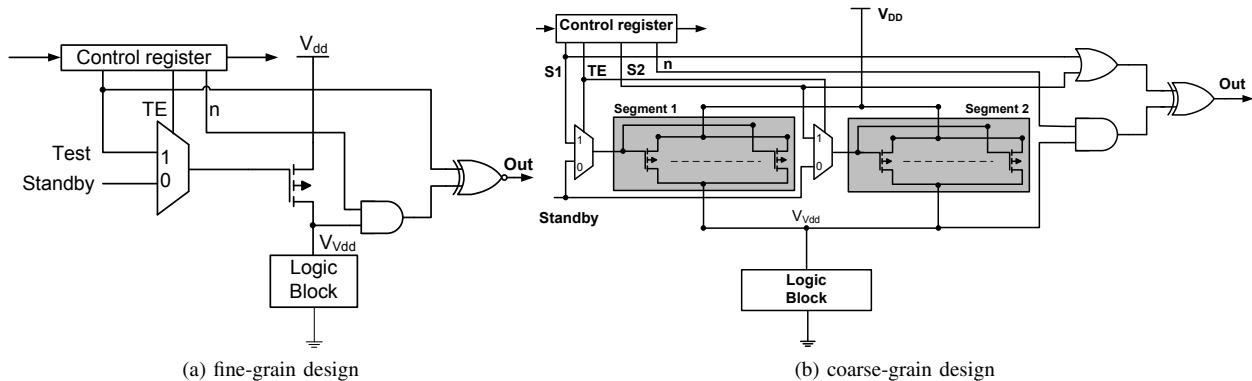
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(a) fine-grain design   (b) coarse-grain design

Fig. 1: DFT for testing power-switches [3]

TABLE I: The rise and fall delay at the V_{Vdd}

Temp.	V_{Vdd} discharge	V_{Vdd} charge	$\frac{discharge}{charge}$
°C	time (ns)		
25	1,723	0.34	5,068
50	699	0.36	1,942
75	320	0.37	865
100	164	0.38	432
125	91	0.39	233

TABLE II: Test vectors for two segment power switch [3]

	TE=1		Out	
Cycle	S1	S2	Fault free	Faulty
1	0	1	0	1
2	1	0	0	1
3	1	1	1	0

Temperature varies during test due to switching activity of the logic block and it also affects the leakage current of the logic block. To observe this effect on charge and discharge time of the power switch, temperature is varied from 25 °C to 125 °C in five discrete steps. The results are shown in Table I. As can be seen the discharge time is 1,723-ns at room temperature and it reduces to 91-ns as temperature increases to 125 °C. This is because of the sub-threshold leakage current of a CMOS transistor and it occurs when the gate voltage is below V_{th}. This current is proportional to the square of the thermal voltage ($\frac{KT}{Q}$; where T is temperature) [1]. As temperature increases the leakage of the logic block increases resulting in reduced discharge time. The last column of Table I shows the ratio between discharge time and charge time. The discharge time is 5,068 times higher than the charge time at 25 °C, and it reduces to 233 at 125 °C. These results (Table I) clearly demonstrate the imbalance in charge and discharge time of the power switch, as implemented in available DFT methods.

Next we demonstrate using a power-gating coarse-grain design how this imbalance may either lead to a false test or long test time. In coarse-grain designs, power switches are divided into segments to collectively test a number of power switches (Fig. 1b). The number of power switches per segment has a trade-off between area overhead and precision in identifying faulty transistors, see [3] for more details. The design shown in Fig. 1b with 2 segments is tested using three test vectors (Table II), where the first two test vectors are used to test transistors in segment 1 and segment 2 for stuck-open fault respectively. The third test vector is used to test stuck-short fault at either of the two segments with V_{dd}. We analyzed the effect on test time through HSPICE simulation using these test vectors on the design shown in Fig. 1b. In this setup, the logic block consists of ten gates (four, 2-input NAND; four, 2-input NOR and two inverters) and single power switch per segment to achieve targeted IR-drop of $\leq$ 5%. For this experiment, we inserted a stuck-open fault in segment 2 transistor, which is tested using the second test vector (Table II). Due to faulty transistor in segment 2, the logic value at the output of comparator "Out" should be "1". The SPICE simulation results are shown in Fig. 2, as can be seen, identifying correct state of the switch requires sufficient waiting time. In this experiment, it takes more than 700-ns (1.2-μs$-$0.5-μs) to observe the correct logic value (Out=1) at "Out". On the other hand sampling the data earlier will result in false test (Out=0) i.e., identifying a faulty power switch as fault-free. Therefore to permit sufficient discharge time the test clock frequency must be less than 1.4 MHz ($\frac{1}{700\times10^{-9}}$; as in this example) to avoid false test (false-fail or false-pass).

From test cost point of view, it is desirable to save test time, however in this case the test clock frequency is limited by the discharge time of the power switch. To use a higher test clock frequency, a simple and effective solution is using an NMOS transistor, referred as *discharge transistor*, between the virtual supply (V_{Vdd}) and ground, to quickly discharge the voltage at V_{Vdd} after the power switch is turned-off. In practice, it is also difficult to estimate the discharge time accurately as it varies across logic blocks. Designing discharge transistor also allows accurate quantization of discharge time leading to not only higher test clock frequency but it also eliminates the possibility of false test (see Sec. IV-A for more details).
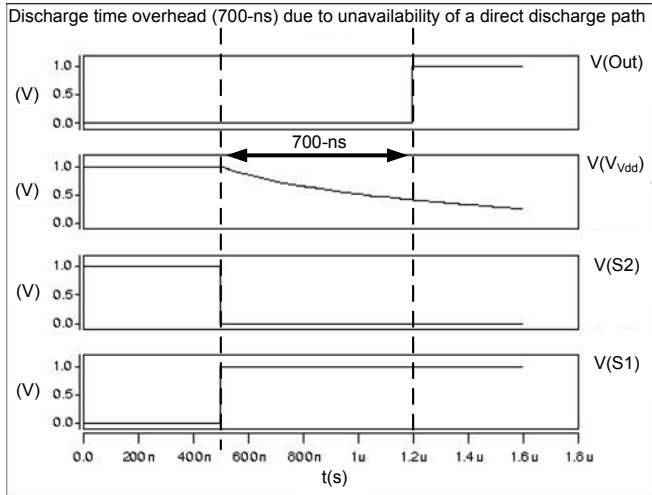
Fig. 2: HSPICE simulation results using DFT for coarse-grain design of power-switches (Fig. 1b)
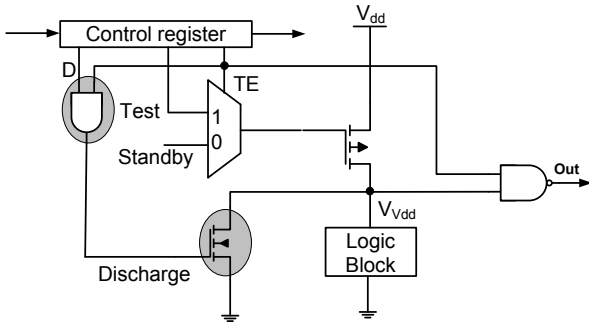

Fig. 3: Proposed DFT using discharge transistor

Fig. 4: $\frac{I_{Discharge}}{I_{Off}}$ for a high V_{th} NMOS transistor

III. PROPOSED DFT FOR TESTING POWER SWITCHES

Fig. 3 shows the proposed DFT for testing power switches, it requires discharge transistor and AND gate to improve the available DFT. The discharge transistor is enabled during test mode through TE (Test Enable) signal. During test the discharge transistor is controlled through the signal D, which is an additional bit in the control register. In this section, we first describe the details of designing an efficient discharge transistor to ensure a balanced charge/discharge time at V_{Vdd}. This is followed by a discussion on test vectors needed for testing power switches using the proposed DFT.

A. High Efficiency Discharge Transistor Design

A proper discharge transistor design is important not only for balanced charge/discharge time but it also affects the performance during normal operation (active mode or sleep mode) of the design. The discharge transistor is switched-off during normal operation of the design and therefore high performance and leaky (low V_{th} or standard V_{th}) transistors are unnecessary. This is why a high V_{th} (low performance and less leaky) NMOS transistor is a better choice to be used as a discharge transistor.
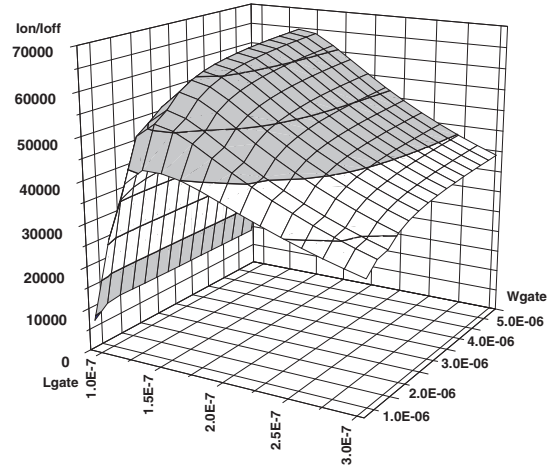
As an example, consider the design shown in Fig. 3. A balanced charge/discharge time at V_{Vdd} is dependent on the power switch and the logic block. The power switch used through out this paper has gate length of 150-nm and width of 1.1-μm. The logic block consists of five logic gates (two, 2-input NAND; two, 2-input NOR and an inverter). A methodology for high efficiency power switch design is discussed in [2], and used in this work to design the discharge transistor. The discharge transistor is designed to achieve high efficiency i.e., high (I_{On}) when transistor is switched-on, referred as $I_{Discharge}$, and low leakage current (I_{Off}) when the transistor is switched-off. The efficiency ($\frac{I_{Discharge}}{I_{Off}}$) of a high V_{th} transistor is simulated through HSPICE. We performed two simulations each with a high V_{th} NMOS transistor to simulate $I_{Discharge}$ and I_{Off}. For $I_{Discharge}$ simulation, V_{ds} of the transistor is set to 10-mV for $< 5\%$ IR-drop target when operating at 1-V V_{dd}, and for illustration the temperature is set to 125 °C to model the operating mode. For I_{Off} simulation, V_{ds} is set to V_{dd} and the temperature is set to 25 °C to model the sleep mode.

The discharge transistor is designed in two steps. Firstly, transistor length is determined by sweeping the NMOS transistor width from 0.2-μm to 5-μm with increment of 5-nm; and this is repeated for a range of transistor lengths, from 90-nm to 300-nm with increment of 5-nm. The efficiency curve $\frac{I_{Discharge}}{I_{Off}}$ is shown in Fig. 4. As can be seen, the highest efficiency is achieved at the gate length of 150-nm. Secondly, at this gate length (L_g=150-nm), the transistor gate width is varied to achieve balanced charge/discharge time at V_{Vdd}. The power switch is turned-on to simulate the charge time and then it is switched-off to simulate the discharge time. Fig. 5 shows the simulation result, as can be seen the discharge transistor with the width of about 0.48-μm show a balanced charge and discharge time at V_{Vdd}. Therefore, high V_{th} NMOS
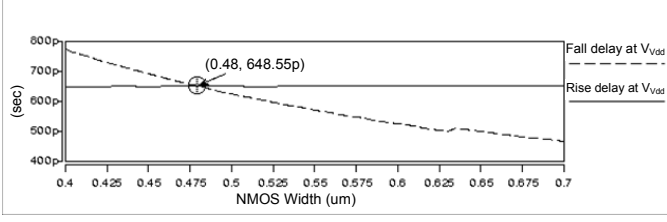
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Fig. 5: Gate width selection of discharge transistor for balanced rise and fall time at V_{Vdd}
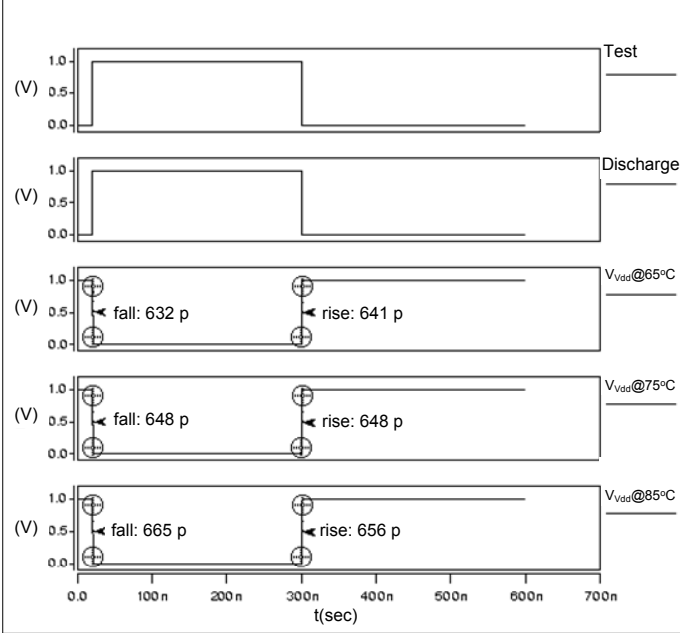

Fig. 6: Rise and fall time at V_{Vdd} at different temperatures

transistor with L_g of 150-nm and W_g of 0.48-μm is suitable as a discharge transistor for the design shown in Fig. 3 with a logic block of five gates. We also analyzed the effect of temperature variation on charge/discharge time at V_{Vdd}, where the temperature is varied from 25 °C to 125 °C in five discrete steps. Fig. 6 shows the simulation results at three temperature settings showing the difference in charge/discharge time is less than 10-ps (representing $< \pm 5\%$ difference).

The proposed DFT fits well in the standard EDA power gating design flow. Fig. 7 shows the proposed DFT flow including the insertion of the discharge transistors. The power switch is usually placed after floor planning, followed by logic cell placement, clock tree synthesis and routing. Power switches are optimized next to ensure IR-drop target in every part of the design. This is followed by discharge transistor placement (highlighted with grey box) because it allows optimized performance of the design by giving priority to standard cell placement, clock tree synthesis and routing. Once the final IR-drop and power switch network are fixed, we have sufficient information to place the discharge transistors while ensuring balanced charge and discharge time. This is followed by Power Rail optimization, which is usually the last step in
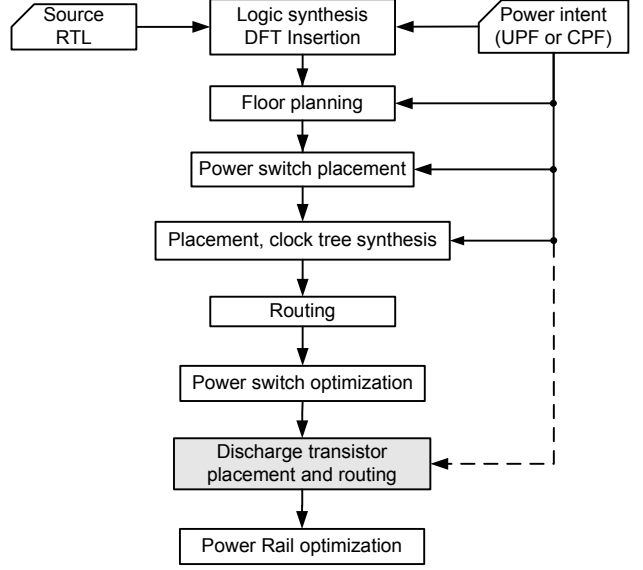

Fig. 7: DFT flow for testing power switches

power-gating design flow.

B. Test set for power gated design

For the proposed DFT, it is necessary to test the discharge transistors and the power switches for two possible faults: stuck-open and stuck-short. This is because a stuck-open fault (transistor drain-source open) in a discharge transistor will result in long discharge time of the power switch leading to a false test, while a stuck-short fault (transistor drain-source short) will lead to a stuck-at 0 fault at V_{Vdd}. It was shown in [3], [4] that for testing power switches in coarse-grain design, power switches are divided into m segments, where each segment contains n power switches. Each segment is tested separately for stuck-open and stuck-short faults. The number of segments m and transistors per segment n exhibit a trade-off between test time and test quality. Larger value of m will require large number of test cycles for testing all power switches, but it improves test quality by isolating faulty power switches from the rest of fault-free switches.

Fig. 8 shows the proposed DFT for coarse-grain power switches with m segments. Power switches per segment are tested together and usually a single segment is activated during test [4]. The discharge transistors are designed to achieve a balanced charge/discharge time at V_{Vdd}, assuming a single active power switch segment. Sec. IV-A discusses the implementation details of coarse-grain design using a number of ISCAS benchmarks.

Table IV shows the test vectors to test a design using the DFT shown in Fig. 8 and assuming two segments $m = 2$. The first test cycle turns-off both power switch segments (Segment 1 and Segment 2) and turns-on the discharge transistors to quickly discharge the voltage at V_{Vdd}. The second test cycle turns-off the discharge transistors to test for stuck-short at
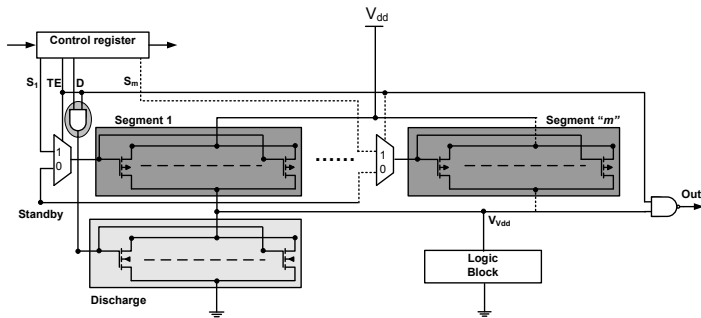
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Fig. 8: Proposed DFT for testing coarse grain power-switches

TABLE IV: Test patterns for testing power-switches and discharge transistors using the proposed DFT (Fig. 8) assuming two segments $m = 2$

Test	$TE = 1$				Out		
cycle	S_1	S_2	D	V_{Vdd}	Fault free	Faulty	Justification
1.	1	1	1	0	1	0	Discharge
2.	1	1	0	0	1	0	Seg. 1 Short Seg. 2 Short
3.	0	1	0	1	0	1	Seg. 1 Open *DT Short
4.	1	1	1	0	1	0	Discharge DT Open
5.	1	0	0	1	0	1	Seg. 2 Open DT Short

*DT $\rightarrow$ Discharge Transistor

either of the two power switch segments. The third test cycle turns-on all power switches in segment 1 while power switches in segment 2 and discharge transistors are switched-off. This charges up the virtual supply node (V_{Vdd}) through power switches in segment 1 and is used to test stuck-open on transistors of segment 1 and stuck-short on discharge transistors. The fourth test cycle turns-off both power switch segments and turns-on the discharge transistors to discharge the voltage at V_{Vdd} that was charged up in the previous test cycle. This test cycle is also used to test stuck-open fault on the discharge transistors. The last test cycle is used to test stuck-open on power switches in segment 2 by turning off power switches in segment 1 and discharge transistors. In general, $''(2 * m) + 1''$ test cycles are needed to test a design with m power switch segments and a discharge segment using the proposed DFT (Fig. 8). For designs with $m \geq 2$ power switch segments, fourth test cycle (Table IV) should be repeated after applying stuck-open test at each segment other than the last segment, to discharge the voltage at V_{Vdd} and to prepare for the next test cycle.

IV. EXPERIMENTAL RESULTS

To demonstrate the improvement in test time using the proposed DFT, we conducted an experiment using coarse-grain power gating designs. The designs are synthesized using 90-nm STMicroelectronics gate library and the netlist is converted to SPICE format using Synopsys STAR-RCXT. The operating voltage is 1-V and IR-drop of 5% or less is targeted for all designs. IR-drop is determined in active mode by simulating the voltage at V_{Vdd}, while feeding transition pulses (high-to-low and low-to-high) to the primary inputs of each design.

A. Coarse-grain power gating designs

Table III lists some of the ISCAS benchmarks used for this experiment. The total number of power switches per design needed to achieve the targeted IR-drop of $\leq 5\%$ is shown in the second column. As expected, the number of power-switches increase with the size of design. For 90-nm STMicroelectronics gate library used in this work, the ratio of power-switches to logic cells is on average approximately 1:5 for many different ISCAS benchmarks and due to space limitation we are showing results only for five benchmarks. The power switches are

divided into a number of segments and the number of discharge transistors are chosen to achieve a balanced charge/discharge time at the V_{Vdd} when only transistors of one segment are turned on. We also validated the charge/discharge time across a range of temperature settings (25 °C to 125 °C in five steps) and the worst-case difference is within $\pm 5\%$ of rise and fall time at the V_{Vdd}, see Sec. III-A for more details. Since the voltage at V_{Vdd} and the rise/fall time at V_{Vdd} is related to the number of transistors switched on at a given time, we assumed three segment sizes "m" per design (5, 15, 25), referred as design configuration. For each of the three design configurations, the number of power switches per segment are shown in the third column, followed by the number of discharge transistors per design configuration in the fourth column. The width of each of the discharge transistors is shown in the fifth column, and as discussed in Sec. III-A, the length of each discharge transistor is kept at 150-nm but the width is varied to achieve a balanced charge/discharge time at V_{Vdd}. The charge time at V_{Vdd} with (proposed) and without discharge transistors (using [3]) is shown in the columns marked as "Charge Time". As expected, the charge time reduces with higher number of power switches per segment and is approximately the same with and without discharge transistors. For example, in case of C432 as the number of power switches per segment increases from 5 to 25, the charge time reduces from 1.5-ns to 0.35-ns. The next column marked as "Discharge Time" show the difference in discharge time at V_{Vdd} using the two (proposed and [3]) DFT methods. As can be seen, there is significant reduction in discharge time using the proposed DFT method. On average, over all designs the reduction in discharge time is more than 346-times; in the best case the reduction is more than 1496-times (third row of C432) and the least reduction is more than 28-times (first row of C3540) in comparison to a design without discharge transistors. As discussed in Sec. II the discharge time has a direct effect on test clock frequency and in case of designs without discharge transistors, the test clock frequency is limited by the discharge time of the power switch. The last two columns of Table III marked as "Max.

TABLE III: Relative improvement in testing coarse-grain power-switches

| Design | Total # of PS* | Segment Size | | DT | Charge Time (ns) | | Discharge Time (ns) | | Max. Test Freq. (MHz) | |
		# of PS	# of DT	Width (μm)	Proposed	[3]	Proposed	[3]	Proposed	[3]
C432	30	5	5	0.35	1.5	1.5	1.5	507.4	666	1.9
		15	15	0.3	0.57	0.57	0.56	513.9	1754	1.9
		25	25	0.29	0.35	0.35	0.35	523.9	2857	1.9
C1908	120	5	5	0.36	3.3	3.3	3.3	422.8	303	2.4
		15	15	0.305	1.3	1.3	1.3	424.5	769	2.4
		25	25	0.28	0.8	0.8	0.8	427.4	1250	2.3
C2670	180	5	5	0.42	4.1	4.1	4.1	484	244	2.1
		15	15	0.375	1.5	1.5	1.5	484.6	667	2.1
		25	25	0.35	0.95	0.95	0.95	486.7	1053	2
C3540	200	5	5	0.325	7.6	7.6	7.6	215.9	132	4.6
		15	15	0.31	2.9	2.9	2.9	210	345	4.8
		25	25	0.32	1.7	1.7	1.7	209	588	4.8
C7552	700	5	5	0.36	12.46	12.6	12.4	423.3	80	2.4
		15	15	0.35	4.4	4.4	4.4	425.7	227	2.3
		25	25	0.32	2.8	2.8	2.8	427.3	357	2.3

PS* $\rightarrow$ Power Switches, DT $\rightarrow$ Discharge Transistors

TABLE V: Test time saving using the proposed DFT solution

| Total Seg. (m) | Test Time (s) | | Test Time saving (hrs) |
	$m + 1$ [3] Freq=2 MHz	$2 * m + 1$ Freq=650 MHz	Per Million
1.E+04	5.0E-03	3.08E-05	1.38
5.E+04	2.5E-02	1.54E-04	6.9
1.E+05	5.0E-02	3.08E-04	13.8
5.E+05	2.5E-01	1.54E-03	69
1.E+06	5.0E-01	3.08E-03	138
2.E+06	1.0E+00	6.15E-03	276
1.E+07	5.0E+00	3.08E-02	1,380

Test Freq." can be used to compare the maximum possible test frequencies with and without using the proposed DFT.

Using a representative test clock frequency for each of the two DFT methods, Table V shows an approximation of test time saving, in terms of number of hours saved per million tested devices, through the proposed DFT method. We assume 2 MHz as representative test clock frequency for a design using available DFT method [3] and 650 MHz for a design employing the proposed DFT method. Test time per device also depends on total number of segments "m" and total number of test clock cycles needed for testing power switches. The total number of test clock cycles are "$m + 1$" for the available DFT method [3] and "$(2 * m) + 1$" for the proposed DFT method. The first column of Table V shows different number of segments per design, the next column shows the test time for testing each device using the two DFT methods (in [3] and proposed) and the last column shows the total test time saving (hours/million tested devices) through the proposed DFT method. It can be observed that test time savings increase with the number of segments. For example, test time saving (per Million tested devices) for a design with 10,000 segments is 1.38 hours and it increases to 13.8 hours for testing a design with 100,000 segments.

V. CONCLUSION

This work has demonstrated that recently proposed DFT methods for testing power switches have long discharge time when the power switch is turned-off. This leads to long test time due to the necessity of applying slower test clock and may lead to false test (false-fail or false-pass). The proposed DFT achieves fast test time through balanced charge and discharge time and eliminates the possibility of false test. Experiments are conducted using a 90-nm gate library and ISCAS benchmarks that show the reduction in discharge time, which is at least 28-times by using the proposed DFT.

ACKNOWLEDGMENTS

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