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Published on: 20 Oct 2016 - IEEE Microwave and Wireless Components Letters (IEEE)

Topics: Doherty amplifier, RF power amplifier, Amplifier, Impedance matching and Wideband

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Authors(s)	Xia, Jing; Yang, Mengsu; Zhu, Anding
Publication date	2016-10-20
Publication information	IEEE Microwave and Wireless Components Letters, 26 (11): 915-917
Publisher	IEEE
Item record/more information	http://hdl.handle.net/10197/8400
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Publisher's version (DOI)	10.1109/LMWC.2016.2615004

Improved Doherty Amplifier Design with Minimum Phase Delay in Output Matching Network for Wideband Application

Jing Xia, *Member*, *IEEE*, Mengsu Yang, and Anding Zhu, *Senior Member*, *IEEE*

***Abstract*—This paper presents an improved Doherty power amplifier (DPA) for high-efficiency and wideband operations. To achieve the impedance transformations both in the low power region and at saturation, a design approach is proposed to determine the desired minimum phase delays of the carrier and peaking output matching networks, which can simplify the load modulation network of the DPA and extend the bandwidth. For verification, a 1.6–2.2 GHz asymmetric DPA was designed and measured. The designed DPA can deliver an efficiency of 51%–55% at 10 dB back-off power over the whole band. For a 20 MHz LTE signal, an average efficiency of higher than 50% can be achieved at 36 dBm average output power with the linearity of –48 dBc after linearization across the band.**

***Index Terms*—Back-off, Doherty, high efficiency, output matching network, power amplifiers, wideband.**

I. Introduction

TO EFFICIENTLY amplify modulated signals with high peak-to-average power ratios (PAPRs), Doherty power amplifiers (DPAs) have been widely used to achieve high efficiency at large back-off output power [1]-[5]. Conventional output matching networks (OMNs) used in DPAs often have complicated topologies that can introduce large phase delays and these phase delays vary over frequencies which cause performance degradation in wideband operation. To minimize the phase delay dispersion and maintain wideband performance, an OMN with compact topology and small phase delay is desired in wideband DPA design. Recently, a post-matching wideband DPA was proposed in [4]. This method extended the bandwidth effectively by using a low-order impedance inverter, but it particularly requires the real part of the carrier load impedance to be invariant at both low power and saturation.

Manuscript received July 02, 2016; accepted July 21, 2016. This work was supported in part by the Natural Science Foundation of Jiangsu Province of China under Grant No. BK20150528 and the Natural Science Foundation of the Jiangsu Higher Education Institutions of China under Grant No. 15KJB510007, and by the Science Foundation Ireland under Grant No. 13/RC/2077 and 12/IA/1267.

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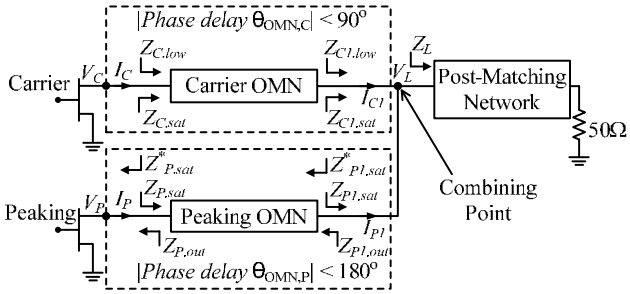

Fig. 1. Simplified circuit diagram of the proposed DPA.

In this paper, to achieve wideband load modulation, unlike the method in [4], a more general OMN design method is proposed. The relationships between the load impedances of the OMNs are deduced first to determine the desired minimum phase delays of the OMNs, according to the requirement of the load modulation. Compact OMNs with minimum phase delays are then designed to enhance wideband performance without using $\lambda_0/4$ transformer or offset lines. For validation, a 1.6–2.2 GHz asymmetric DPA with higher than 50% efficiency at 10 dB output-back-off (OBO) power was designed and measured.

II. Proposed OMN Design for Wideband DPA

The simplified circuit diagram of the proposed DPA is shown in Fig. 1, where $Z_{C1,sat}$, $Z_{C,sat}$, $Z_{P1,sat}$ and $Z_{P,sat}$ represent the load impedances, at the combining point and at the device output, of the carrier and peaking amplifiers at saturation while $Z_{C1,low}$, $Z_{C,low}$, $Z_{P1,out}$ and $Z_{P,out}$ are the load and output impedances at low power (back-off) region, respectively. The design procedure of the OMNs with minimum phase delay is presented as follows.

A. Calculation of minimum phase delays of the OMNs

In Doherty operation, the OMNs are used to convert the load impedances to the desired values to obtain enhanced efficiency. As shown in Fig. 1, the carrier OMN should convert $Z_{C1,low}$ to $Z_{C,low}$ when the amplifier is at low power region and convert $Z_{C1,sat}$ to $Z_{C,sat}$ when the amplifier is in saturation. Similarly, the peaking OMN should transform the impedance $Z_{P,out}$ to the open-circuited impedance $Z_{P1,out}$, at low power region, and convert $Z_{P1,sat}$ to $Z_{P,sat}$ at saturation. Ideally the impedance transformations mentioned above can be achieved by using a $\lambda_0/4$ impedance inverter and a $\lambda_0/2$ transmission line, but in

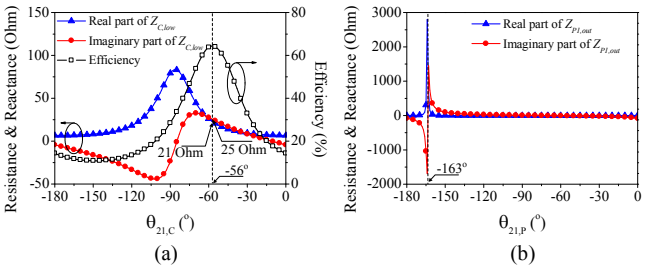

Fig. 2. Graphical illustration of the calculation of the minimum phase delay at the frequency of 1.9 GHz. (a) Carrier OMN. (b) Peaking OMN.

practice, directly employing these transmission lines cannot achieve the best performance because the desired phase delays of the carrier and peaking OMNs may not be exactly 90° and 180°, respectively, due to the effects of device package.

If we re-look at the Doherty architecture and use network analysis, we actually can design the OMNs in a different way. In Fig. 1, because the S parameters of a lossless reciprocal OMN can be determined by two parameters, i.e., S_{11} and the phase of S_{21} (θ_{21}) [6], the $ABCD$ parameters can also be expressed in terms of S_{11} and θ_{21}. To design the carrier OMN, the following equations can be obtained:

$$\begin{bmatrix} V_C \\ I_C \end{bmatrix} = \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} V_L \\ I_{C1} \end{bmatrix} = \begin{bmatrix} \dfrac{a+c}{2\sqrt{c}} & Z_0\dfrac{b-c}{2\sqrt{c}} \\ \dfrac{1}{Z_0}\dfrac{d-c}{2\sqrt{c}} & \dfrac{e+c}{2\sqrt{c}} \end{bmatrix} \begin{bmatrix} V_L \\ I_{C1} \end{bmatrix} \quad (1)$$

where Z_0 is the reference impedance, and

$$a = (1+S_{11})(1+S_{11}^* e^{j2\theta_{21}}) \qquad b = (1+S_{11})(1-S_{11}^* e^{j2\theta_{21}})$$
$$c = (1-|S_{11}|^2)e^{j2\theta_{21}} \qquad d = (1-S_{11})(1+S_{11}^* e^{j2\theta_{21}})$$
$$e = (1-S_{11})(1-S_{11}^* e^{j2\theta_{21}})$$

From (1), considering V_C=$I_C Z_C$ and V_L=$I_{C1} Z_{C1}$, the effective load impedances of the carrier device, at saturation and in the low power region, can be written as

$$Z_{C,sat} = \frac{Z_{C1,sat}A_C + B_C}{Z_{C1,sat}C_C + D_C} = \frac{Z_0 Z_{C1,sat}a + Z_0^2 b + Z_0(Z_{C1,sat} - Z_0)c}{Z_{C1,sat}d + Z_0 e + (Z_0 - Z_{C1,sat})c} \quad (2)$$

$$Z_{C,low} = \frac{Z_{C1,low}A_C + B_C}{Z_{C1,low}C_C + D_C} = \frac{Z_0 Z_{C1,low}a + Z_0^2 b + Z_0(Z_{C1,low} - Z_0)c}{Z_{C1,low}d + Z_0 e + (Z_0 - Z_{C1,low})c} \quad (3)$$

In the design process, the optimum values for the four impedances, i.e., $Z_{C,sat}$, $Z_{C1,sat}$, $Z_{C,low}$ and $Z_{C1,low}$, can be determined by using load-pull measurement or simulation. The design parameters of the carrier OMN (S_{11} and θ_{21}) can then be obtained according to (2) and (3). It should be emphasized that, due to the periodicity of the exponential function, a series of θ_{21} satisfy the above equations. To minimize the phase delay dispersion over the whole frequency band for wideband operation, only the θ_{21} with minimum value should be chosen. Similar design method can also be employed to obtain the design parameters of the peaking OMN.

To illustrate the design procedure, let's take the design of a 1.6–2.2 GHz asymmetric DPA using Cree CGH40010F and CGHV40030F GaN HEMTs as an example. Considering the

TABLE I

DESIGN PARAMETERS OF THE OMNS

	$Z_{C,sat}/Z_{P,sat}$	$Z_{C1,sat}/Z_{P1,sat}$	$S_{11,C}/S_{11,P}$	$\theta_{21,C}/\theta_{21,P}$
Carrier	23.1–j5Ω	60Ω	–0.44–j0.1*	–56°*
Peaking	19.4+j15.4Ω	24Ω	0.018+j0.35**	–163°**

* with reference impedance of 60Ω
** with reference impedance of 24Ω

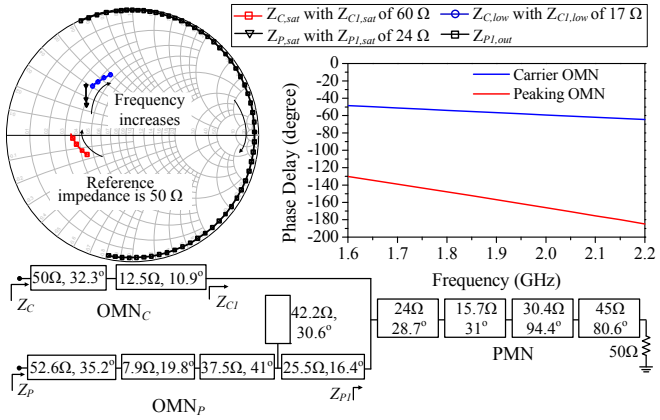

Fig. 3. The designed OMNs of the carrier and peaking amplifiers.

lower class C biasing of the peaking amplifier, the power ratio of the peaking and carrier amplifiers ρ was calculated to be 2.5 according to the load-pull results. To decrease the impedance transformation ratio between the load Z_L and the 50 Ω load, the impedance Z_L was chosen to be 17 Ω. Assuming the current ratio $\delta = \rho$, $Z_{C1,sat}$ = 60 Ω and $Z_{P1,sat}$ = 24 Ω can be calculated [7].

For the carrier OMN design, the load impedance of 23.1–j5 Ω was chosen as $Z_{C,sat}$ by using load pull simulation at the frequency of 1.9 GHz. The reference impedance Z_0 was set to be equal to $Z_{C1,sat}$ (60 Ω) and thus (2) can be simplified to be independent from θ_{21}. From (2), S_{11} of the carrier OMN $S_{11,C}$ can then be calculated to be –0.44–j0.1. Considering $\theta_{21,C}$ as a degree of freedom, a set of carrier effective load impedances $Z_{C,low}$ were calculated by using (3) with $Z_{C1,low}$ of 17 Ω, as shown in Fig. 2(a). To determine the desired $\theta_{21,C}$ for high back-off efficiency, the simulated efficiencies of the carrier amplifier at back-off power (about 37 dBm) with those $Z_{C,low}$ are also depicted. It is shown that the desired $\theta_{21,C}$ can be determined to be –56° with associated $Z_{C,low}$ of 21+j25 Ω. The design parameters of the carrier OMN are shown in Table I.

For the peaking OMN, the output impedance of the device $Z_{P,out}$ in class C operation was calculated to be 0.3–j42 Ω, according to the simulation when the peaking amplifier is in off-state. With the reference impedance of 24 Ω, $Z_{P,sat}$= 19.4+j15.4 Ω and $Z_{P1,sat}$= 24 Ω, by using four impedances ($Z^*_{P1,sat}$, $Z^*_{P,sat}$, $Z_{P1,out}$ and $Z_{P,out}$), similar procedure can also be employed to estimate the phase delay of the peaking OMN ($\theta_{21,P}$) for high output impedance $Z_{P1,out}$, as shown in Fig. 2(b). The calculated parameters are also shown in Table I.

B. Realization and Optimization of the OMNs

After the S_{11} and the minimum θ_{21} of the OMNs are obtained by using the design method in Section II-A, the OMNs can be designed by using stepped-impedance matching network theory and tuned by optimization considering the requirements

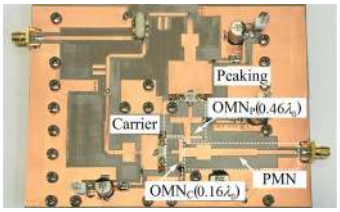

Fig. 4. Photograph of the fabricated DPA.

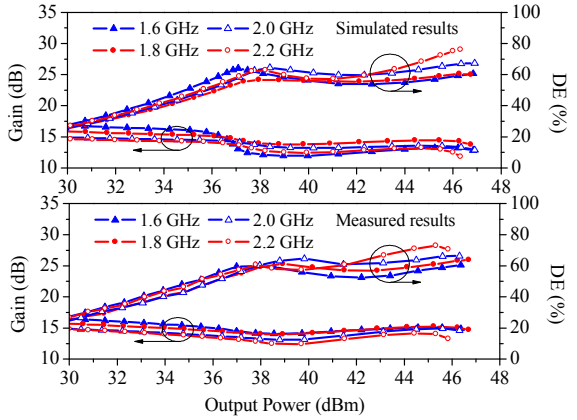

Fig. 5. Simulated and measured DE and gain across the bandwidth.

of load-pull results and the phase delay over the frequency band of 1.6–2.2 GHz, as shown in Fig. 3. For the whole frequency band, the carrier OMN was optimized for high efficiency at both low-power region and saturation, while the peaking OMN was tuned to achieve quasi open-circuited behavior before it turns on. The phase delay dispersions of the two OMNs are minimized. The simulated impedances and phase delays are depicted in Fig. 3. It is shown that, with the proposed method, the compact carrier and peaking OMNs can achieve phase delay dispersions of only 15° and 55° over wide frequency band respectively, which implies good wideband performance.

III. Verification and Measurement Results

For verification, the DPA was fabricated on a Taconic RF35 substrate ($\varepsilon_r = 3.55$, $h = 30$ mil) within the band of 1.6–2.2 GHz, as shown in Fig. 4. The input matching networks were designed by using the stepped-impedance matching network to cover the required bandwidth. A 3 dB 90° hybrid coupler was used as the input splitter. In addition, a four-order real-to-real post-matching network (PMN) was used to convert 50 Ω to Z_L at the combining point. The carrier quiescent current and the peaking gate bias were chosen to be 0.1 A and –7 V, while the drain bias of the two amplifiers were 28 V and 50 V.

Fig. 5 shows the simulated and measured drain efficiency (DE) and gain of the DPA under continuous wave (CW) measurement across the design bandwidth. Good Doherty efficiency behavior with a saturated output power of higher than 46 dBm can be observed. The DE is within 60%–71% and 51%–55% at saturation and 10 dB OBO powers, while the gain fluctuation is less than 2 dB. The DPA was also measured under a 20 MHz long term evolution (LTE) signal with 9.1 dB PAPR at an average output power of 36 dBm, as shown in Fig. 6. The results show that the DPA can achieve good average efficiency of higher than 50% with adjacent channel leakage

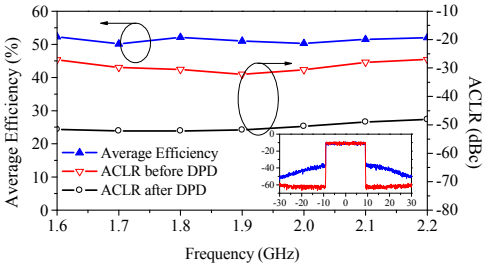

Fig. 6. The measured average efficiency and ACLR before and after DPD using modulated signal and measured spectrum at 1.9 GHz.

TABLE II

Comparison of DPAs with Large Back-off Power Range

Ref.	Freq. (GHz)	FBW (%)	OBO (dB)	DE@ Sat.(%)	DE@ OBO(%)	Signal BW(MHz)	ACLR with DPD(dBc)
[1]	0.79-0.96	19.4	10	52-60	50-60	20	-50
[2]	1.85-2.4	25.9	10	55-75	33-65	20	-42
[3]*	0.7-0.95	30.3	9.54	60-78.3	50.2-67	5	-49
This work	1.6-2.2	31.6	10	60-71	51-55	20	-48

* three-stage DPA

ratio (ACLR) of better than –48 dBc at 10 dB OBO power after digital predistortion (DPD). The piecewise second-order dynamic deviation reduction (DDR) model was used in the DPD modeling [7]. Fig. 6 shows the measured spectrum of the DPA before and after DPD at the frequency of 1.9 GHz. Table II compares the performance of the DPAs. The proposed DPA achieves the widest operation bandwidth, while maintaining high efficiency at 10 dB OBO power over the design band.

IV. Conclusion

A DPA topology with minimum phase delay in OMN was introduced and validated. The designed DPA achieves an efficiency of higher than 50% at 10 dB OBO power with the fractional bandwidth (FBW) of over 31.6%.

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