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Chun-Hu Cheng, H.C. Pan, H.J. Yang, C.N. Hsiao ...+3 more authors

Institutions: National Chiao Tung University, National Research Council

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Topics: Film capacitor, Leakage (electronics), Capacitor, High-κ dielectric and Dielectric

Improved High-Temperature Leakage in High-Density MIM Capacitors by Using a TiLaO Dielectric and an Ir Electrode

C. H. Cheng, H. C. Pan, H. J. Yang, C. N. Hsiao, C. P. Chou,
S. P. McAlister, *Senior Member, IEEE*, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We have fabricated high-κ TaN/Ir/TiLaO/TaN metal–insulator–metal capacitors. A low leakage current of 6.6×10^{-7} A/cm^2 was obtained at 125 °C for 24-fF/μm^2 density capacitors. The excellent device performance is due to the combined effects of the high-κ TiLaO dielectric, a high work-function Ir electrode, and large conduction band offset.**

***Index Terms*—High-κ, Ir, metal–insulator–metal (MIM), TiLaO.**

I. INTRODUCTION

THERE is a continuing demand to increase the capacitance density $(\varepsilon_0\kappa/\mathrm{t}_\kappa)$ of the metal–insulator–metal (MIM) capacitors [1]–[16]. To achieve this, the MIM devices have evolved by using higher κ dielectrics such as SiN [3], [4], Al_2O_3 [6], [7], Ta_2O_5 [5], HfO_2 [8]–[10], Nb_2O_5 [11], TiTaO [12], [13], and $SrTiO_3$ (STO) [14]–[16]. Unfortunately, increasing the κ value usually decreases the conduction band offset $(\Delta E_C)$with respect to the metal electrode. For STO [17], ΔE_C can even be slightly negative. A low ΔE_C leads to unwanted leakage current for a MIM device at high temperatures [16], where such increase in the operational temperature is unavoidable due to the increased circuit density and higher power dissipation. Although STO shows higher κ values and good device characteristics, a higher process temperature > 450 °C for nanocrystal formation and thicker thickness to reduce leakage are necessary. This exceeds the maximum temperature (400 °C) permitted for backend integration [14]–[16].

Here, we report low thermal leakage TiLaO MIM capacitors using a high work-function Ir electrode, which are processed at 400 °C. We measured leakage currents of 1×10^{-7} and 6.6×10^{-7} A/cm^2 at 1 V at 25 °C and 125 °C, respectively; these currents are lower than those in the previously reported TiTaO and 400 °C-processed STO capacitors.

II. EXPERIMENTAL PROCEDURE

The high-κ TiLaO MIM capacitors were fabricated on standard Si wafers. To permit VLSI backend integration, the process began with depositing a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then, a 50-nm TaN was deposited on a 200-nm Ta layer by sputtering and used as the lower capacitor electrode. The TaN surface was then given a plasma treatment to increase the oxidation resistance before the high-κ deposition and postdeposition annealing (PDA) [5], [6]. A 15-nm-thick $Ti_xLa_{1-x}O$ (x $\sim$ 0.67) film was deposited by PVD, followed by a 400-°C PDA in an oxygen ambient to reduce the defects and the leakage current [3] (the TiLaO thickness was later measured by cross-sectional transmission electron microscopy). Finally, 20-nm Ir and/or 50-nm TaN were deposited and patterned to form the top electrode. A large capacitor size of 100 μm × 100 μm was chosen to avoid any variations in dimensions arising from lithography. The devices were characterized by C–V and J–V measurements.

III. RESULTS AND DISCUSSION

In Fig. 1, we show the C–V, J–V, and thermal-stability characteristics of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN devices. A comparison with other data is summarized in Table I. A high capacitance density of 24–24.5 fF/μm^2 was measured for the TiLaO MIM devices, which gives a high-κ value of $\sim$45 for the TiLaO dielectric. A leakage current of 2.2×10^{-6} A/cm^2 at -1 V was measured for the TaN/TiLaO/TaN MIM capacitor close to that of an Ir/TiTaO/TaN device (Table I) with a slightly lower capacitance density. Since the work function of the TaN on TiLaO is $\sim$0.7 V lower than that of Ir on TiTaO, the comparable leakage current indicates that the TiLaO is a better choice for MIM capacitors than TiTaO. This is confirmed by the five times lower leakage current of 1×10^{-7} A/cm^2 in the TaN/Ir/TiLaO/TaN device compared with the Ir/TiTaO/TaN capacitor. This improved leakage current, at a comparable capacitance density, is due to the higher ΔE_C between metal and high-κ interface, which lowers the leakage current exponentially. A similar lower leakage current was also reported by adding higher ΔE_C Al_2O_3 into HfO_2 MIM capacitor [9]. The

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C. H. Cheng and C. P. Chou are with the Department of Mechanical Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

H. C. Pan and C. N. Hsiao are with the Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan, R.O.C.

H. J. Yang and A. Chin are with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: albert_achin@hotmail.com; achin@cc.nctu.edu.tw).

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON K1A 0R6, Canada.

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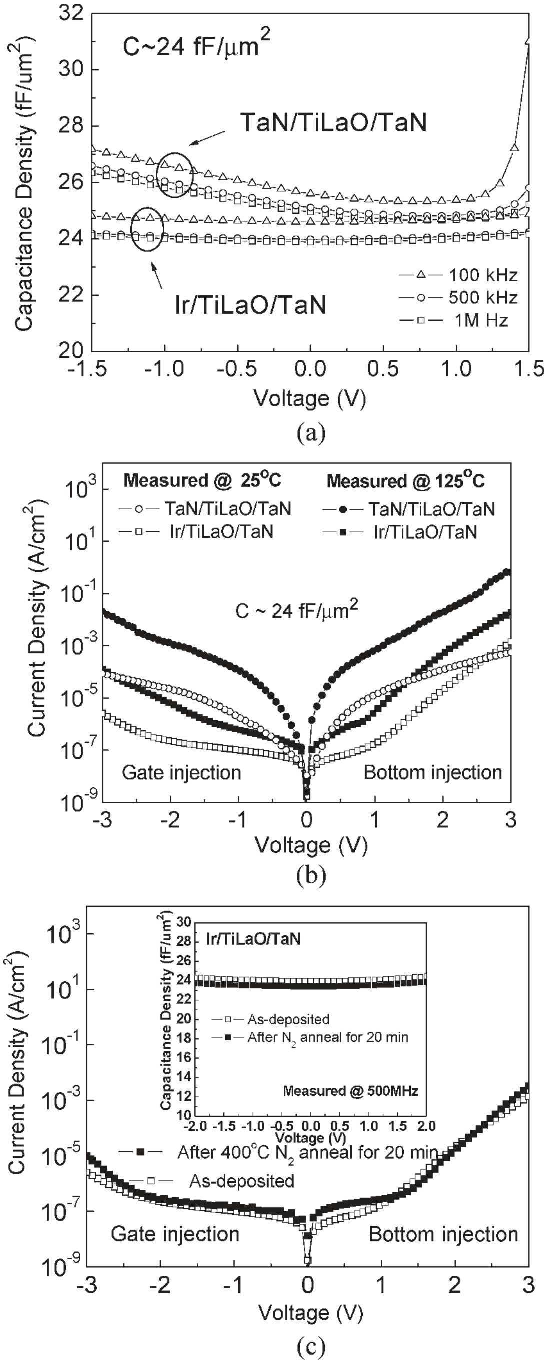

(a)

(b)

(c)

Fig. 1. (a) C–V, (b) J–V, and (c) thermal-stability characteristics of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN MIM capacitors measured at various frequencies, at 25 °C and 125 °C. The thermal-stability test was performance at 400 °C for 20 min in an ambient N_2.

small changes of J–V and C–V, after 400-°C N_2 annealing, indicate that the thermal stability is acceptable. Note that good thermal stability was reported for metal-gate/high-κ pMOS for Ir on HfAlON at Rapid Thermal Anneal (RTA) temperatures up to 900 °C [17].

A larger ΔE_C at the metal/high-κ interface is very important at 125 °C, which is a temperature required for both DRAM and nonvolatile memory [18]. This is shown in the comparison with STO: The leakage current (at -1 V) of a 400 °C-formed Ni/STO/TaN capacitor increased from 2×10^{-7} to 5×10^{-6} A/cm^2, from 25 °C to 125 °C (Table I), whereas in the TaN/Ir/TiLaO/TaN capacitor, it only increased from 1×10^{-7} to 6.6×10^{-7} A/cm^2. Although the work function of the Ir electrode (5.27 eV) is slightly higher than Ni (5.1 eV), the improved 125-°C leakage current can be attributed to the large ΔE_C. We note that La_2O_3 has the highest ΔE_C with respect to Si (2.3 eV) compared with HfO_2 (1.5 eV), ZrO_2 (1.4 eV), Ta_2O_5 (0.3 eV), and STO (−0.1 eV) [19].

TABLE I
COMPARISON OF MIM CAPACITORS WITH VARIOUS DIELECTRICS AND METAL ELECTRODES

	HfO_2 [8]	Tb-HfO_2 [10]	Al_2O_3-HfO_2 [9]	TiTaO [12]–[13]	STO [16]	STO [14]	**TiLaO**	
Process Temp. (°C)	400	400	400	400	400	450	**400**	
Top Electrode	Ta	Ta	TaN	Ir	Ni	TaN	TaN	Ir
Work-function (eV)	4.2	4.2	4.6	5.27	5.1	4.6	4.6	5.27
C Density (fF/μm^2)	13	13.3	12.8	23	25.2	28	24.5	24
J (A/cm^2) @25°C	6×10^{-7} (2V)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-6} (1V) 2×10^{-5} (2V)	2×10^{-7} (1V) 8×10^{-6} (2V)	3×10^{-8} (2V)	2.2×10^{-6} (1V)	1×10^{-7} (1V) 2.3×10^{-7} (2V)
J (A/cm^2) @125°C	2×10^{-6} (1V)	2×10^{-7} (2V)	6×10^{-9} (1V) 5×10^{-8} (2V)	-	5×10^{-6} (1V)	-	1.3×10^{-4}	6.6×10^{-7} (1V) 6.7×10^{-6} (2V)

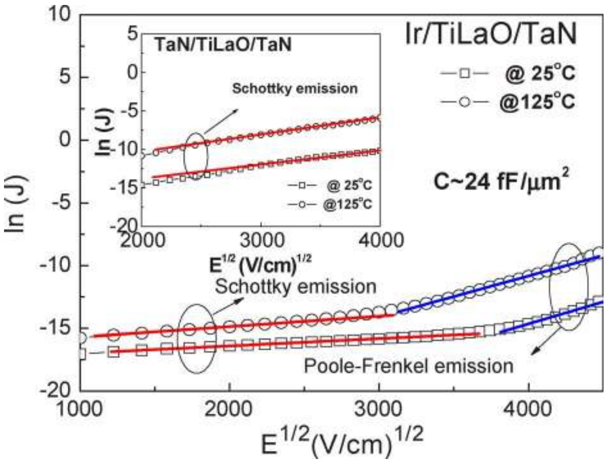

Fig. 2. Measured and simulated J–$E^{1/2}$ of an Ir/TiLaO/TaN capacitor. A TaN/TiLaO/TaN device is shown, for comparison, in the inset.

To investigate the current conduction mechanism we plot, in Fig. 2, $\ln(J)$ versus $E^{1/2}$ for the TaN/Ir/TiLaO/TaN MIM capacitors

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \tag{1}$$

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2}. \tag{2}$$

Here, K_∞ is the high-frequency dielectric constant $(= n^2)$. The refractive index n is 2.57 or 1.9 for TiO_2 or La_2O_3 [20],

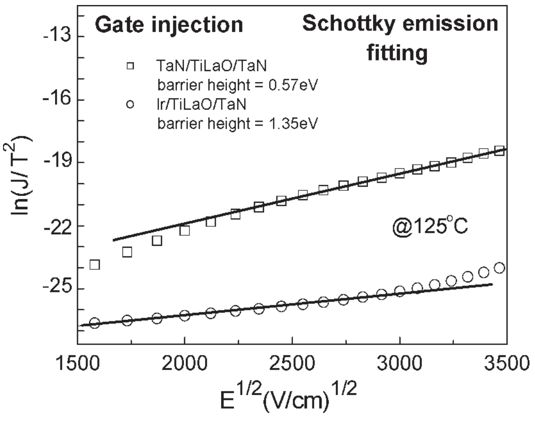

Fig. 3. J/T^2–$E^{1/2}$ plots of TaN/TiLaO/TaN and TaN/Ir/TiLaO/TaN MIM capacitors.

and η is 1 or 4 for Schottky emission (SE) or Frenkel–Poole (FP) conduction, respectively. The data fitting suggests that the current conduction mechanism of the TaN/Ir/TiLaO/TaN device changes from SE at low electric fields to FP at higher fields. In contrast, the TaN/TiLaO/TaN devices fit an SE description at both low and high fields.

The SE barrier height (V_b) at 125 °C was determined from J/T^2–$E^{1/2}$ plots (Fig. 3). Values for V_b were 0.57 and 1.35 eV for TiLaO devices at 125 °C with TaN and Ir top electrodes, respectively. The large V_b difference explains the reduced leakage current and the weaker temperature dependence in the TaN/Ir/TiLaO/TaN devices. Thus, a low leakage current at high temperature can be obtained in MIM capacitors by combining a high-κ dielectric, having a high ΔE_C, with a high work-function metal electrode.

IV. CONCLUSION

A high capacitance density and low leakage current at 125 °C have been achieved in Ir/TiLaO/TaN MIM capacitors. The device-processing temperature of 400 °C would enable them to be integrated into the VLSI backend technology and be used in multiple functions associated with system-on-a-chip.

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