Improved Off-Current and Subthreshold Slope in Aggressively Scaled Poly-Si TFTs With a Single Grain Boundary in the Channel

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***Abstract*—A polycrystalline-silicon thin-film transistor (TFT), with a single grain boundary (GB) present in the channel, is simulated using two–dimensional numerical simulation, which includes a model of deep trap states at GBs. It is observed that the potential barrier resulting from a GB in the channel acts to suppress current flowing through the channel when the barrier height is greater than the thermal voltage. The conduction mechanism in the subthreshold regime is clarified. The turn-on characteristics of the device are controlled primarily by gate-induced grain barrier lowering as opposed to modulation of carriers in the channel by the gate voltage. In the negative bias region it is found that suppression of the off current is aided by the GB potential barrier. Scaling of the various geometrical parameters of the device are investigated. Improved subthreshold characteristics, compared to an equivalent silicon-on-insulator (SOI) structure, are found for aggressively scaled devices, due to the presence of a GB in the channel.**

***Index Terms*—Defect, device simulation, electric conductivity, grain boundary, moderately doped, polysilicon, scaling, thin-film transistor.**

I. Introduction

POLYSILICON thin-film transistors (TFTs) have been studied extensively in recent years for their application in flat panel active matrix displays and three-dimensional (3-D) integration. When poly-Si TFTs are used in LCD applications, the minimum feature size is typically very large $\gg 10$ μm and therefore a large number of grain boundaries (GBs) are present in the channel. When modeling such devices, the effect of the GBs is considered to reduce the electron mobility below the bulk-single crystal value. In such an analysis the discrete properties of individual GBs are not considered. In scaling the channel of the device down to a length comparable to the poly-Si grain size or by controlling grain growth using modern metal-induced lateral crystallization (MILC) or excimer laser annealing techniques it is possible to create devices where only a small number of discrete GBs exist in the TFT channel.

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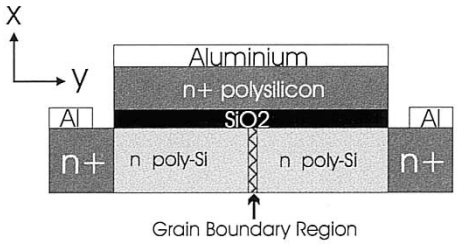

Fig. 1. Structure used for the TFT simulation.

Therefore it is increasingly important to understand the discrete effects of a GB on conduction [1].

In this work, we study the effect of having a single grain boundary in the channel of a moderately doped poly-Si TFT. Specifically we seek to explain more fully the conduction mechanism when a single GB is present than has been previously discussed [2], [3]and to investigate the effect on transistor performance. By comparing the subthreshold characteristics of the TFT with a silicon-on-insulator (SOI) equivalent device any differences due to the presence of the GB can be observed. This study investigates effects on subthreshold slope, off current and threshold voltage in devices where only one GB is present in the channel. The effect of scaling the channel length $L_{\rm eff}$ and the silicon thickness $t_{\rm si}$ in such as device is also investigated.

II. Description of Modelling Approach

To simulate the TFT and silicon-on-insulator (SOI) devices, a two-dimensional (2-D) device simulator [4] was used. The basic semiconductor equations used are the same as those of a single crystal device except that the trapped charges within the grain boundary region are included in Poisson's equation. A conventional drift-diffusion method is used to model carrier transport and, moreover, the Shockley–Read–Hall model for carrier emission-absorption processes at the boundary is included. Poisson's equation and the current continuity equations are discretized on a 2-D finite difference mesh lattice and then numerically solved in an iterative way.

The device structure used to simulate the device is shown in Fig. 1 and the device parameters in Table I. The effective trapping density at the grain boundary is taken to be $1.0 \times 10^{13}{\rm cm}^{-2}$ and the trap energy relative to the conduction band $\delta E_{DD} = 0.51\,{\rm eV}$. The capture rate for electrons (C_D^n) and the capture rate for holes (C_D^p) is equal to 1×10^{-8} ${\rm cm}^3/{\rm sec}$. Initially, only electron traps are considered at the grain

TABLE I
PARAMETERS FOR THE SIMULATED DEVICE

Parameter	Range of Values
Channel Length L_{eff}	50nm-400nm
Silicon Film Thickness t_{si}	25nm-200nm
Gate Oxide Thickness t_{ox}	10nm
Channel Doping Concentration N_{D}	$1\text{x}10^{17} cm^{-3}$
Source,Drain and Gate Doping Concentration	$1\text{x}10^{21} cm^{-3}$
Density of Deep Donor like Traps N_{DD}	$1\text{x}10^{13} cm^{-2}$
Density of Deep Acceptor like Traps N_{DA}	$1\text{x}10^{13} cm^{-2}$
Trap Energy Level Relative to Conduction Band δE_{DD}	0.51eV
Trap Energy Level Relative to Valence Band δE_{DA}	0.51eV
Capture Rate for Holes C_{A}^{p},C_{D}^{p}	$1\text{x}10^{-8} cm^3/sec$
Capture Rate for Electrons C_{A}^{n},C_{D}^{n}	$1\text{x}10^{-8} cm^3/sec$

boundary. A model of trap-to-band tunneling, for gate-induced drain leakage (GIDL), is not included in the present simulation. This enables the effect of the presence of the GB, on the subthreshold characteristics, to be observed without being obscured by high leakage currents. The position of the GB is assumed to be at the centre of the channel and it is considered to have a finite width of 4 nm. In a real device it is difficult to control the position of the GB relative to the source and drain and therefore the positional dependance of the GB in the channel requires further investigation.

III. CARRIER TRAPPING AT THE GB AND GATE-INDUCED GRAIN BARRIER LOWERING

The carrier-trapping model used by Seto in [5]–[7] is used as the basis for the explanation of the conduction mechanism in the poly-Si film. In this model it was shown that a potential barrier forms at the GB associated with carriers becoming immobilized by traps due to strain and dangling bonds located at the boundary. As a consequence, the boundary becomes negatively charged and a positively charged depletion region forms at both sides of the boundary to satisfy charge neutrality. This results in bending of the energy bands and so a potential barrier forms at the GB. An increase in the number of carriers trapped at the GB leads to an increase in the height of the potential barrier. Setos model predicts that, above a critical doping density, all the traps at the GB will be filled and the remaining carriers will reduce the width of depletion region, leading to a decrease in the height of the barrier. This behavior is described by

Theorem 1 (Setos Depletion Approximation Model): While the doping density

$$N_D < \frac{N_T}{L} \tag{1}$$

the potential barrier height increases as a function of N_D

$$qV_B = \frac{qN_D L^2}{8\epsilon} \tag{2}$$

and when

$$N_D > \frac{N_T}{L} \tag{3}$$

the potential barrier height decreases

$$qV_B = \frac{qN_T^2}{8\epsilon N_D} \tag{4}$$

where qV_B is the barrier height, N_D the doping density, N_T the trap density, L the grain size, and ϵ the dielectric constant of silicon.

It is expected that a similar reduction in the height of the GB potential barrier will be observed in the doped poly-Si channel of a TFT [6]. As the gate bias is increased, the number of carriers close to the interface should increase, so decreasing the width of the depletion layer. The effect on the depletion layer width is similar to that resulting from an increase in doping density. This reduces the height of the potential barrier and causes the so-called gate induced grain barrier lowering (GIGBL) effect [8], [9].

Using the 2-D simulation described previously we calculated the potential barrier height for equilibrium conditions as a function of channel doping density Fig. 2(a). Also plotted is the barrier height obtained using Setos model. The disagreement between the two curves is believed to result from simplifications made in [5] in deriving (1)–(4). In Setos model it is assumed that all free carriers become trapped when the depletion region does not extend throughout the entire crystallite and therefore is valid only for the special situation where the fermi level E_F is always above the trap energy level E_T. In fact, as the doping concentration N_D is decreased the fermi level moves away from the conduction band. When E_F becomes equal to E_T the Fermi energy becomes pinned Fig. 2(b) and hence the barrier height does not extend to the height predicted by the Seto model [7].

This simulation indicates that the critical doping density for a GB seems to be around 1×10^{17} cm^{-3}. A potential barrier of this magnitude would be sufficient to reduce the current flow significantly. A number of devices with different doping densities were simulated. In each simulation the gate bias was swept from 0 to 10 V and the potential barrier height at a depth (x direction) of 2 nm from the interface plotted as a function of V_g. The results Fig. 3 suggest that the barrier height can be controlled by modulation of carriers in conduction channel. Importantly, the barrier height is reduced rapidly with increasing gate bias, so that only a small bias voltage needs to be applied for the barrier to be lowered significantly. The maximum height of the barrier is highly dependent on the defect or trap density at the GB, with a large number of defects resulting in a high potential barrier, when all the trap states are filled [10]. The maximum barrier height is lower when the gate electrode is included in the

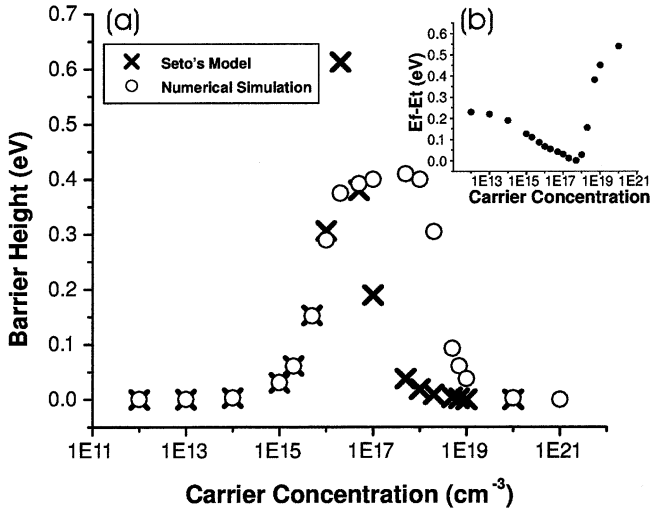

Fig. 2. (a) Grain boundary potential barrier height plotted against doping density N_D. Values calculated using Setos model and numerical simulation are shown. For the numerical simulation, the critical doping density appears to be around 10^{17} cm^{-3} above this value the barrier height decreases rapidly. (b) $E_f - E_t$ as a function of carrier concentration showing some fermi pinning phenomena at moderate doping concentrations.

device structure. This is a result of downward band bending at the interface caused by the difference in the work function of the semiconductor and gate electrode.

IV. Dynamic Threshold Behavior in TFT Subthreshold Characteristics

As a result of the n-type doping of the channel region devices operate in accumulation mode [6]. In [1] it was suggested that thermionic emission over the GB barrier is the limiting transport process when V_B is larger than the thermal voltage. When V_B is reduced by GIGBL to below the thermal voltage, the characteristics will become similar to those predicted by a conventional SOI MOSFET model. When the barrier height becomes greater than the thermal voltage the current flow will be reduced. Two devices were simulated, both with a channel doping density of 1×10^{17} cm^{-3}, channel thickness $(t_{\rm si})$ 0.2 μm, channel length $(L_{\rm eff})$ 0.4 μm and oxide thickness $(t_{\rm OX})$ 10 nm. The first device has a grain boundary present in the centre of the channel and the other device uses a single crystal silicon channel.

A. Subthreshold Characteristics

The resulting subthreshold characteristics can be seen in Fig. 4. For a device with a grain boundary in the channel and an equivalent SOI device, the drain current (I_d) against the gate voltage (V_g) are plotted. This result is for the linear regime of the TFT with a low drain bias voltage $(V_d = 0.01$ V).

It can be seen that the current in the TFT device appears to be suppressed around the 0 V region of operation producing a dip in the subthreshold slope. When the gate voltage is highly positive $(V_g > 1$ V) or negative $(V_g < -1$ V) the drain current is similar to that for the SOI device. Conventionally, the concept of subthreshold swing or S-factor is usually used to describe the quality of the turn on characteristics where the device is controlled solely by modulation of carriers in the channel by a gate voltage. As discussed in [9], the TFT characteristics are not

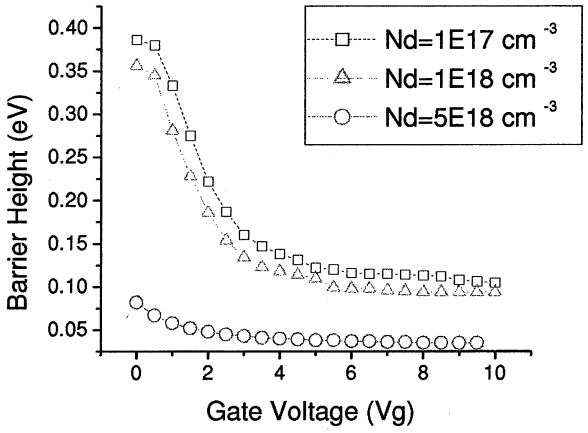

Fig. 3. Grain boundary barrier height against gate bias for various channel doping densities. Notice that the barrier height decreases very rapidly for small increases in gate voltage (V_g). This is GIGBL.

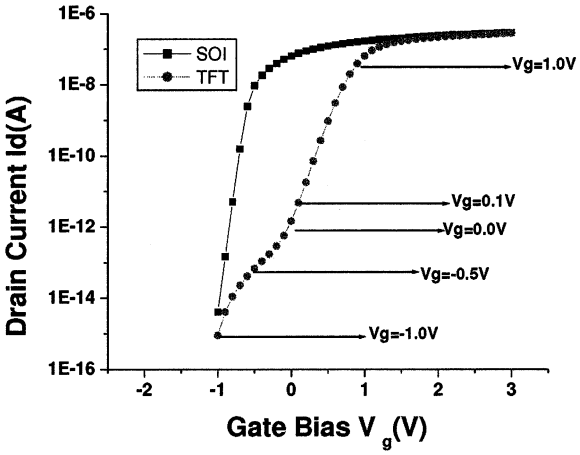

Fig. 4. Comparison of characteristics for a TFT with a single GB in the channel and single crystal SOI TFT with similar geometry. The TFT has a non linear "pseudo-subthreshold slope" as its turn on voltage is determined by GIGBL rather than carrier modulation by the gate bias.

linear and the turn on of the device seems to occur by a different mechanism than applies in the conventional SOI MOSFET, so perhaps, calling this the "pseudo-subthreshold slope" is appropriate. We suggest that this behavior is made clear in our device simulations because leakage current mechanisms are not included. In a real device leakage currents of greater that 1×10^{-13} A would hide the current suppression that results from the GB [11], [12]. To investigate the effect of the GB on conduction in the region of interest, the 2-D surface potential was plotted for points where the gate bias was above, below and equal to the point of maximum current suppression.

B. Conduction Mechanism Leading to Dynamic Threshold Behavior

The results seem to show two distinct conduction effects caused by the GB. When the gate is unbiased the region in the channel surrounding the GB is close to full depletion, with all the available trapped states at the grain boundary filled. Hence the resulting potential barrier is at, or close to, its maximum height.

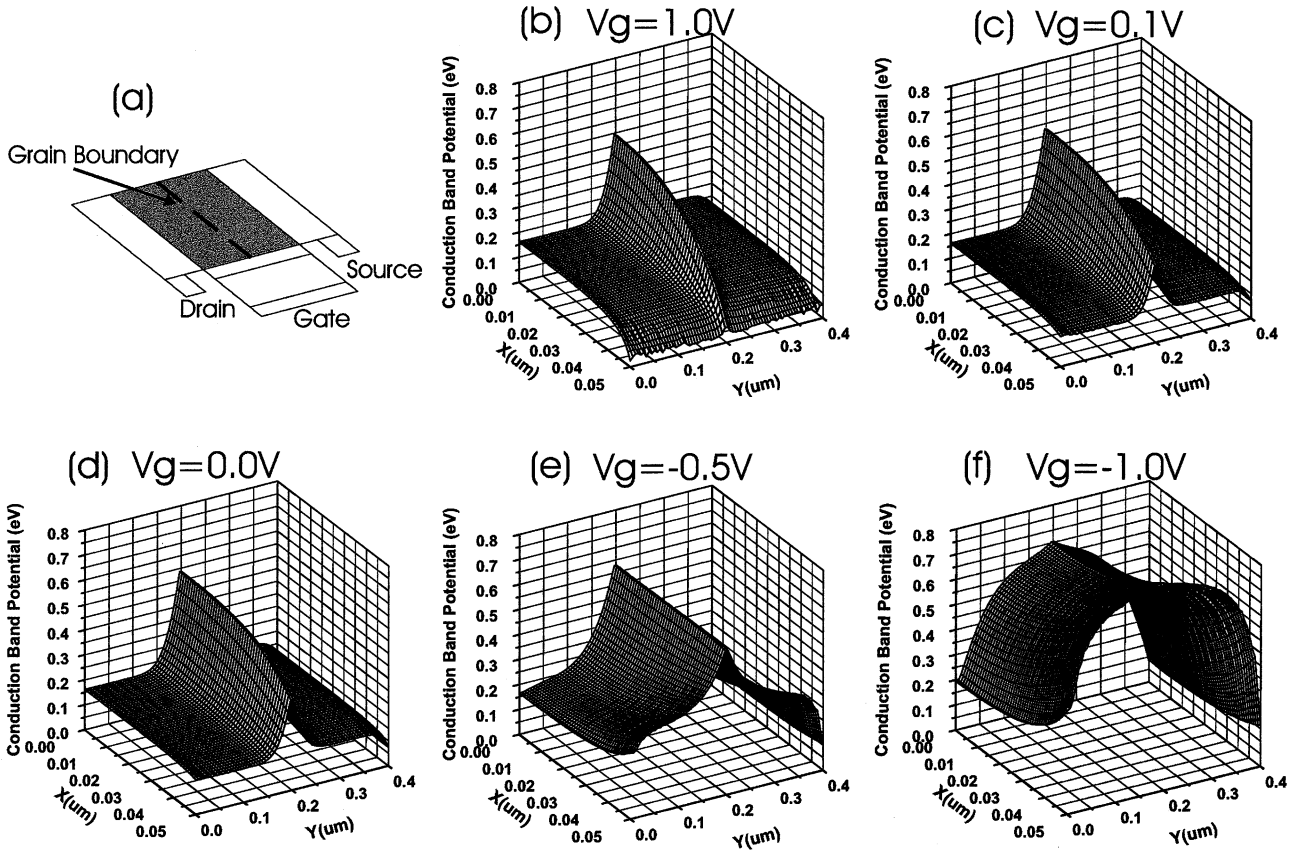

Fig. 5. (a) Device cross-section with modeled region of channel shaded. Conduction band potential for (b) $V_g = 1.0$ V, (c) $V_g = 0.1$ V, (d) $V_g = 0$ V, (e) $V_g = -0.5$ V, and (f) $V_g = -1.05$ V.

1) On Current Regime: With increasing gate bias, Fig. 5(b)–(d) shows that the barrier is reduced close to the interface allowing more current to flow. This continues until the barrier height at the interface is smaller than the thermal voltage, at which point the barrier no longer impedes current flow and the transistor behavior is similar to that of the SOI equivalent device. The strong dependance of the drain current on the gate voltage in this region is due to the rapid reduction of the barrier with gate bias observed in Fig. 3.

2) Subthreshold Regime: In the subthreshold regime the presence of the barrier aids the suppression of the off current. As the bias voltage is made increasingly negative, the potential barrier at first acts to suppress the current flow in the channel; resulting in a lower drain current than is present in the SOI MOSFET under this gate bias. Later, the modulation of the channel potential by the gate becomes dominant and the potential barrier formed by this mechanism becomes equal to, or greater than, the GB barrier. At this point the characteristics again match those of the SOI device Fig. 5(f) as the GB is no longer a significant factor in the conduction mechanism within the channel.

C. Effect of Minority Carriers on GB Potential Barrier

So far in our simulations we have neglected hole traps at the GB. It has been assumed that as holes are the minority carrier, their trapping at the GB would have a minimal effect. To investigate this, a number of hole trap states were introduced at the same energy relative to the valence band as the electron trap states were to the conduction band ($\delta E_{DD} = \delta E_{DA}$). The hole trap density was also made equal to that for the electron traps ($N_{DD} = N_{DA}$).

Fig. 6(a) shows a comparison of the subthreshold characteristics for a TFT with a single GB with just electron traps, both hole and electron traps, and a single crystal SOI device. The introduction of hole traps has the effect of reducing the magnitude of the current suppression caused by the GB barrier. This behavior can be explained as follows. The minority carriers cause the barrier height to be reduced by neutralizing some of the charge due to the majority carriers trapped at the grain boundary. This is illustrated in Fig. 6(b) and (c) the lower barrier height in Fig. 6(c) is a result of the introduction of hole trap states in the energy bandgap. This effect is especially important for the case when the gate is negatively biased. This causes the holes to be pulled toward the conducting channel as an inversion layer is formed. When only a small number of holes are present it is assumed that all will be trapped in hole trap states. Therefore the net negative charge at the GB decreases and the amount of compensating charge in the surrounding space charge region also decreases. Hence the barrier height is lower than with electron traps only and the current suppression and dynamic threshold behavior are reduced. However under large negative bias their effect is unimportant, as modulation of the channel potential by the gate is again dominant and causes the characteristics to revert to those of the SOI MOSFET.

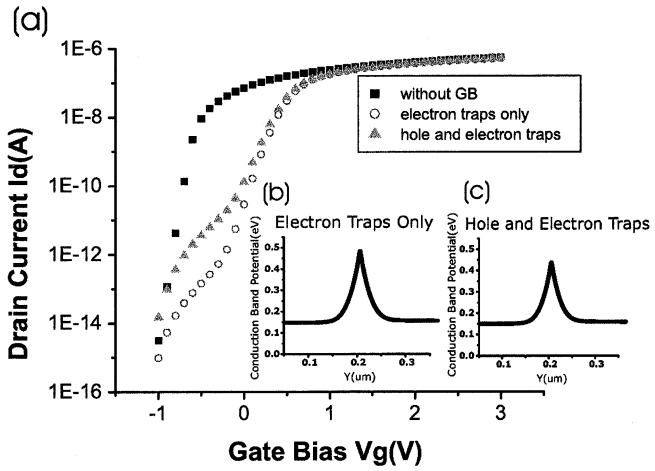

Fig. 6. (a) Including hole traps in the simulation model leads to a reduction in the current suppression when compared to the simulation where only electron trapping was considered. At 0 V the current differs by around an order of magnitude. The potential at 10 nm from the interface for (b) a device with just electron traps and (c) a device with both hole and electron traps.

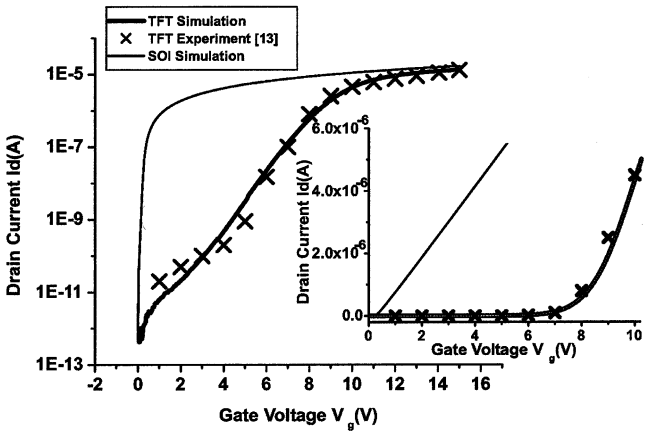

Fig. 7. Comparison between simulated and experimental [13] I_d–V_g characteristics for a p-channel inversion mode TFT with two lateral GBs in the channel region on both logarithmic and (inset) linear scale. Notice dip in slope at $V_g = 5$ V which corresponds to the gate bias where the barrier height is at a maximum. Good agreement is found when $E_T = 0.65$ eV and $N_T = 6 \times 10^{19}$ cm^{-3}.

If the grain boundary had only hole traps, this would have little effect on an n-type device. The characteristics would be similar to a SOI equivalent device. However if the channel was p-type and conduction was by holes rather than electrons then the a downward barrier would be formed at the GB. This would impede hole transport in a similar way that the upward barrier impedes electron transport therefore suppressing the current.

Fig. 6 suggests a significant change in characteristics is caused by the introduction of minority carrier traps and that their effect should not be ignored. Therefore in all further simulations hole traps were included in the simulation model.

D. Comparison With Experiment

It is necessary to provide experimental proof to support these modeling results. An SOI transistor with two GBs in the channel region perpendicular to the current flow is described in [13]. The device is an inversion mode transistor with a 5×10^{16} cm^{-3} p-doped channel region with channel length $L_{\text{eff}} = 14$ μm. Measurements indicate current suppression at a gate bias of 5 V which the author attributed to leakage currents. We believe the cause to be GIGBL with a gate bias of greater than 5 V required to lower the GB barriers in the channel. The threshold voltage is larger than in Fig. 6 for two reasons. Firstly this can be attributed to the device being a p-type inversion mode transistor as opposed to an n-type accumulation mode transistor Fig. 6 and therefore large band bending is required for the onset of inversion. Secondly a thicker oxide is used for this simulation, to match the structure used in the experiment.

To validate our modeling technique we simulated this device and compared the results with those measured by experiment [13]. Comparing the experimental and simulation results in Fig. 7 we can see there is good agreement on both linear and logarithmic scales. This result was found by setting $E_T = 0.65\,\text{eV}$, $N_T = 6 \times 10^{19}$ cm^{-3}, which is in agreement with the experimentally measured values in [14] and giving the silicon regions a reduced mobility of $\mu_n = 600$ cm^2/V $\cdot$ s. Capture rates and source and drain doping were as given in Table I.

V. Device Scaling

In order to investigate the usefulness of the GB effects a range of simulations were performed comparing SOI devices and single GB TFT devices with equal geometries. This was done to study whether the TFT would conform to the same scaling laws that have been proposed for the conventional SOI MOSFET [15].

It is instructive to look at the scaling theory of SOI devices to indicate what changes in behavior to expect as the GB TFT device is scaled.

A. Scaling Theory of SOI Devices

By solving Poisson's equation in the body of a fully depleted SOI MOSFET transistor, Yan *et al.* [16] defined an intrinsic length

$$\lambda_{\text{FD}} = \sqrt{\frac{\epsilon_{\text{si}}}{\epsilon_{\text{OX}}} t_{\text{si}} t_{\text{OX}}}. \tag{5}$$

According to this theory, in order to maintain subthreshold characteristics as the device is scaled, the SOI MOSFET should be designed to maintain

$$\alpha = \frac{L_{\text{eff}}}{\lambda_{\text{FD}}}. \tag{6}$$

It has been shown that reasonable values for subthreshold swing, charge sharing effect and drain induced barrier lowering are achieved if the channel length L_{eff} is 5–10 times larger than λ_{FD}.

B. Scaling of Silicon Film Thickness (t_{si}) and Channel Length (L_{eff})

According to (5) and (6), it suggests that if L_{eff} is reduced then t_{si} must also be reduced and similarly if t_{si} is increased then L_{eff} must be increased. Otherwise degradation of transistor performance will occur as a result of short channel effects [15], [17]–[19].

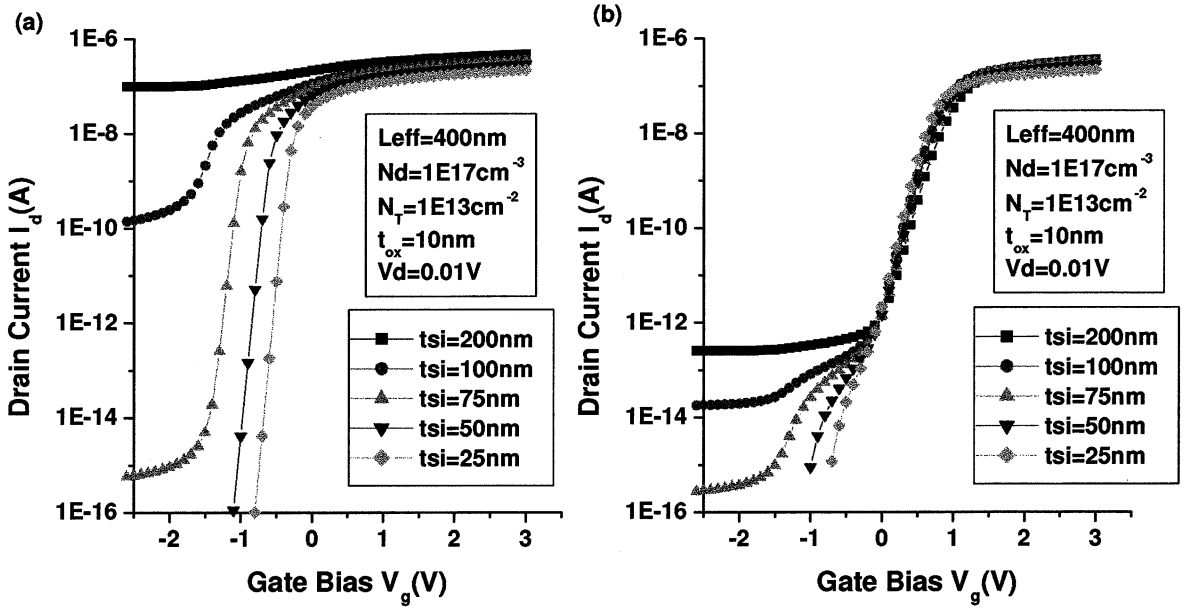

Fig. 8. (a) SOI MOSFET and (b) single-GB TFT. The single GB TFT shows superior transistor characteristics than for the SOI MOSFET when the silicon thickness $t_{\rm si} > 0.75$ μm. Notice also that above 0 V the TFT pseudo-subthreshold slope is almost independent of $t_{\rm si}$, this is because the turn on point is determined by GIGBL.

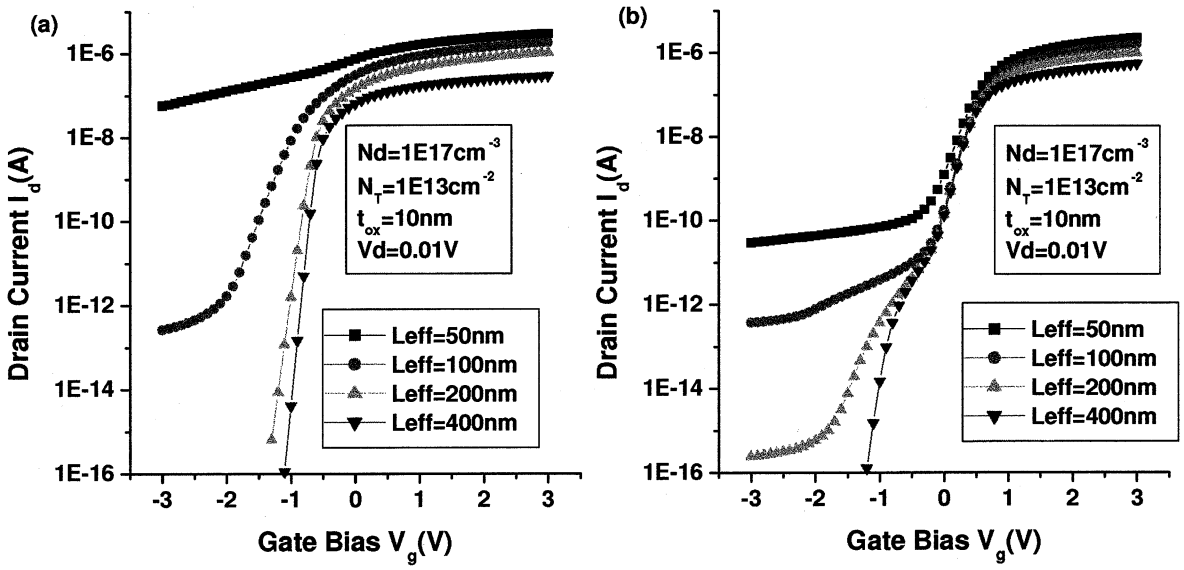

Fig. 9. (a) SOI MOSFET and (b) single-GB TFT. Similar to Fig. 9, the single GB TFT shows better subthreshold behavior when the channel length is scaled below 0.1 μm turn in is by GIGBL and additional current suppression in the off regime is provided by the GB potential barrier.

Simulation results are shown in Figs. 8 and 9. As expected, increasing $t_{\rm si}$ while leaving $L_{\rm eff}$ unaltered leads to degradation of the performance of the SOI transistor due to short channel effects. At a $t_{\rm si}$ of 0.2 μm the modulation of the channel potential by the gate is so weak that there is less than one order of magnitude change between the off and the on currents.

In contrast, for the TFT with a GB at the centre of the channel there is only degradation in pseudo-subthreshold slope in the negative bias regime as the channel thickness is increased. Above 0 V, in the region where the conduction in the channel is controlled by GIGBL, the subthreshold slope is nearly constant for all thicknesses. As the turn on characteristics are determined by GIGBL, as previously discussed, a finite voltage (threshold voltage $V_T = 1$ V in our case) is required to turn on the device, whereas the SOI device will turn on at $V_T = 0$ V. In summary, superior subthreshold behavior is obtained by introducing a GB into the channel for high $t_{\rm si}$ at the cost of an increase in V_T. However, for thicknesses consistent with the SOI scaling rule, given by (5) and (6), the SOI device remains superior.

A similar trend is found if we decrease $L_{\rm eff}$ while keeping $t_{\rm si}$ constant (Fig. 9). The subthreshold slope for the TFT with the GB varies very little above 0 V for devices with channel length as small as 50 nm. Fig. 10 illustrates this behavior by comparing the SOI and TFT characteristics for a device with $L_{\rm eff} = 50$ nm.

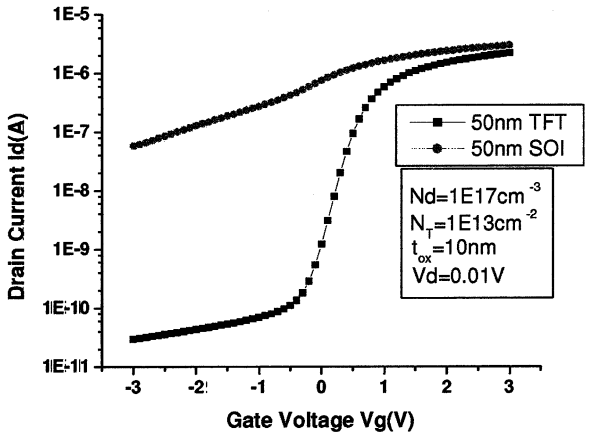

Fig. 10. Channel length is scaled down to 50 nm. By direct comparison of the I_d–V_g characteristics of a single GB TFT and a same geometry SOI device, it is easy to see that the GB improves the subthreshold behavior.

The TFT characteristics are clearly superior to the SOI characteristics for a device with these dimensions. Using the same arguments presented for increasing $t_{\rm si}$, improved subthreshold behavior is found by having a GB present in the channel for the case of short channel length devices, again at the cost of an increased threshold voltage.

VI. Conclusion

In this paper, the operation of TFT and equivalent SOI accumulation mode transistors in the linear regime have been simulated, showing that a TFT with a single GB at the centre of the channel operates by different conduction mechanisms than a conventional SOI MOSFET. By analysis of the 2-D potential in the channel region these mechanisms have been clarified. The threshold voltage V_T is determined by the GIGBL effect while suppression of the off current is aided by the GB potential barrier. The modeling technique used has been justified by comparison with a known experimental result for a TFT with two perpendicular GBs in the channel. Minority carrier traps have been shown to have a significant effect on the subthreshold characteristics, reducing current suppression by neutralizing negative charge at the GB.

For aggressively scaled devices—where in an SOI MOSFET short channel effects would have an unacceptably detrimental effect on subthreshold slope and off-current—the presence of a GB at the centre of the TFT channel aids in both suppression of the off current and improving the "pseudo-subthreshold slope". Therefore it is concluded that that for optimal TFT design complete removal of GBs may not be desirable. Further improvements in characteristics can be obtained through conventional scaling of $t_{\rm si}$ and $L_{\rm eff}$. It is also expected that the effects on the off current and subthreshold slope in aggressively scaled TFTs, will be present in TFTs with multiple perpindicular GBs in the channel, but the cost of an increased threshold voltage V_T.

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