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Improved Reactance-Compensation Technique for the Design of Wideband Suboptimum Class-E Power Amplifiers

Jiafeng Zhou (周加峰), Kevin Morris, Gavin Watkins, and Keiichi Yamaguchi

Abstract— **A reactance-compensation technique has been introduced recently for the design of wideband class-E power amplifiers. With this technique, the load resistance can be transformed to an optimal complex drain impedance in a broad frequency band. One potential problem of this technique is that an additional network is often needed to transform 50 Ω to the optimum load resistance, which is typically at a lower value.**

This paper proposes a method to improve the reactance compensation technique. By using the proposed method, the required low-value load resistance is up to four times the original value. This is achieved not by adding more components, but by simply changing the order and values of them. With the proposed method, the additional resistance matching network is no longer needed in many cases, or can be significantly simplified in other cases.

To validate the theory, two broadband class-E amplifiers were designed using the original technique and the proposed method, respectively. The performances of the two amplifiers are compared. By using similar complexity of matching networks, the PA designed using the original method can achieve better than 70% power added efficiency for a fractional bandwidth of 42%. The PA designed using the proposed method can achieve above 70% efficiency for a bandwidth of 51%. The proposed method can be used in the design of many other types of amplifiers.

Index Terms— **Class-E, switching mode, power amplifier, wideband, matching networks, impedance transforming, reactance compensation.**

I. Introduction

Due to their simple structure and relatively high efficiency, class-E[1] power amplifiers (PA) have been widely used for modern communication systems. Although the class-E PA was originally designed to operate in a narrow bandwidth, many techniques have been explored to increase its operational bandwidth. Design of tunable or switchable matching networks was reported in [2]. Discrete design of a wideband matching network was presented in [3]. A continuum of closed-form solutions for class-E power amplifiers is derived in [4], which provides possibilities for wideband class-E PA synthesis. Design of differential class-E load transformation networks for wideband operation was investigated in [5]. The wideband operation of class-E amplifiers can also be realized by using a finite feed inductor combined with LC-ladder lowpass filters [6][7].

A reactance-compensation technique [8] has been proposed to design wideband RF devices. Recently, the reactance-compensation technique has been introduced in [9] [10] [11][12] for the design of wideband class-E PAs. The reactance-compensation matching networks are relatively simple and a very wide bandwidth can be achieved with this technique. In [13], the technique was used to design a high-power wideband class-E PA at L-band from 900 MHz to 1500 MHz. To achieve wider bandwidth, one or more L-C components can be added to the reactance-compensation circuit. By adding one pair of inductor and capacitor in shunt to the reactance-compensation network, the double reactance-compensation network can be realized. One amplifier using the double reactance-compensation was developed to cover the whole UHF TV broadcasting band[14].

A schematic circuit diagram of the double reactance-reactance technique is shown in Fig. 1(a). Circuit elements are normalized to angular frequency $\omega_0 = 1$ with a load resistance of R = 1 Ω. The design technique and element values of the schematic can be found in [11] [14]. The calculated magnitude and phase of the impedance seen by the switch are shown in Fig. 1(b). It can be seen that a flat load angle has been achieved around the center frequency, which is required for wideband class-E operation.

The element values given in Fig. 1(a) are a starting point for circuit optimization in PA design. In practice, the transistor is far from an ideal switch at RF frequencies. The transistor can achieve high efficiency only when the drain is presented with a certain range of impedances, which can be found out by load-pull measurement or simulation. For the design of high efficiency broadband class-E PAs, the desired drain impedance is obtained by compromising the optimal impedance found by the load-pull measurement and the optimal impedance for

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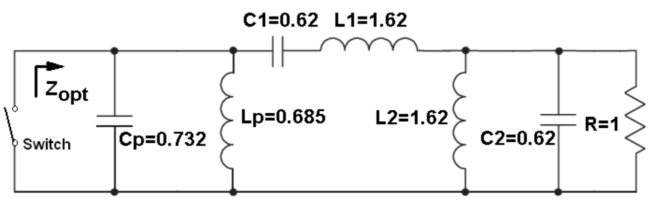
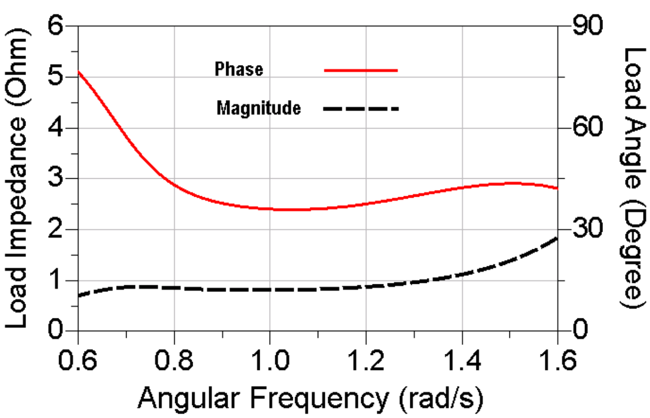
class-E operation as shown in Fig. 1(a).

One of the particular issues with high power amplifiers is that the magnitude of the optimal drain impedance is very low. For example, the magnitude of the optimal impedance of a typical high power LDMOS transistor is typically about 3 Ω to 6 Ω or even lower. As can be seen in Fig. 1(b), the value of the load resistance of R should be almost equal to the magnitude of the desired drain impedance. An additional resistance transformation network is needed to transform the usual 50 Ω load to the desired load resistance R_{opt} as shown in Fig. 1(c). In [6][7] [11], an additional two- or three-stage lowpass filter was added to transform the 50 Ω load to the desired low value resistance mentioned above. In [15], a transformer was used for this purpose.



(a)



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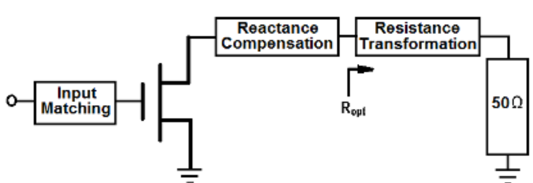


(c)

Fig. 1. (a) A schematic of the idealized double reactance compensation circuit with normalized circuit elements, (b) magnitude and phase of the impedance seen by the switch normalized to ω=1 rad/s and load R=1 Ω and (c) the block diagram of a broadband PA using the reactance compensation technique.

In this paper, a useful impedance transformation technique is introduced to improve the reactance-compensation network. By using the improved technique, without adding any more components, the desired load resistance can be four times the original value, while the flat load angle is maintained as shown in Fig. 1(b). As a result, the overall output matching network can be significantly simplified. Or by using the same number of components in the matching network, a much wider operational bandwidth can be achieved. The theory is validated by comparing the performances of two class-E amplifiers designed using the original and the proposed methods, respectively.

In this paper, the broadband impedance transformation technique is introduced in detail in section II. Section III describes how to design suboptimum class-E amplifiers using the proposed technique. The fabrication and experimental results are presented in section IV to verify the design. Finally future work and conclusions are drawn in section V.

II. Broadband Impedance Transformation

A. A Useful Impedance Transformation Network

A useful impedance transformation method has been introduced in [16] [17] [18]. With this method, a bandpass filter can be transferred into an impedance matching network. The method can be more generalized as shown in Fig. 2. The input impedance of the network shown in Fig. 2(a) and Fig. 2(b) can be given by

$$Z_{in\_a} = Z_a + \frac{1}{\frac{1}{Z_b} + \frac{1}{Z_L}} \tag{1}$$

$$Z_{in\_b} = \frac{1}{\frac{1}{Z_{bt}} + \frac{1}{Z_{at} + Z_{Lt}}} \tag{2}$$

respectively. It can be proven that, with any value of Z_a, Z_b and Z_L, the input impedance Z_{in} of the network shown in Fig. 2(a) and Fig. 2(b) will be equal to each other by choosing

$$n = \frac{Z_a}{Z_b} + 1 \tag{3}$$

$$Z_{bt} = nZ_b \tag{4}$$

$$Z_{at} = (n^2 - n)Z_b \tag{5}$$

$$Z_{Lt} = n^2 Z_L \tag{6}$$

where Z_a, Z_b, Z_L, Z_{at}, Z_{bt} and Z_{Lt} are defined in Fig. 2, and n^2 is the transformation ratio.

One very attractive aspect of this type of transformation is that, if n is a constant independent of frequency, the input impedance seen in Fig. 2(a) is identical to Fig. 2(b) at all frequencies. In a simple scenario, if both Z_a and Z_b are composed of a single inductor (or capacitor), respectively, n will be a constant value of the ratio of the inductances of the two inductors (or the reciprocal of the ratio of the capacitances). By choosing element values using (3)-(6), the two networks shown in Fig. 2 will have the same input impedance at all frequencies. By doing so, the value of Z_{Lt} is n^2 times of Z_L. This is very useful for impedance transformation because, while Z_{in} is the same at all frequencies, the value of Z_{Lt} is much higher than Z_L.

B. Broadband Impedance Matching

The impedance transformation method discussed in the last section is very useful for the design of high power amplifiers especially with LDMOS transistors because the magnitude of the optimal drain impedance of these amplifiers is usually very low. With this method, the optimal drain impedance can be transformed from a much higher load resistance.

This method can be easily applied to the reactance compensation network shown in Fig. 1(a). By taking C_1 as Z_a, C_2 as Z_b and R in parallel with L_2 as Z_L, the network can be transformed to the one shown in Fig. 3(a). In this case, n = 2 is a constant independent of frequency. The values of the elements in Fig. 3(a) can be obtained from (3)-(6). The impedance Z_{opt} seen by the switch, or the drain impedance, is identical to the network shown in Fig. 1(a) at any frequency. The only differences are the order and the values of the elements.

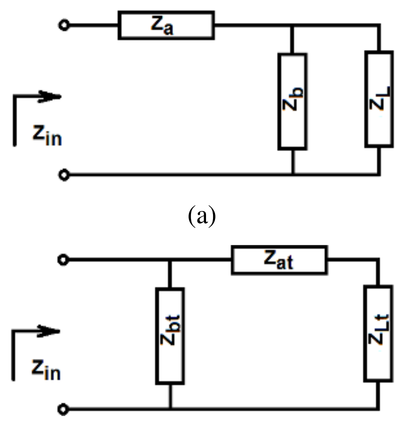


Fig. 2. Network (a) can be transformed to network (b), or vice versa, by properly choosing the values of circuit elements.

The impedance transformation network can be flexible. For example, by splitting L_1 in Fig. 1(a) into two 0.81 H inductors and using only one of the split inductors in the transformation, a constant value of n = 1.5 can obtained. The resultant network is shown in Fig. 3(b). The desired load resistance is transformed by a ratio of $n^2 = 2.25$. It is evident that the same method can be used to transform the desired load resistance to a lower value as well if necessary, by converting the network of Fig. 2(b) to Fig. 2(a).

The most useful aspect of this transformation is that the optimal impedance Z_{opt} is transformed from a load resistor of a much higher value. In this case n = 2, the optimal impedance is transformed from a load resistor of R = 4 rather than R = 1 in the original case as shown in Fig. 1(a). By using the method illustrated in Fig. 3(b), n could have any value between 1 and 2. In practical PA design, if the magnitude of the desired drain impedance is between 12.5 Ω and 50 Ω, the additional network required in the original design is no longer needed. If the magnitude of the desired impedance is lower than 12.5 Ω, the additional network is still needed. But since the optimal impedance can be transformed from a load resistance up to four times the magnitude, the matching network can be much more easily designed, because the resistance transformation ratio is now much smaller.

It is obvious that the proposed technique is not limited to the broadband class-E amplifier design discussed here. The technique can be used in many other applications where the transformation of load impedance is desired and the characteristics of the matching network need to be maintained.

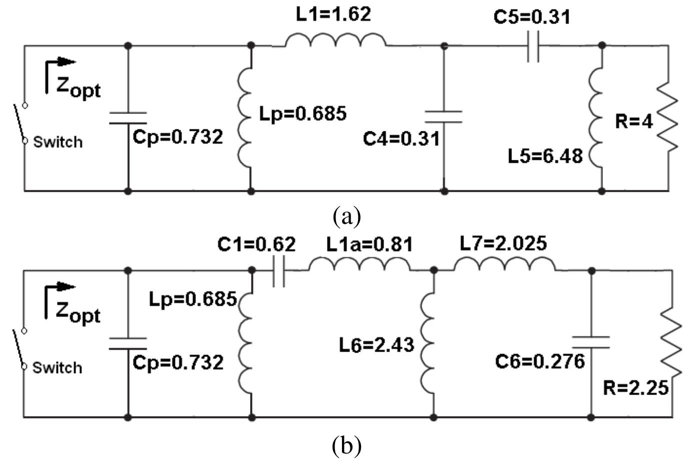


Fig. 3.(a) A schematic of the double reactance compensation network after applying the proposed impedance transformation technique, and (b) A smaller resistance transformation ratio can be obtained by "splitting" one of the circuit elements.

III. Broadband Suboptimum Class-E PA Design

In [14], a wideband class-E PA using a GaN transistor was developed to cover the whole UHF TV broadcasting band. Since the power density of GaN transistors is about 10 times larger than traditional transistors, the optimal drain impedance of GaN transistors is much higher than most other types of transistors [19], which makes the impedance matching easier.

At UHF frequencies, LDMOS transistors are a good candidate for the development of high power amplifiers. To reduce cost and improve reliability, another PA using LDMOS transistors is developed which can cover the UHF broadcast band from 470 MHz to 750 MHz. The PA should be able to deliver an output power of 10 W with a power added efficiency (PAE) of above 70%. The linearity of this PA can be improved by an envelope modulator in an envelope tracking or envelope elimination and restoration topology and further improved by digital pre-distortion, which is not the topic of this paper. To deliver the same output power, the LDMOS transistors usually have a much lower drain impedance than GaN transistors. It will be shown below how the proposed technique can be used to simplify the PA design using LDMOS transistors.

A BLF642 from NXP is an LDMOS RF power transistor for broadcast transmitter and industrial applications. The excellent ruggedness and broadband performance of this device make it ideal for applications in digital TV transmitters. The BLF642 was chosen to develop the PA.

The BLF642 can deliver an average output power of P_{OUT} = 35 W under the nominal drain supply voltage of V_{DS} = 32 V. The output capacitance of the transistor is $C_{OUT} = C_{DG} + C_{DS}$ = 15.84 pF according to the datasheet. The maximum switching frequency of the transistor can be estimated by [10]

$$f_{max} = 0.0798 \frac{P_{OUT}}{C_{OUT} {V_{DC}}^2} = 172 \text{ MHz} \tag{7}$$

This frequency is much lower than the highest frequency of interest. It was therefore necessary to design the PA in suboptimum Class-E operational mode [20], rather than the

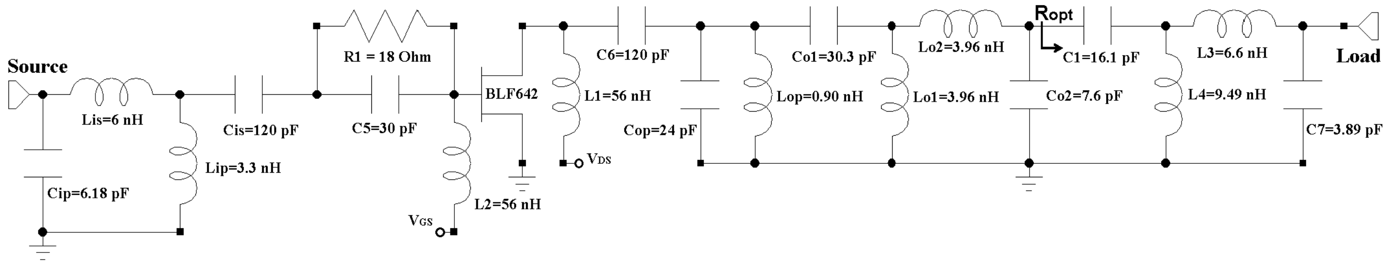


Fig. 4. A schematic of the wideband class-E PA using the improved reactance-compensation technique.

nominal class-E mode. The design of suboptimum class-E PA is described in detail in [10][20]. The suboptimum class-E PA can achieve high efficiency well above f_{max}. Another advantage of the suboptimum class-E is that the ratio of the peak drain voltage to V_{DC} can be much lower than that of the nominal class-E of 3.56.

On the other hand, at RF and microwave frequencies, the PA can achieve high efficiency only when the transistor is presented with an appropriate load impedance. To design the PA, a load-pull simulation using ADS from Keysight Technologies with the circuit model provided by the transistor manufacturer was carried out to find the optimum impedances for the transistor to achieve the highest PAE at different frequencies. The results are summarized in TABLE I. It can be seen that the magnitude of the optimum impedances is around 6 Ω. It can be found from Fig. 1(b) that the corresponding load resistance desired is close to the magnitude of the optimum impedance, and is also about 6 Ω.

TABLE I OPTIMUM IMPEDANCES COMPARED WITH THE REALIZED VALUES FOR THE BLF642 TO ACHIEVE HIGH PAE AT UHF FREQUENCIES.

F (MHz)	Optimum Impedance (Ω)	Realized Impedance (Ω)
470	3.1 + j5.5	2.3 + j5.6
550	3.3 + j5.0	3.2 + j4.2
650	3.4 + j4.6	2.6 + j4.2
750	3.5 + j3.8	2.2 + j4.8

In the previous design [14], the magnitude of the optimal resistance for the GaN resistor is around 34 Ω, which is very close to the usual load resistance of 50 Ω. It has been shown in [14] that an additional resistance transformation network is not necessarily needed for the PA to cover the whole UHF broadcast band.

In this case, if the original reactance compensation network shown in Fig. 1(a) were used, an additional resistance transformation network would be needed to transfer the usual 50 Ω load to the desired load resistance of 6 Ω first. Then by using the double reactance-compensation network shown in Fig. 1(a), the 6 Ω resistance can be transformed to an optimal impedance to design the wideband PA.

The optimal impedance is the compromised value of the impedance for ideal class-E operation and the optimum impedance obtained in the load-pull simulation, as given in TABLE I. The impedances are optimized in such a way that the PA can achieve high efficiency when the output power is 10 W over the frequency band of interest.

By using the proposed network as illustrated in Fig. 3(a), where n = 2, the additional network needed only to transform the 50 Ω to 24 Ω. Although an additional network is still needed, such an additional network is much easier to design because the transformation ratio is much lower.

Traditionally in [6][7] [11], a two- or three-stage lowpass filter was used to transform the 50 Ω load to a lower-value resistance. This can also be realized using a bandpass filter [17][18]. It is indicated in [21] that efficient impedance matching networks are necessarily bandpass filter structures. To design the resistance transforming network, a bandpass filter is firstly synthesized [22]. After applying the transformation technique shown in Fig. 2, the bandpass filter can be transformed to a resistance matching network. By properly choosing filter types, in-band ripple and bandwidth of the filter, it is always possible to match 50 Ω to any desired lower value [17].

A two-stage/resonator resistance transforming network was used to transform the 50 Ω load to the desired load resistance of 24 Ω. This network is cascaded with the impedance matching network shown in Fig. 3(a) to construct the whole output matching network as shown in Fig. 4.

For the PA to achieve high efficiency, it is important to realize the output impedance close to the values given in TABLE I. The realized load angles using the original reactance-compensation method and the proposed method are shown in Fig. 5(a), compared with the optimum values. It can be seen that the proposed method can achieve good performance in a much wider frequency band.

The component values after optimization in ADS are also shown in Fig. 4. The components C_7, L_3, L_4 and C_1 transform the 50 Ω load to the optimal resistance R_{opt} as shown in Fig. 4. The double reactance-compensation network composed of C_{op}, L_{op}, C_{o1}, L_{o1}, C_{o2} and L_{o2} transform the optimal resistance R_{opt} to the optimal drain impedance across the band of interest.

The input matching network is less critical and was realized in a similar way to achieve wideband performance. A source-pull simulation was carried out to obtain the optimum impedances at different frequencies. For the input matching network, there is no need to consider the load angle as in the output matching network. A second-order bandpass filter was designed to transform 50 Ω to the optimum impedances. The same technique as shown in Fig. 2 was used to realize the impedance transformation. The resultant input matching network is shown in Fig. 4. A resistor R_1 and a capacitor C_5 in parallel are used at the gate to stabilize the PA. The simulated return loss of the PA is shown in Fig. 5(b). It can be seen that reasonably good input loss was realized over the frequency band of interest. In the design, the input matching network was optimized for high efficiency across the band of interest.

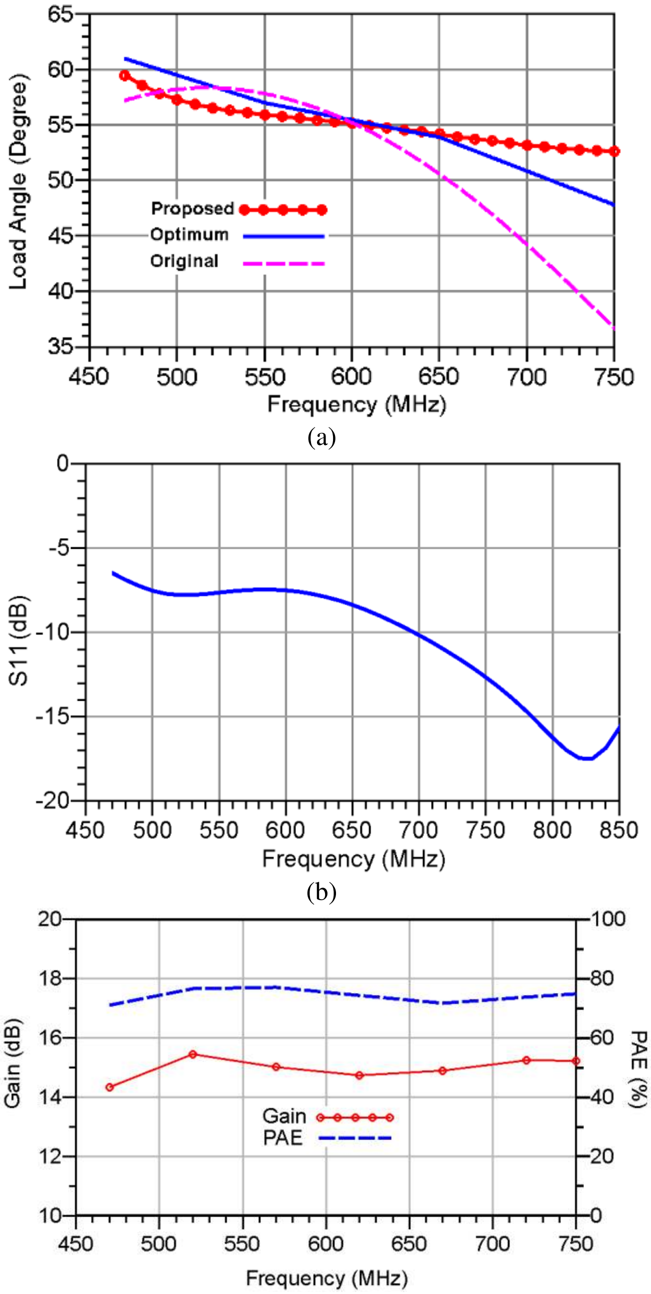


Fig. 5. (a) Simulated load angles achieved by using the original and the proposed double reactance-compensation method compared with the optimum values obtained by load-pull simulation., (b) Simulated S_{11} of the PA, and (c) Simulated gain and PAE of the PA across the frequency band of interest after optimization with V_{DC} = 16 V.

It should be noted that for three major reasons the output matching networks needed further optimization. The first is that the input impedance of the resistance matching network is not purely resistive. This input impedance is composed of the desired R_{opt} as shown in Fig. 4 and a small value of reactance. The whole matching network needs to be tuned to minimize the effect of this small residue reactance.

The second reason is that, as mentioned above, the phases of the optimum impedances in TABLE I are different from the ideal values for the broadband reactance-compensation class-E design specified in [10]. In the PA design process, it was necessary to tune the output matching network by compromising the optimal impedances for broadband class-E operation as specified in Fig. 3(a) and the optimal impedances obtained by load-pull simulation shown in TABLE I. It was also necessary to tweak the matching networks to trade off efficiency with other PA performance parameters such as the gain and the output power. Especially, in this application, it is desired for the PA to achieve high efficiency when the output power is around 10 W across the required frequency band.

The third reason is that the circuit model provided by the manufacturer also includes the effects of the package, which could potentially violate the suboptimum class-E operation. The intrinsic and extrinsic parameters of the package can be estimated and taken into consideration in the design [23][24]. It was found the output capacitance was the dominating factor. In the design, it was necessary to cut short the pins of the transistor package to the minimum lengths as shown in Fig. 6(a). In particular, the capacitor C_{op} has a value of 3.0 pF after optimization, instead of 24 pF as shown in Fig. 4.

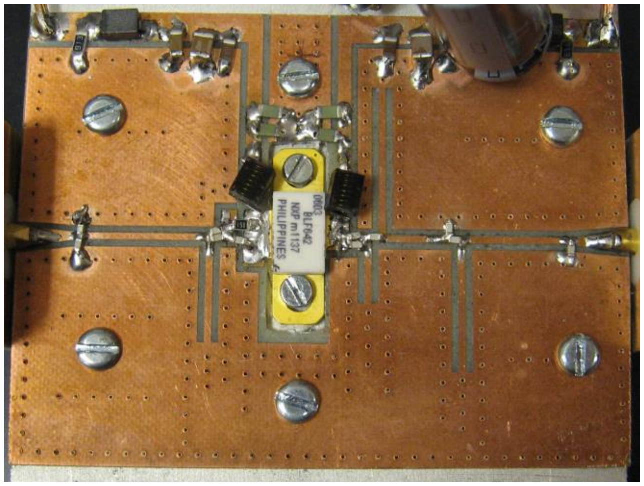
When constructing the PA, lumped-element capacitors were used in the circuit. The MuRata GRM615 series capacitors were used in the design. All of the inductors in the matching networks were realized by coplanar transmission lines with a ground plane on the other side of the PCB as shown in Fig. 6(a). The circuit was designed on a GML 1000 substrate with a thickness of 1.57 mm. The line width of the transmission lines to realize inductors is 0.8 mm, the gap between the line and the ground planes on the same side is also 0.8 mm. The required length L_L to realize each inductor can be calculated by [22]

$$L_L = \frac{\lambda_g}{2\pi}\sin^{-1}\frac{\omega_0 L}{Z_0} \tag{8}$$

where λ_g is the wavelength of the transmission line at the centre frequency ω_0, $Z_0 = 92\ \Omega$ is the characteristic impedance of the transmission line, and L is the inductance to be realized. Small through-pins were added to connect the ground planes on the same side of the lines with the ground plane on the other side of the substrate. The lengths of the transmission lines were first estimated using (8) and then further optimized in ADS.

The simulated PAE and gain of the PA after optimization across the frequency band of interest are shown in Fig. 5(c). The PAE is better than 70% throughout and the gain is better than 14 dB. The DC supply voltage V_{DC} = 16 V is assumed in the simulation.

The simulated drain voltage and drain current waveforms at 600 MHz and 750 MHz are shown in Fig. 7(a) and Fig. 7(b), respectively. It can be seen the PA operates in close-form class-E modes at these frequencies. In these simulation results, the DC supply voltage is assumed to be V_{DC} = 25 V. This is the highest voltage needed for the PA to deliver 10 W output power over the frequency band of interest, to be discussed in more detail in the next section.



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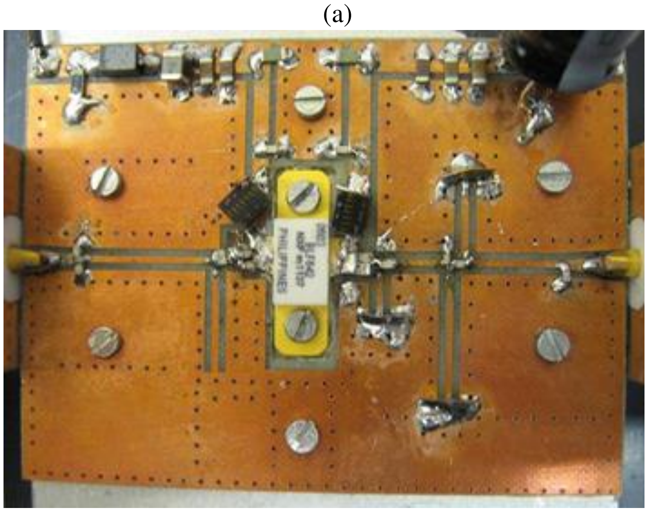

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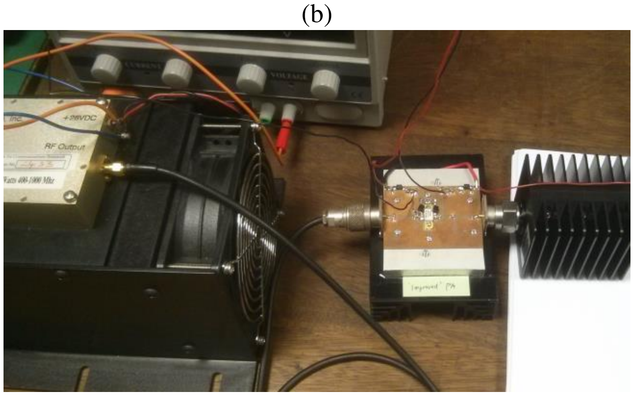
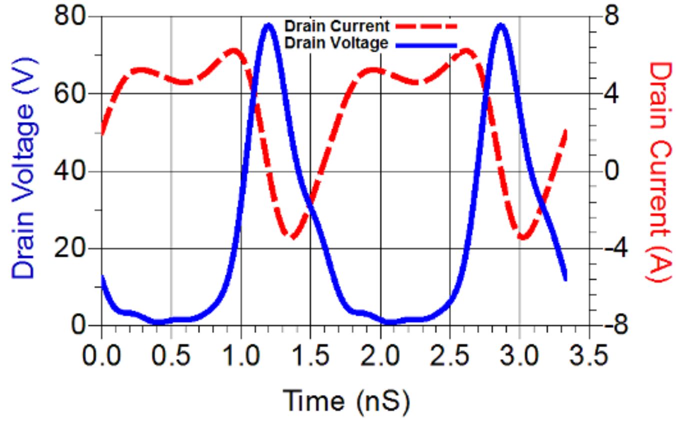


(c)

Fig. 6. A photograph of the fabricated broadband class-E PA designed (a) using the improved reactance-compensation technique and (b) a PA designed using the original technique, and (c) the measurement set-up.

The breakdown voltage of the transistor is 65 V. It can be seen that at 750 MHz, the highest drain voltage is lower than this value. Although the simulated drain voltage is higher than 65 V at 600 MHz, it will be shown in the next section that a DC supply voltage of 15 V is needed to deliver the specified output power of 10 W. The drain voltage is therefore much lower than 65 V. In fact, the PA has been tested with a pulsed input signal under V_{DC} = 30 V. The input signal was a square wave having a duty ratio of 10% and a period of 40 µs. No damaging effect to the transistor has been observed in the test.



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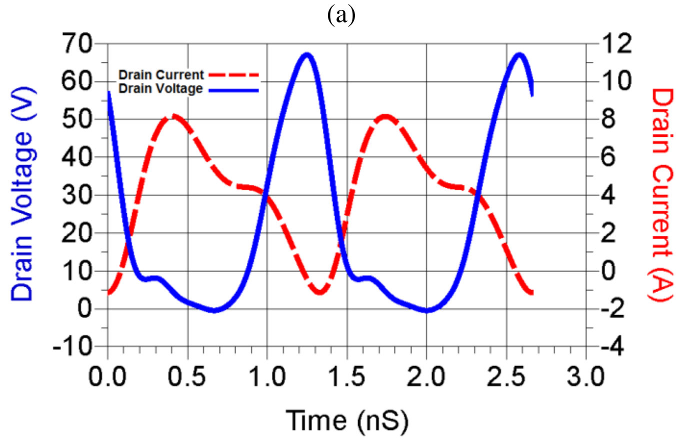


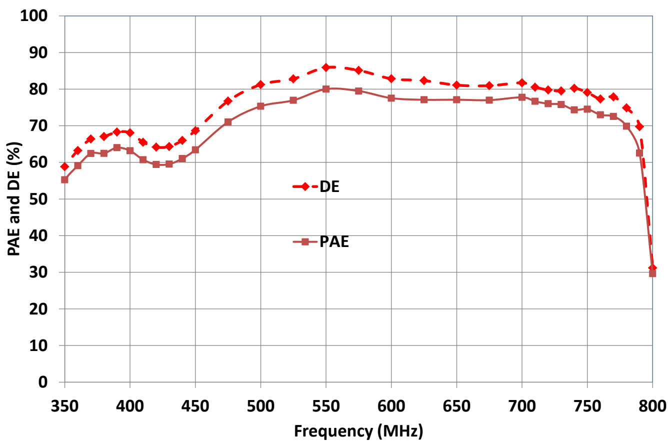
(b)

Fig. 7. Simulated drain voltage and drain current waveforms of the wideband PA at (a) 600 MHz and (b) 750 MHz.

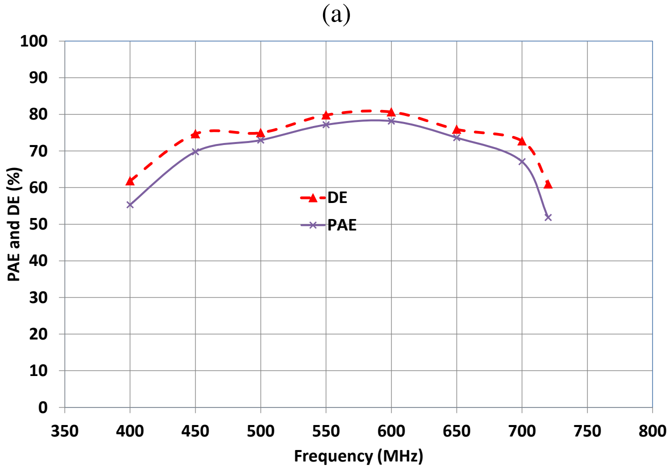
IV. Experimental Results

The circuit was fabricated on a GML 1000 laminate with a thickness of 1.57mm. A hole was made in the PCB to accommodate the LDMOS transistor. The PCB and the transistor were mounted on an aluminum base and the base was attached to a heatsink. A photograph of the assembled circuit is shown in Fig. 6(a). The measurement set-up is shown in Fig. 6(c). A buffer amplifier was used to boost the power level of the input signal from the RF signal generator. The output signal from the PA is attenuated by attenuators before being fed into a spectrum analyzer to observe the output spectrum. To measure the output power more accurately, a power meter was used to replace the spectrum analyzer for the power reading.

The measured drain efficiency (DE) and PAE of the PA is shown in Fig. 8(a). In the measurement, the output power was kept constant at 10 W. It can be seen that the PAE is up to 80%. The maximum PAE is better than 85% when the output is higher than 10 W. The PA can achieve a PAE of better than 60% for the frequency band of 360 MHz to 790 MHz, a fractional bandwidth of 81%. Or, the PAE can be better than 70% for the frequency band of 470 MHz to 780 MHz, a fractional bandwidth of 51%. The achieved efficiency is in good agreement with the simulation shown in Fig. 5(c). The measured bandwidth and efficiency are comparable to those PAs designed with GaN transistors in [13] and [14].



(a)



(b)

Fig. 8. (a) Measured PAE and drain efficiency of the wideband class-E PA designed using the improved reactance-compensation technique and (b) measured PAE and drain efficiency of the wideband class-E PA designed using the original technique. The output power is 10 W for all measurements.

The measured performance of the proposed PA is compared with other state-of-the-art wideband PAs that can achieve greater than 70% PAE. It can be seen that this work has achieved comparable performance with other PAs. It should be pointed out the performance of the proposed PA was measured under the condition that the output power is the constant value of 10 W as specified. Although the PA was expected to cover the broadcast band of 470 MHz to 750 MHz, the system bandwidth required is 8 MHz. The supply voltage was chosen at each frequency so that the maximum output power is about 10 W. The measured PAE, gain and output power can be much greater if a higher DC supply voltage is used at each frequency.

The measured output power, PAE and gain as a function of the input power at 600 MHz are shown in Fig. 9(a). In this measurement, V_{DC} = 15 V was chosen so that the PA can achieve high efficiency at the specified output power level. The gain is very flat when the input power varies between 14 dBm and 27 dBm, the corresponding output power is 0.4 W (27 dBm) to nearly 10 W (40 dBm).

The DC power supply voltage used at each frequency and the corresponding gain are shown in Fig. 9(b). It can be seen that the gain is reasonably flat over the frequency band. The gain is slightly higher at high frequencies, mainly because the DC supply voltage used is a little higher. The DC supply voltage is around 16 V in general. The lowest required voltage is 12 V at 470 MHz and the highest is 25 V at 750 MHz. The PA was biased at class-B conditions with V_{GS} = 1.95 V.

TABLE II STATE-OF-THE-ART BROADBAND PAS WITH PAE>70%

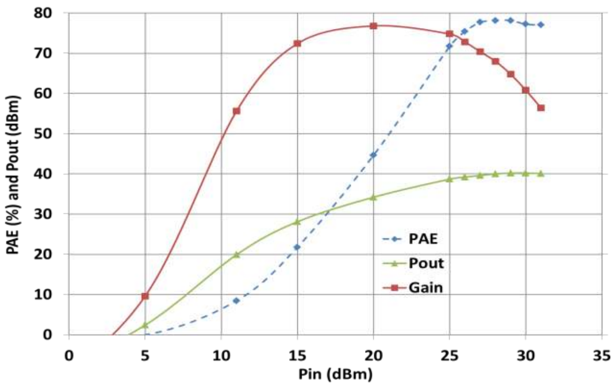
Reference	Frequency (MHz)	FBW (%)	Pout (W)	PAE_{Peak} (%)	Notes
2008[11]	155	25	9	74	Class-E
2009[3]	715	35	49	81	Class-E
2011[25]	1500	53	20	81	Class-E
2011[26]	710	52	13	74	Class-F
2013[14]	590	41	10	78	Class-E
2013[13]	1170	45	180	81	Class-E
This work	605	51	10	80	Class-E

TABLE III COMPARISON OF THE MEASURED PERFORMANCE OF THE TWO PAS

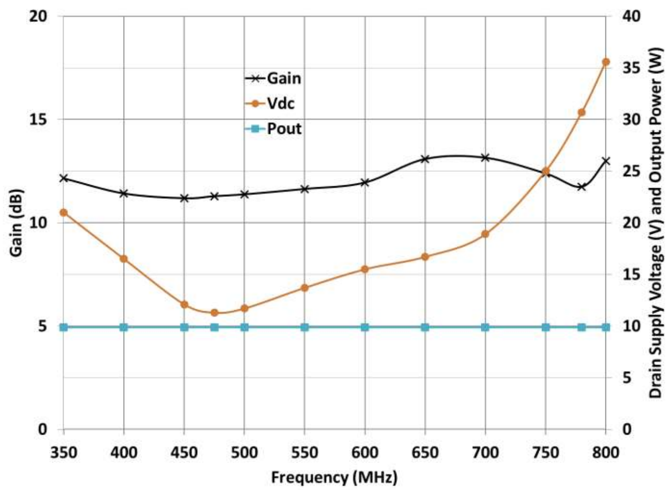
	Original PA	Proposed PA
>70% PAE Freq. Band (MHz)	450-680	470-780
>70% PAE bandwidth	42%	51%
>60% PAE Freq. Band (MHz)	420-710	360-790
>60% PAE bandwidth	53%	81%

The realized impedances of the output matching network at different frequencies are shown in TABLE I, compared with the optimum impedance obtained from load-pull simulation. However, while the impedances of the passive matching network are usually constant, the optimum impedances of the transistor do change with the drain supply voltage. Fig. 9(c) shows the measured performance of the PA when the drain supply voltage is fixed to be V_{DC} = 16 V, under which condition the optimum impedances were obtained by simulation, as shown in TABLE I. It can be seen that high efficiency and gain achieved are in good agreement with the simulation results shown in Fig. 5(c). The output power is lower than the specified value of 10 W (40 dBm). This is can be improved by using a high DC drain supply voltage as shown in Fig. 9(b).

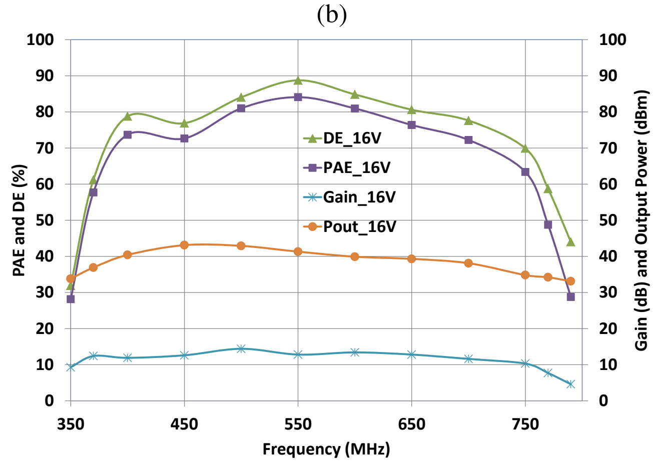
For comparison, the same transistor was used to design another broadband PA using the original reactance compensation technique shown in Fig. 1(a) and the same type of two-stage resistance transformation network as shown in Fig. 4. In this case, the resistance transformation network had to transform the 50 Ω load to the desired load resistance of 6 Ω. Following the same design and optimization process, the manufactured PA is shown in Fig. 6(b). It can be seen that the area of the PCB and the complexity of the matching networks of the two PAs are quite similar. The losses of the matching networks are also expected to be very similar.



(a)



(b)



(c)

Fig. 9. (a) Measured output power P_{out}, PAE and gain as a function of the input power at 600 MHz with different input power levels, (b) Measured power and gain of the proposed PA. It was necessary to change the drain supply voltage V_{DC} across the frequency band of interest to achieve an output power of 10 W, and (c) measured drain efficiency, PAE, gain and output power of the PA when V_{DC} is fixed to be 16 V.

The measured performance of the PA designed with the original reactance compensation technique is shown Fig. 8(b). It can be seen that the PA could achieve better than 60% PAE only over a frequency band of 420 MHz to 710 MHz, or better than 70% PAE over the frequency band of 450 MHz to 680 MHz. The fractional bandwidth is 42%, significantly lower than the PA designed with the proposed technique as discussed above. The measured gain is below 3 dB and the PAE is less than 10% at 350 MHz and 800 MHz, respectively. The comparison is summarized in TABLE III. It was estimated by calculation that a four- or five-stage resistance transformation would be needed for this PA to achieve a similar bandwidth as shown in Fig. 8(a).

V. Conclusion

This paper has proposed ways to improve the reactance compensation technique to design high power amplifiers. This is achieved by changing the values and the order of components used in the traditional technique. Using the original technique, an additional resistance transformation network is usually needed to transform the 50 Ω to a lower-value resistance. With the improved technique, the additional network will be no longer needed if the magnitude of the desired drain impedance is between 12.5 Ω and 50 Ω. Even if the additional network is still needed, design of such a network will be significantly simplified, as a much lower impedance transformation ratio is required.

To validate the theory, two PAs using the original method and the proposed technique are designed, respectively, and compared. It has been shown that, by using matching networks of similar complexity, the PA designed with the original matching network can achieve a PAE of better than 70% across a fractional bandwidth of 42%, while the PA designed with the proposed technique can achieve better than 70% PAE over a significantly increased bandwidth of 51%. In future work, the proposed technique will be further improved to realize a greater ($n^2 > 4$) transformation ratio.

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