Improved Small-Signal Equivalent Circuit Model and Large-Signal State Equations for the MOSFET/MODFET Wave Equation

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***Abstract*—A simple non-quasi-static small-signal equivalent circuit model is derived for the ideal MOSFET wave equation within the gradual channel approximation. This equivalent circuit represents each *Y*-parameter by its dc small-signal value shunted by a (trans)capacitor in series with a charging (trans)resistor. The resistor and capacitors are selected such that the resulting *Y*-parameters admits the correct frequency power-series expansion. The resulting small-signal model admits a graceful degradation outside its frequency range of validity. When compared with the exact solution this first-order *RC* equivalent circuit is demonstrated to be valid at higher frequencies than the second-order frequency-power series or even second-order iterative solutions of the MOSFET equation. A large-signal model for the intrinsic MOSFET is derived by first implementing this *RC* topology in the time domain. Modified state equations similar to ones recently reported are then introduced to enforce charge conservation. Transient simulations with this approximate large-signal model yields results which compare with reported exact numerical analysis for the long-channel MOSFET for a wide range of bias conditions. This unified small- and large-signal model applies to both the three- and four-terminal intrinsic MOSFET in the region of the channel where the gradual channel approximation is applicable. A non-quasi-static small-signal equivalent circuit for the velocity-saturated MOSFET wave equation is also reported.**

Nomenclature

C_g	$= \epsilon_2/d$, the gate capacitance per unit area.
d	Width of the oxide or high-bandgap region.
d_s	Channel width in the saturation region.
ϵ_1	Dielectric constant for the channel material.
ϵ_2	Average dielectric constant for the high-bandgap or oxide region.
q	Electron charge.
L_g	Gate length.
μ	Channel mobility.
V_T	Threshold voltage.
$V_{CS}(x)$	DC channel-to-source voltage at position x.
$v_{GC}(x)$	Instantaneous gate-to-channel voltage at position x.
$V_{GC}(x)$	DC gate-to-channel voltage at position x.
$v_{gc}(x)$	AC gate-to-channel voltage at position x.
v_{GS}	Instantaneous applied voltage between the gate and the source.
V_{GS}	DC applied voltage between the gate and the source.
v_s	Saturation velocity of electrons.
v_{gs}	AC applied voltage between the gate and the source.
v_{bs}	AC applied voltage between the substrate and the source.
v_{DS}	Instantaneous applied voltage between the drain and the source.
V_{DS}	DC applied voltage between the drain and the source.
v_{ds}	AC applied voltage between the drain and the source.
W_g	Gate width.

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I. Introduction

With the recent development of submicrometer gate technology there has been a revival of interest in developing analytic non-quasi-static small- and large-signal models for the MOSFET and MODFET holding to high frequencies compared to the unity current gain cutoff frequencies f_T. Because f_T is bias-dependent, even at low frequencies experimental data [1] point to the importance and the need for non-quasi-static modeling in conventional analog circuits.

Several of the high-frequency models [2]–[6] recently reported for the long and short channel, three- or four-terminal MOSFET rely on the MOSFET wave equation [7]–[9]

$$\frac{\partial^2 V^2(x, t)}{\partial x^2} = \frac{2}{\mu} \frac{\partial V(x, t)}{\partial t}.$$

Note that the MOSFET wave equation is based on the gradual channel approximation and is therefore only used in the region of the FET channel where the gradual channel approximation holds. For the three-terminal MOSFET the voltage V is simply $v_{GC} - V_T$. See [2] for the definition of V in the case of the four-terminal MOSFET.

For small-signal excitation the MOSFET wave equa-

tion reduces to

$$\frac{d^2}{dx^2}\left[V_0(x)\, v(x,\omega)\right] = j\frac{\omega}{\mu} v(x,\omega)$$

with $V_0(x) = V_{GC}(x) - V_T$ (see [5]).

An exact solution of the small-signal MOSFET equation was obtained in terms of Bessel functions for $k = 1$ by Burns [14] (for all k see [5]). Simple approximate solutions suitable for circuit simulation have also been reported. Small-signal Y-parameters holding up to high frequencies can be obtained using the frequency power series introduced by Van Der Ziel [10]

$$Y_{ij} = g_{ij} + j\omega\alpha_{ij} + (j\omega)^2\beta_{ij} \tag{1}$$

where g_{ij} are the dc Y-parameters [4], [11].

An alternate procedure based on an iterative scheme was introduced by Van Nielen [13] to obtain accurate approximate results of the MOSFET wave equation. Conducted up to second order, the iterative procedure yields for the three-terminal MOSFET/MODFET, small-signal Y-parameters of the following form:

$$Y_{ij} = \frac{g_{ij} + j\omega a_{ij} + (j\omega)^2 b_{ij}}{1 + j\omega c_{ij} + (j\omega)^2 d_{ij}}. \tag{2}$$

The same Y-parameters can also be obtained by expanding the Bessel functions in a frequency power series in the exact solution of the small-signal MOSFET wave equation. This iterative solution was used by Bagheri and Tsividis [2] and Bagheri [3] for deriving the small-signal Y-parameters of the long-channel four-terminal MOSFET and three-terminal MOSFET/MODFET, respectively. The small-signal Y-parameters obtained by an iteration of order two admit a frequency power-series expansion valid up to power two. These iterative Y-parameters hold for higher frequencies and have the advantage of providing a more graceful degradation outside their frequency range of validity compared to the Y-parameters obtained by the frequency power series [3].

Several transient analyses of the large-signal MOSFET wave equation have also been reported [15], [16], and [19]. These methods are not however suited for circuit simulation. Chai and Paulos [6] recently extended the application of the iterative technique to the large-signal MOSFET wave equation and derived simple approximate state equations for the four-terminal MOSFET which are suitable for circuit simulation.

In this paper we will show that a simple *RC* equivalent circuit representation of the frequency power-series Y-parameters also admits a graceful degradation and is valid for higher frequencies than the second-order iterative Y-parameters. We will use this *RC* model to develop a simple large-signal model in Section V which closely resembles the one reported in [6]. We will establish the limitations and capabilities of this simple large-signal model using several transient experiments. We will demonstrate in Section VI that this large-signal model enforces charge conservation and will compare it to the Chai and Paulos model in Section VII. We will consider in Section VIII alternate equivalent circuits, discuss the physical basis for the *RC* equivalent circuit, and will state in Section IX the requirements for the optimal second-order *RC* model. We will demonstrate in Section X that the unified small- and large-signal model presented applies to both the three- and four-terminal MOSFET wave equations. Finally, we will present in Section XI an extension of this non-quasi-static small-signal equivalent circuit to the velocity-saturated MOSFET wave equation

II. Normalized Long-Channel Y-Parameters

Consider the small-signal Y-parameters of the MOSFET in the common-source configuration

$$i_g = Y_{gg}(\omega)\, v_{gs} + Y_{gd}(\omega)\, v_{ds}$$

$$i_d = Y_{dg}(\omega)\, v_{gs} + Y_{dd}(\omega)\, v_{ds}.$$

One can easily verify that the exact small-signal Y-parameters obtained from the MOSFET wave equation can be written in terms of dimensionless parameters

$$\frac{Y_{ij}}{g_0} = f_{ij}\left(k, \frac{\omega}{\omega_0}\right)$$

with $k = V_{DS}/(V_{GS} - V_T)$, with g_0 the channel conductance

$$g_0 = \frac{\mu C_g W_g (V_{GS} - V_T)}{L_g}$$

and with ω_0 a normalization frequency given by

$$\omega_0 = 2\pi f_0 = \mu\frac{(V_{GS} - V_T)}{L_g^2}.$$

This normalization can also be applied to the frequency-power-series solution given in [4]. These approximate Y-parameters can then be rewritten in the following normalized fashion:

$$\frac{Y_{gg}}{g_0} = j\frac{\omega}{\omega_0}\mathfrak{I}_{gg}(k) + \left(\frac{\omega}{\omega_0}\right)^2 \mathfrak{R}_{gg}(k)$$

$$\frac{Y_{gd}}{g_0} = -j\frac{\omega}{\omega_0}\mathfrak{I}_{gd}(k) - \left(\frac{\omega}{\omega_0}\right)^2 \mathfrak{R}_{gd}(k)$$

$$\frac{Y_{dg}}{g_0} = k - j\frac{\omega}{\omega_0}\mathfrak{I}_{dg}(k) - \left(\frac{\omega}{\omega_0}\right)^2 \mathfrak{R}_{dg}(k)$$

$$\frac{Y_{dd}}{g_0} = (1-k) + j\frac{\omega}{\omega_0}\mathfrak{I}_{dd}(k) + \left(\frac{\omega}{\omega_0}\right)^2 \mathfrak{R}_{dd}(k).$$

The coefficients $\mathfrak{R}_{ij}$ and $\mathfrak{I}_{ij}$ are given in [4] except for an error in $\mathfrak{R}_{dd}$ which is corrected both in [5] and [17]. The existence of a normalized representation is useful as it permits one to establish results which are device-independent. This property is used in Section IV to study the range of validity of the equivalent circuit model proposed.

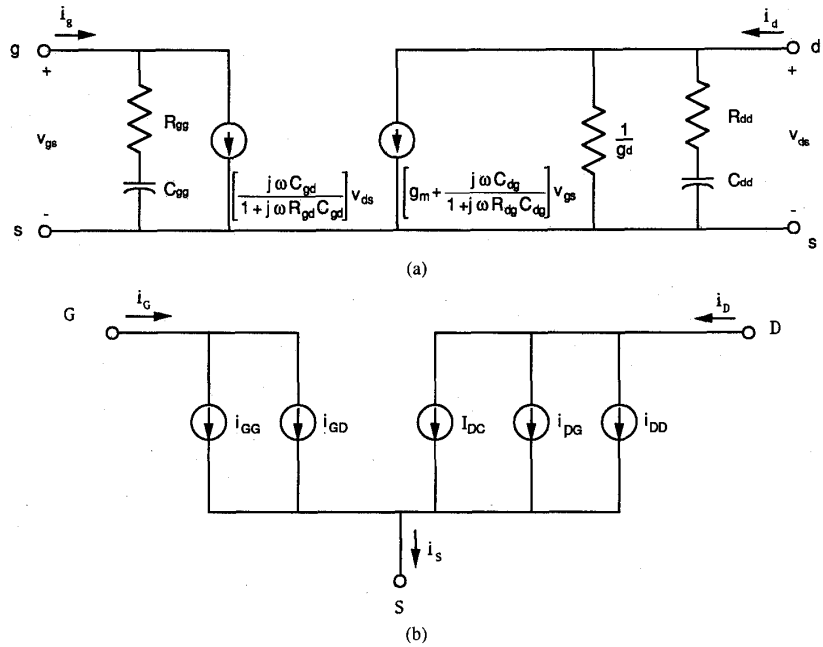


Fig. 1. Approximate small-signal (a), and large-signal (b) equivalent circuits for the intrinsic MOSFET.

III. A Simple *RC* Equivalent Circuit Representation

To provide a graceful degradation of the *Y*-parameters for frequencies ω larger than ω_0 we shall introduce a simple *RC* equivalent circuit model. The physical meaning of this model will be discussed in Section VIII. The *RC* model selected consists of the dc ($\omega = 0$) small-signal parameters g_{ij} shunted by a capacitor C_{ij} in series with a charging resistor R_{ij}. The resulting intrinsic *Y*-parameters are

$$Y_{gg} = \frac{j\omega C_{gg}}{1 + j\omega R_{gg} C_{gg}}$$

$$Y_{gd} = \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}}$$

$$Y_{dg} = g_m + \frac{j\omega C_{dg}}{1 + j\omega R_{dg} C_{dg}}$$

$$Y_{dd} = g_d + \frac{j\omega C_{dd}}{1 + j\omega R_{dd} C_{dd}}.$$

The associated equivalent circuit for the intrinsic MOSFET is shown in Fig. 1(a). For frequencies $\omega \ll 1/(R_{ij} C_{ij})$ these *Y*-parameters admit the frequency-power series (1)

$$Y_{ij} = g_{ij} + j\omega C_{ij} + \omega^2 R_{ij} C_{ij}^2. \tag{3}$$

We can now readily identify the resistors and capacitors to be

$$C_{gg} = \frac{g_0(V_{GS})\, \mathcal{G}_{gg}(k)}{\omega_0} \qquad R_{gg} = \frac{\mathcal{R}_{gg}}{g_0(V_{GS})\, \mathcal{G}_{gg}^2(k)}$$

$$C_{gd} = -\frac{g_0(V_{GS})\, \mathcal{G}_{gd}(k)}{\omega_0} \qquad R_{gd} = -\frac{\mathcal{R}_{gd}}{g_0(V_{GS})\, \mathcal{G}_{gd}^2(k)}$$

$$C_{dg} = -\frac{g_0(V_{GS})\, \mathcal{G}_{dg}(k)}{\omega_0} \qquad R_{dg} = -\frac{\mathcal{R}_{dg}}{g_0(V_{GS})\, \mathcal{G}_{dg}^2(k)}$$

$$C_{dd} = \frac{g_0(V_{GS})\, \mathcal{G}_{dd}(k)}{\omega_0} \qquad R_{dd} = \frac{\mathcal{R}_{dd}}{g_0(V_{GS})\, \mathcal{G}_{dd}^2(k)}.$$

The time constants $\tau_{ij} = R_{ij} C_{ij}$ appearing in the small-signal *Y*-parameters are then given by

$$\tau_{gg} = R_{gg} C_{gg} = \frac{1}{\omega_0} \frac{60 - 120k + 81k^2 - 21k^3 + 2k^4}{15(2-k)^3(6 - 6k + k^2)}$$

$$\tau_{gd} = R_{gd} C_{gd} = \frac{1}{\omega_0} \frac{30 - 41k + 16k^2 - 2k^3}{15(2-k)^3(3-k)}$$

$$\tau_{dg} = R_{dg} C_{dg} = \frac{1}{\omega_0} \cdot \frac{600 - 1440k + 1290k^2 - 540k^3 + 110k^4 - 9k^5}{30(2-k)^3(30 - 45k + 20k^2 - 3k^3)}$$

$$\tau_{dd} = R_{dd} C_{dd} = \frac{1}{\omega_0} \frac{320 - 560k + 340k^2 - 90k^3 + 9k^4}{30(2-k)^3(20 - 15k + 3k^2)}.$$

To demonstrate the graceful degradation provided by this equivalent-circuit representation we have plotted in Fig. 2 the magnitude (Fig. 2(a)) and phase (Fig. 2(b)) of Y_{gg}/g_0 for $k = 0.65$, obtained with the *RC* equivalent circuit (dashed-dotted line, *EQ*), the exact solution (plain line, *EXACT*), the frequency power series (dashed line,

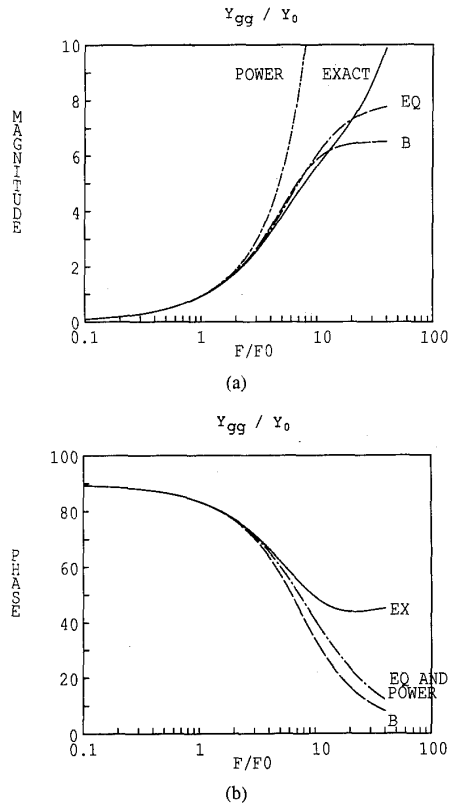


Fig. 2. Comparison of the amplitude (a) and phase (b) of Y_{gg}/g_0 for $k = 0.65$, obtained with the *RC* equivalent circuit (dashed-dotted line, *EQ*), the exact solution (plain line, *EXACT*), the frequency power series (dashed line, *POWER*), and the second-order iterative *Y*-parameters reported in [3] (dashed line, *B*).

POWER), and the second-order iterative *Y*-parameters derived in [3] (dashed line, *B*).

IV. Range of Validity of the *RC* Small-Signal Model

We wish now to establish the range of validity of the *RC* circuit representation introduced above for all bias conditions. For this purpose we have calculated for each parameter Y_{ij} the frequency $f_{5\%}(Y_{ij})$ for which an error Err (Y_{ij}) of 5% is obtained between the exact Bessel solution (see for example [5]) and the approximate results. The error Err (Y_{ij}) is

$$\text{Err}\,(Y_{ij}) = \frac{|Y_{ij}(\text{exact}) - Y_{ij}(\text{approximate})|}{|Y_{ij}(\text{exact})|}.$$

For the sake of comparison we have plotted in Fig. 3, $f_{5\%}(Y_{ij})/f_0$ for each Y_{ij} parameter as a function of the biasing parameter k for the frequency power-series model (dashed line, *POWER*), the second-order iterative results [3] (dashed line, *B*2), the first-order iterative results [3] (dashed line, *B*1), and the simple *RC* circuit representation of the frequency power-series model (dashed-dotted line, *EQ*). One observes that the simple *RC* representation of the frequency power series holds for all bias conditions up to a higher frequency than both the frequency power series and the iterative results. On the same curve we have also plotted the unity current gain cutoff frequency f_T/f_0 (dashed line, *FT*) and the maximum frequency of oscillation $f_{\max}/f_0$ (plain line, *FMAX*), (frequency at which the unilateral gain is one [18]). Both f_T and $f_{\max}$ are calculated using the exact Bessel solution.

All approximate small-signal models except the first-order iterative model hold for frequencies larger than the cutoff frequency f_T for all bias conditions. The *RC* circuit representation holds for frequencies larger than the maximum frequency of oscillation $f_{\max}$ for k smaller than ~ 0.9. For k larger than ~ 0.9, $f_{5\%}$ is however smaller than $f_{\max}$. Note that both the exact and the approximate models predict an infinite maximum frequency of oscillation at $k = 1$. Obviously in the extrinsic device the unavoidable source, drain, and gate resistances and drain output conductance will limit $f_{\max}$ to a finite value. The infinite $f_{\max}$ predicted for the intrinsic FET is nonetheless an indication of the limited validity of the long-channel model. Indeed even in long-channel devices the drain-current saturation ultimately results from velocity saturation and not pinchoff so that we always have $k < 1$ in the unsaturated part of the channel. The readers are referred to [12] for a discussion of the resonant behavior of the unilateral gain calculated using the short-channel model [5].

To conclude note that the normalization frequency f_0 is bias-dependent. For gate voltages approaching the threshold voltage, the normalization frequency f_0 is small and none of these so-called high-frequency approximate models can account for the distributed effects arising even at low frequencies.

V. Large-Signal Model

The *RC* equivalent circuit developed for the small-signal MOSFET wave equation can be readily implemented into a primitive large-signal model.

This is done by simply replacing g_m and g_d with the current source I_{DC} of the MOSFET *I–V* characteristics and by substituting for the dc gate and drain voltage V_{GS} and V_{DS} in the resistors and capacitors and in I_{dc} their instantaneous values v_{GS} and v_{DS}.

The gate, drain, and source currents are then given by (see Fig. 1(b))

$$i_G = i_{GG} + i_{GD}$$

$$i_D = I_{\text{DC}} + i_{DD} + i_{DG}$$

$$i_S = i_G + i_D$$

with

$$I_{\text{DC}} = \frac{C_g W_g \mu}{2L_g}\left[(v_{GS} - V_T)^2 - (v_{GS} - V_T - v_{DS})^2\right]$$

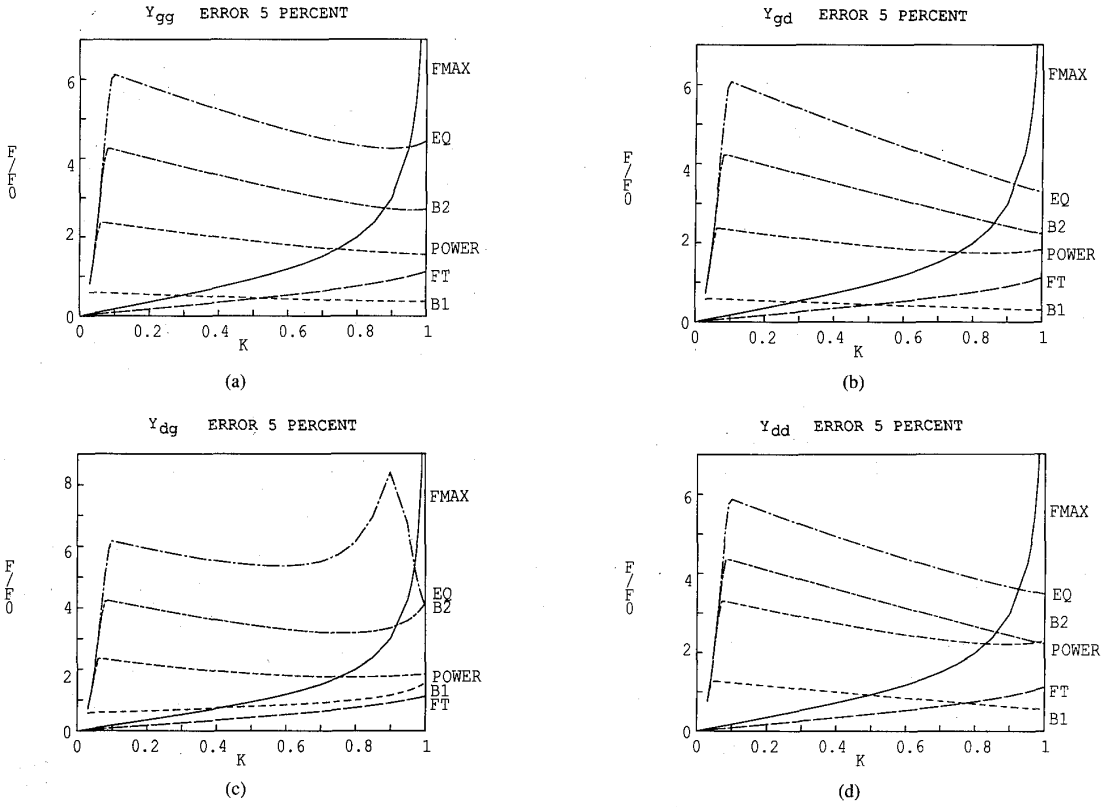


Fig. 3. Plot of $f_{5\%}(Y_{ij})/f_0$ for (a) Y_{gg}, (b) Y_{gd}, (c) Y_{dg}, and (d) Y_{dd} as a function of the biasing parameter k for the frequency power-series model (dashed line, *POWER*), the first-order iterative results [3] (dashed line, *B1*), the second-order iterative results [3] (dashed line, *B2*), the *RC* equivalent circuit (dashed-dotted line, *EQ*). Also shown are the unity current gain cutoff frequency f_T/f_0 (dashed line, *FT*), and the maximum frequency of oscillation f_{max}/f_0 (plain line, *FMAX*).

$$i_{GG} = C_{gg}(v_{GS}, v_{DS}) \frac{d}{dt} [v_{GS} - R_{gg}(v_{GS}, v_{DS}) i_{GG}]$$

$$i_{GD} = C_{gd}(v_{GS}, v_{DS}) \frac{d}{dt} [v_{DS} - R_{gd}(v_{GS}, v_{DS}) i_{GD}]$$

$$i_{DG} = C_{dg}(v_{GS}, v_{DS}) \frac{d}{dt} [v_{GS} - R_{dg}(v_{GS}, v_{DS}) i_{DG}]$$

$$i_{DD} = C_{dd}(v_{GS}, v_{DS}) \frac{d}{dt} [v_{DS} - R_{dd}(v_{GS}, v_{DS}) i_{DD}].$$

To test this *RC* large-signal model we submitted it to the four large-signal computer experiments used by Mancini *et al.* [19] and Chai and Paulos [6] for their four-terminal MOSFET large-signal models. The mobility ($\mu = 609$ cm^2/V), and gate length ($L_g = 10$ μm) given in [6] and [19] are used for our three-terminal MOSFET together with $V_T = 0$.

In the first test the drain voltage is $v_{DS} = 1$ V and the gate voltage v_{GS} varies from 2 to 10 V in 1 ns. The currents calculated using the *RC* model (plain lines) are shown in Fig. 4(a) and (b). For comparison we have also plotted in Fig. 4(a) and (b) the currents obtained using the trans-capacitor model (dashed lines) which relies on the same capacitors C_{ij} but neglect the charging resistors $R_{ij} = 0$.

In the second test the drain voltage is $v_{DS} = 1$ V and the gate voltage v_{GS} varies from 10 to 2 V in 1 ns. The currents calculated using the *RC* model (plain lines) and using the trans-capacitor model (dashed lines) are shown in Fig. 5(a) and (b).

In the third test the gate voltage is $v_{GS} = 10$ V and the drain voltage v_{DS} varies from 1 to 10 V in 1 ns. The currents calculated using the *RC* model (plain lines) and using the trans-capacitor model (dashed line) are shown in Fig. 6(a) and (b).

The currents calculated with the three-terminal *RC* large-signal model exhibit the same type of transient obtained with the numerical results reported by Mancini [19] for the four-terminal MOSFET. The success of the *RC* model is attributed to the fact that for these biases the MOSFET is operating in the triode region and the C_{ij} and R_{ij} vary slowly with the instantaneous bias.

In the fourth test the drain voltage is $v_{DS} = 4$ V and the gate voltage v_{GS} varies from 0.0001 to 10 V in 1 ns. The currents calculated using the *RC* model (plain lines) and

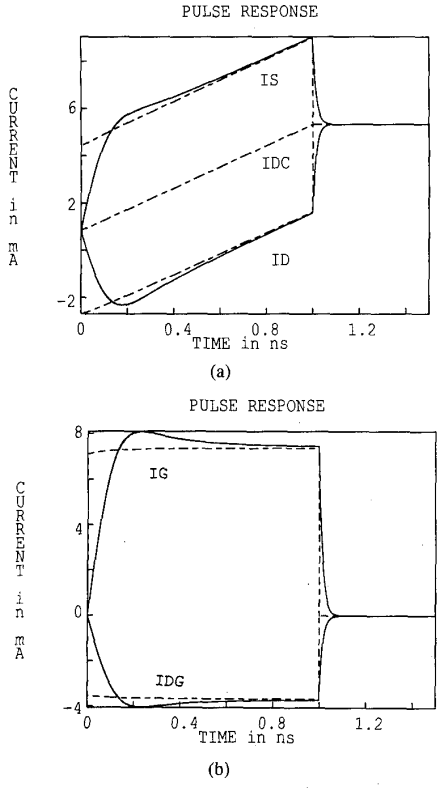


Fig. 4. Plot of (a) i_D, i_S, and I_{DC} and (b) i_G and i_{DG} calculated for v_{DS} = 1 V and v_{GS} varying from 2 to 10 V in 1 ns using the *RC* model (plain lines), the trans-capacitor model (dashed lines), and the state equations (dashed-dotted lines).

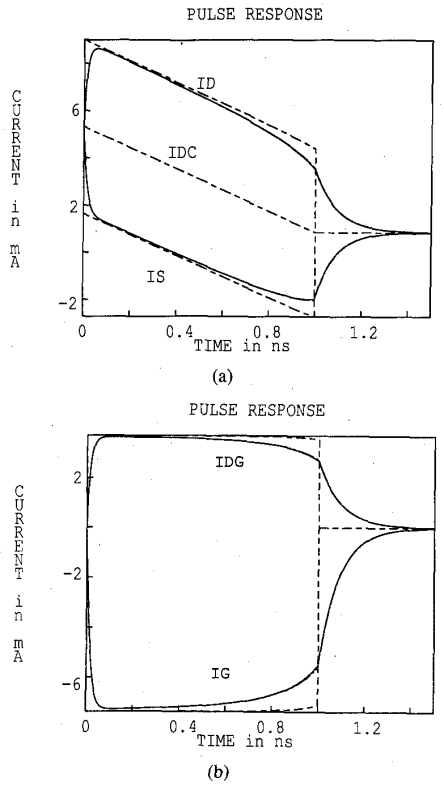


Fig. 5. Plot of (a) i_D, i_S, and I_{DC} and (b) i_G and i_{DG} calculated for v_{DS} = 1 V and v_{GS} varying from 10 to 2 V in 1 ns using the *RC* model (plain lines), the trans-capacitor model (dashed lines), and the state equations (dashed-dotted lines).

using the trans-capacitor model (dashed line) are shown in Fig. 7(a) and (b).

When compared with the results reported by Mancini [19] (for the four-terminal MOSFET), the (three-terminal) *RC* model fails on two accounts. The *RC* large-signal model predicts a negative drain current between $t = 0$ and $t = \sim 0.35$ ns, which is not present in the exact numerical solution [19]. Finally it introduces a rapid increase of the drain and gate currents at $t = 0.4$ ns, when the MOSFET switches from the pinchoff to the triode mode. This rapid variation of the current, not observed in the exact solution [19], originates from the rapid variation of C_{ij} and R_{ij} near pinchoff. As we shall see this problem can be removed if charge conservation is enforced.

Recently Chai and Paulos [6] reported a unified large- and small-signal model derived using an iterative technique which permitted them to reproduce the numerical results of Mancini quite well [19].

For small-signal analysis, their first-order iterative technique reduces to the first-order iterative solution of the MOSFET wave equation (see [2] and [13]). Their work suggests the use of the following alternate set of differential equations:

$$i_{GG} = C_{gg}(v_{GS}, v_{DS}) \frac{dv_{GS}}{dt} - \frac{d}{dt} \cdot [C_{gg}(v_{GS}, v_{DS})\, R_{gg}(v_{GS}, v_{DS}) i_{GG}]$$

$$i_{GD} = C_{gd}(v_{GS}, v_{DS}) \frac{dv_{DS}}{dt} - \frac{d}{dt} \cdot [C_{gd}(v_{GS}, v_{DS})\, R_{gd}(v_{GS}, v_{DS}) i_{GD}]$$

$$i_{DG} = C_{dg}(v_{GS}, v_{DS}) \frac{dv_{GS}}{dt} - \frac{d}{dt} \cdot [C_{dg}(v_{GS}, v_{DS})\, R_{dg}(v_{GS}, v_{DS}) i_{DG}]$$

$$i_{DD} = C_{dd}(v_{GS}, v_{DS}) \frac{dv_{DS}}{dt} - \frac{d}{dt} \cdot [C_{dd}(v_{GS}, v_{DS})\, R_{dd}(v_{GS}, v_{DS}) i_{DD}]. \quad (4)$$

The response of the intrinsic MOSFET to the gate and drain voltage ramps as predicted with these new differential equations is shown in Figs. 4, 5, 6, and 7(a) and (b) using dashed-dotted lines. It is not possible to distinguish this modified *RC* model (dashed-dotted) from the *RC* model (plain lines) except in Fig. 7(a) and (b) where a smoother response in agreement with the numerical simulation [19] results when the MOSFET enters the triode mode.

The modified large-signal model still predicts a negative drain current in Fig. 7. As is explained by Mancini *et al.* [19] the drain current cannot be negative for large drain voltages. Indeed for large drain voltages, when the device is biased in the saturation region, a fraction of the

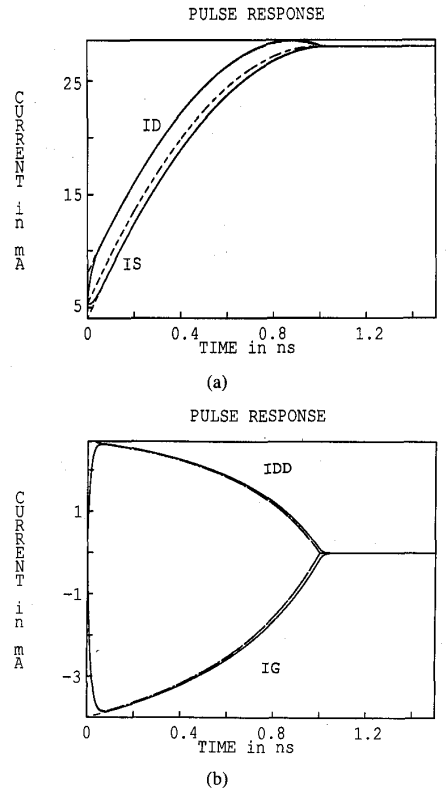


Fig. 6. Plot of (a) i_D, i_S, and I_{DC} and (b) i_G and i_{DD} calculated for v_{GS} = 10 V and v_{DS} varying from 1 to 10 V in 1 ns using the *RC* model (plain lines), and trans-capacitor model (dashed lines), and the state equations (dashed-dotted lines).

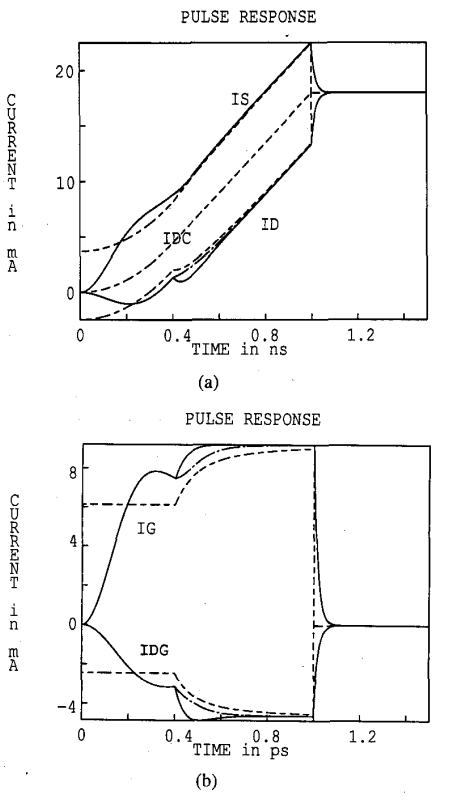


Fig. 7. Plot of (a) i_D, i_S, and I_{DC} and (b) i_G and i_{DG} calculated for v_{DS} = 4 V and v_{GS} varying from 0.0001 to 10 V in 1 ns using the *RC* model (plain lines), the trans-capacitor model (dashed lines), and the state equations (dashed-dotted lines).

applied drain voltage is dropped in the built-in potential barrier in the drain region. The resulting increase in the potential barrier at the drain prevents the electrons from diffusing from the drain to the channel to charge the channel. A negative drain current charging the depleted channel is however possible in the triode mode (Figs. 4 and 5) since in this case the built-in potential barrier is not increased by the drain voltage (see, for example, [20]). The simple wave equation used here [4] does not account in its boundary conditions for diffusion and cannot therefore predict this effect. Note that large built-in potentials at the drain arise only when the device is biased in saturation (pinch-off). Therefore, both the small- and large-signal *RC* models proposed here should be correct for the unsaturated MOSFET and moderately saturated (long-channel) MOSFET. A more complicated equivalent circuit is required for the saturated MOSFET (see Section XI). Note that the use of improved boundary conditions to drive the state equations presented here might not be sufficient by itself to avoid the negative drain current in Fig. 7. Chai and Paulos, who used such boundary conditions for the long-channel MOSFET, still found it necessary to assume the result (set the drain current to zero when it would be negative) on a physical basis rather than derive it from their state equations (see [6, Appendix II]. Another possible reason for the failure to reproduce the exact response (no negative current) in Fig. 7 is that for small gate voltages V_G the frequency f_0 becomes very small and the channel of the MOSFET quickly behaves like a true transmission line. Indeed the (*RC*) state equations derived above cannot be used for excitation with frequency components much in excess of f_0 (or $f_{5\%}$). Note however that the non-quasi-static state equations generate a current response (dashed-dotted line) far superior to the quasi-static model (dashed line).

VI. Charge Conservation

Charge conservation is an important issue in circuit simulation. The charge ΔQ transferred to a device through a terminal X in a time Δt by an in-going current $i_X(t)$ is simply given by

$$\Delta q_X = \int_0^{\Delta t} i_X(t)\, dt.$$

Global charge conservation in the FET model results from Kirchhoff's current law $i_S = i_G + i_D$ as is verified by integration over time. This global charge conservation does not however prevent the gate and channel of a large-signal FET model from continuously accumulating charge over

time [21]. Such an accumulation of charge in the channel is inconsistent with the assumption of dc *I–V* characteristics which are not history-dependent. Furthermore, it is known that such unphysical charge accumulation adversely affects the external circuits in a circuit simulator [26].

The gate (or channel) charge Q_G in the MOSFET in steady state is given by

$$Q_G(V_{GS}, V_{DS}) = W_g \int_0^{L_g} qN_S(x)\,dx = W_g C_g L_g \frac{2}{3} \frac{(V_{GS} - V_T - V_{DS})^3 - (V_{GS} - V_T)^3}{(V_{GS} - V_T - V_{DS})^2 - (V_{GS} - V_T)^2}.$$

The variation of the gate charge predicted by the dc model from the steady-state bias conditions 1 to 2 is

$$\Delta Q_G(1, 2) = Q_G[V_{GS}(2), V_{DS}(2)] - Q_G[V_{GS}(1), V_{DS}(1)].$$

Let us verify that the FET state equations (4) predict a variation of gate and channel charge which is compatible with the dc model. The instantaneous charge transferred to the gate Δq_G (which is also the charge accumulated in the FET channel) is

$$\Delta q_G(t_1, t_2) = \int_{t_1}^{t_2} i_G\,dt = \int_{t_1}^{t_2} (i_{GG} + i_{GD})\,dt = \Delta Q_G(t_1, t_2) - \int_{t_1}^{t_2} \left(\frac{d}{dt}(R_{gg}C_{gg}i_{GG}) + \frac{d}{dt}(R_{gd}C_{gd}i_{GD}) \right) dt$$

where $\Delta Q_G(t_1, t_2)$ is

$$\Delta Q_G(t_1, t_2) = \int_{t_1}^{t_2} \left(C_{gg} \frac{dv_{GS}(t)}{dt} + C_{gd} \frac{dv_{DS}(t)}{dt} \right) dt. \tag{5}$$

The variation of the instantaneous gate charge is then

$$\begin{aligned}\Delta q_G(t_1, t_2) &= \Delta Q_G(t_1, t_2) - \tau_{gg}[v_{GS}(t_2), v_{DS}(t_2)]i_{GG}(t_2) \\ &\quad + \tau_{gg}[v_{GS}(t_1), v_{DS}(t_1)]i_{GG}(t_1) \\ &\quad - \tau_{gd}[v_{GS}(t_2), v_{DS}(t_2)]i_{GD}(t_2) \\ &\quad + \tau_{gd}[v_{GS}(t_1), v_{DS}(t_1)]i_{GD}(t_1).\end{aligned}$$

If the device is in steady state at time t_1 and t_2, i_{GG} and i_{GD} must be zero at these times, and we have $\Delta q_G(t_1, t_2) = \Delta Q_G(t_1, t_2)$.

One can easily verify that the capacitor C_{gg} and C_{gd} can be obtained from the gate (or channel) charge Q_G by

$$C_{gg}(v_{GS}, v_{DS}) = \frac{\partial Q_G(v_{GS}, v_{DS})}{\partial v_{GS}}$$

$$C_{gd}(v_{GS}, v_{DS}) = \frac{\partial Q_G(v_{GS}, v_{DS})}{\partial v_{DS}}.$$

Since in the unsaturated MOSFET ($0 \le k < 1$) the gate charge Q_G admits continuous partial derivatives, its time derivative is then given by

$$\frac{dQ_G}{dt} = C_{gg}(v_{GS}, v_{DS}) \frac{dv_{GS}}{dt} + C_{gd}(v_{GS}, v_{DS}) \frac{dv_{DS}}{dt}.$$

$\Delta Q_G(t_1, t_2)$ as defined by (5) can now be written

$$\Delta Q_G(t_1, t_2) = \int_{t_1}^{t_2} \frac{dQ_G}{dt}\,dt = Q_G[v_{GS}(t_2), v_{DS}(t_2)] - Q_G[v_{GS}(t_1), v_{DS}(t_1)]$$

which is path-independent. It results that $\Delta q_G(t_1, t_2)$ is equal to $\Delta Q_G(1, 2)$ if the FET is in the steady-state biasing conditions 1 and 2 at times t_1 and t_2, respectively.

The modified large-signal model using the differential equation topology inspired by Chai and Paulos model [6] enforces the desired conservation of charge for the unsaturated FET. Charge conservation is also enforced in the saturated MOSFET ($v_{DS}(t) > v_{GS}(t) - V_T$). Indeed, the saturated MOSFET follows the same state equations since we use $k = 1$ to calculate the *RC* elements in saturation. Using $k = 1$ is equivalent to applying an effective drain voltage $v_{DS}(t) = v_{GS}(t) - V_T$. However, as we would expect in an ideal pinched-off MOSFET, this effective time-varying drain-to-source voltage $v_{DS}(t)$ does not induce any charging currents in the saturated FET since we have $C_{gd}(k = 1) = C_{dd}(k = 1) = 0$.

VII. Comparison with the Chai and Paulos Large-Signal Model

Let us now compare our large-signal model with the large-signal model reported by Chai and Paulos [6].

The capacitor C_{dg} and C_{dd} can be obtained from the partial derivatives of a charge Q_D

$$C_{dg}(v_{GS}, v_{DS}) = \frac{\partial Q_D(v_{GS}, v_{DS})}{\partial v_{GS}}$$

$$C_{dd}(v_{GS}, v_{DS}) = \frac{\partial Q_D(v_{GS}, v_{DS})}{\partial v_{DS}}$$

where Q_D is the portion of the gate (or channel) charge Q_C associated with the drain and given by

$$Q_D(v_{GS}, v_{DS}) = C_g W_g L_g \times \frac{2}{15} \frac{-15(v_{GS} - V_T)^3 + 25(v_{GS} - V_T)^2 v_{DS} - 15(v_{GS} - V_T)v_{DS}^2 + 3v_{DS}^3}{4(v_{GS} - V_T)^2 - 4(v_{GS} - V_T)v_{DS} + v_{DS}^2}.$$

These identities cannot be used here to reduce the number of differential equations. The large-signal model introduced here therefore requires four differential equations instead of the two in the Chai and Paulos large-signal model [6]. This originates from the fact that their first-order iterative model relies on the single relaxation time constant τ whereas our model uses four different relaxation time constants $\tau_{gg} = R_{gg}C_{gg}$, $\tau_{gd} = R_{gd}C_{gd}$, $\tau_{dg} = R_{dg}C_{dg}$, and $\tau_{dd} = R_{dd}C_{dd}$.

Using the identities

$$Q_1 - \tau I_{DC} = Q_D$$

$$Q_2 + \tau I_{DC} = Q_G + Q_D$$

relating the charges Q_1 and Q_2 defined in [6] to Q_D and Q_G, respectively, the two state equations derived by Chai and Paulos [6] can be rewritten after a few manipulations

$$(i_{GG} + i_{GD}) = \frac{dQ_G}{dt} - \frac{d}{dt}[\tau(i_{GG} + i_{GD})]$$

$$(i_{DG} + i_{DD}) = \frac{dQ_D}{dt} - \frac{d}{dt}[\tau(i_{DG} + i_{DD})]. \qquad (6)$$

By setting $\tau_{gg} = \tau_{gd} = \tau_{dg} = \tau_{dd} = \tau$, one can then easily verify that the large-signal model proposed here reduces exactly to the Chai and Paulos model. The use of four differential equations instead of two is expected to increase the frequency range. This is demonstrated for the small-signal parameters in Figs. 3(a)–(d), where the first-order Y-parameters (EQ) resulting from the four differential equations (4) are seen to be valid for $k > 0.1$ to a frequency $f_{5\%}$, 4 to 12 times that of the first-order iterative Y-parameters ($B1$) resulting from the two differential equations (6). This is also noticeable in the time domain in [6, figs. 1, 2, and 3] where approximate and exact responses are compared. The approximate transient response at $t = 1$ ns seems to overestimate the exact relaxation time by approximately a factor of two. Indeed, the exact relaxation-time constants τ_{ij} are approximately half τ as can be seen in Fig. 8 where the different relaxation-time constants τ_{gg}, τ_{gd}, τ_{dg}, and τ_{dd} are compared with τ for all biasing conditions ($0 \le k \le 1$).

VIII. Alternate Equivalent Circuits

Given the frequency power series (1) or even the expansion (2) it is not possible to extract a unique small-signal equivalent circuit model.

Consider the following equivalent circuit model for Y_{dg}:

$$Y_{dg} = \frac{g_m}{1 + j\omega\tau_{RC}} e^{-j\omega\tau_{TL}}$$

$$Y_{dg} = (g_m + j\omega C_1)e^{-j\omega\tau_{TL}}.$$

It is possible to select the transmission line delay τ_{TL} and the capacitor C_1 or the RC delay τ_{RC} such that these alternate equivalent circuits admit the desired frequency power series of the form (1). Physical considerations indicate however that these popular equivalent circuits are not acceptable representations of the frequency power-series Y-parameters for the unsaturated MOSFET. For frequencies ω up to ω_0 the unsaturated three-terminal MOSFET/MODFET behaves like a lumped device. Any phase shift present in the device cannot therefore arise from a transmission-line-type delay τ_{TL}. It also seems natural to use resistors and capacitors since only the Poisson equations are solved in this simple model. Note that R_{gd}, R_{dg} and C_{gd}, C_{dg} are negative. However, both time-delay constants $R_{gd}C_{gd}$ and $R_{dg}C_{dg}$ remain positive.

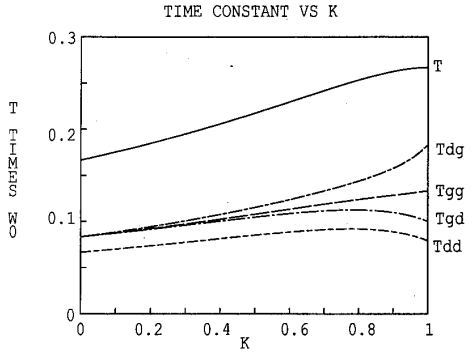


Fig. 8. Plot of τ_{gg}, τ_{gd}, τ_{dg}, and τ_{dd} (plain lines) and τ ([2] and [6]) (dashed lines) normalized by $1/\omega_0$ versus the biasing parameter k.

Despite its limitations, the smooth transient analysis reported in Section V agrees well with the numerical simulation of Mancini [19] and the large-signal model of Chai and Paulos [6]. This clearly supports the choice of an RC-based small-signal equivalent circuit over a transmission-line-delay representation for the unsaturated MODFET at the frequencies for which the frequency f power series is valid ($f < f_{5\%}$).

An alternative RC implementation of the frequency power-series Y-parameter can be generated with the following topology:

$$Y_{dg} = \frac{g_m}{1 + j\omega\tau_{RC}} + \frac{j\omega C_1}{1 + j\omega R_1 C_1}. \qquad (7)$$

A large-signal implementation of this alternate RC circuit representation was studied for various RC delays τ_{RC}. It did not yield as smooth a transient performance as the simple RC equivalent circuit and was ruled out. Indeed, this popular circuit topology strongly departs from the topology derived rigorously by Chai and Paulos [6].

IX. The Optimal Second-Order Equivalent Circuit

The simple RC equivalent circuit shown in Fig. 9(a) is valid when the frequency considered is small enough so that the unsaturated MOSFET behaves like a lumped device. At high frequencies, transmission line effects become important and a second-order equivalent circuit becomes desirable.

A second-order RC equivalent circuit can be obtained if we rewrite the second-order iterative Y-parameters of

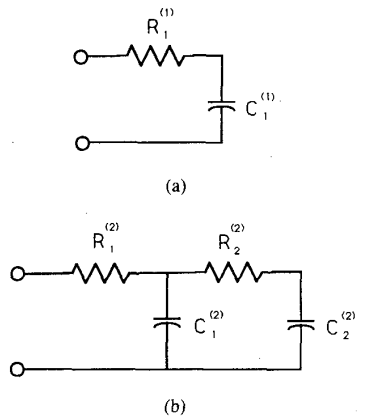


Fig. 9. First-order (a) and second-order (b) *RC* equivalent circuits for $Y_{ij} - g_{ij}$, the frequency-dependent component of a *Y*-parameter Y_{ij}.

(2) under the form

$$Y_{ij} = g_{ij} + \frac{j\omega a'_{ij} + (j\omega)^2 b'_{ij}}{1 + j\omega c_{ij} + (j\omega)^2 d_{ij}} \tag{8}$$

using $a'_{ij} = a_{ij} - g_{ij}c_{ij}$ and $b'_{ij} = b_{ij} - g_{ij}d_{ij}$. Our discussion in the previous section suggests that the *RC* equivalent circuit shown in Fig. 9(b) is the preferred (most physical) equivalent-circuit representation of $Y_{ij} - g_{ij}$ in (8) for the unsaturated MOSFET.

In order to generate an optimal second-order equivalent circuit the *Y*-parameters of Fig. 9(b) must admit a frequency power-series expansion valid up to $(j\omega)^4$.

The second-order iterative *Y*-parameters [3], although of the correct topology, admit a frequency power-series expansion valid only up to $(j\omega)^2$. Indeed, the optimal first-order *RC* equivalent circuit was found in Section IV to hold up to higher frequencies than the second-order iterative *Y*-parameters [3].

We have verified that the optimal second-order *Y*-parameters exist and indeed have a much higher frequency range of validity than the fourth-order iterative *Y*-parameters obtained with the iterative method. In particular, they offer an excellent graceful degradation. These optimal second-order *Y*-parameters and their associated small-signal equivalent circuits will be reported elsewhere [24].

X. The Four-Terminal MOSFET

The work reported here was initially developed for the MODFET (see [4] and [5]), a high-performance heterojunction FET (HFET) which behaves much like an ideal three-termimal MOSFET. We will now demonstrate that the three-terminal *Y*-parameters (exact or approximate), the small-signal equivalent circuit, and the large-signal state equations reported here can be readily applied without modification to the four-terminal MOSFET model developed by Bagheri and Tsividis [2]. Indeed, their model is based on the same MOSFET wave equations, provided we use the following normalization constants:

$$k = \frac{V_0(0) - V_0(L_g)}{V_0(0)}$$

$$g_0 = \frac{\mu}{1+\delta}\frac{C_g W_g V_0(0)}{L_g}$$

$$\omega_0 = \frac{\mu}{1+\delta}\frac{V_0(0)}{L_g^2}$$

where δ is a bias-dependent constant associated with the bulk capacitance (see [2]). The dc boundary conditions $V_0(0)$ and $V_0(L_g)$ are obtained in [2, Appendix I] using an iterative procedure. The gate current $i_g(4)$, the substrate current $i_b(4)$, and the drain current $i_d(4)$ for the four-terminal MOSFET are given by [23]

$$i_g(4) = j\omega C_g W_g L_g \frac{\delta}{1+\delta}(v_{gs}(4) - v_{bs}(4)) + \frac{1}{1+\delta} i_g(3)$$

$$i_b(4) = j\omega C_g W_g L_g \frac{\delta}{1+\delta}(v_{bs}(4) - v_{gs}(4)) + \frac{\delta}{1+\delta} i_g(3)$$

$$i_d(4) = i_d(3)$$

where $i_g(3)$ and $i_d(3)$ are the three-terminal currents

$$i_g(3) = Y_{gg}(3)\, v(0) + Y_{gd}(3)(v(0) - v(L_g))$$

$$i_d(3) = Y_{dg}(3)\, v(0) + Y_{dd}(3)(v(0) - v(L_g)).$$

Note that we have $i_g(4) + i_b(4) = i_g(3)$. The *Y*-parameters $Y_{ij}(4)$ of the four-terminal MOSFET can then be evaluated in terms of the three-terminal MOSFET *Y*-parameters $Y_{ij}(3)$ once the boundary conditions $v(0)$ and $v(L_g)$ are known.

In the strong-inversion limit the ac boundary conditions $v(0)$ and $v(L_g)$ simplify to

$$v(0) = v_{gs}(3) = v_{gs}(4) + \delta v_{bs}(4)$$

$$v(L_g) = v_{gs}(3) - v_{ds}(3) = v_{gs}(4) + \delta v_{bs}(4) - (1+\delta) v_{ds}(4).$$

The small-signal currents of the four-terminal MOSFET are then simply given by

$$i_g(4) = \left[\frac{1}{1+\delta} Y_{gg}(3) + j\omega C_g W_g L_g \frac{\delta}{1+\delta}\right] v_{gs}(4) + [Y_{gd}(3)]\, v_{ds}(4) + \left[\frac{\delta}{1+\delta} Y_{gg}(3) - j\omega C_g W_g L_g \frac{\delta}{1+\delta}\right] v_{bs}(4)$$

$$i_b(4) = \left[\frac{\delta}{1+\delta} Y_{gg}(3) - j\omega C_g W_g L_g \frac{\delta}{1+\delta}\right] v_{gs}(4) + [\delta Y_{gd}(3)] v_{ds}(4) + \left[\frac{\delta^2}{1+\delta} Y_{gg}(3) + j\omega C_g W_g L_g \frac{\delta}{1+\delta}\right] v_{bs}(4)$$

$$i_d(4) = [Y_{dg}(3)] v_{gs}(4) + [(1+\delta) Y_{dd}(3)] v_{ds}(4) + [\delta Y_{dg}(3)] v_{bs}(4).$$

The Y-parameters of the four- and three-terminal MOSFET are seen to be related by simple relations in strong inversion. This can be easily generalized to any mode of operation by using the constants H_i given in [2]. A large-signal model is easily constructed from this small-signal model.

XI. The Velocity-Saturated MOSFET Wave Equation

The small-signal model presented above for the intrinsic MOSFET holds only for the region of the channel for which the gradual channel approximation (GCA) holds. However, in saturation it becomes necessary to account for the contribution of the built-in potential. A more complex equivalent circuit results in which the equivalent circuit introduced for the MOSFET wave equation is now just a subcircuit.

Let us demonstrate this approach for the velocity-saturated MOSFET wave equation we recently reported [5]. In this conventional MODFET model the FET channel is divided into the GCA and saturation regions of length $X_S = L_g - l$ and l, respectively. In the saturation region the electron velocity is assumed to saturate (to a value v_s) while the GCA is failing. The channel potential in the saturation region is then assumed to be supported uniquely by the electron distribution in the channel. An exact solution of the wave equation was obtained in [5] in terms of Bessel functions. Rewriting the resulting Y-parameters $Y_{ij}(\text{sat})$ in terms of the Y-parameters of the GCA region $Y_{ij}(3)$ of reduced gate length $X_S = L_g - l$, the following expressions are obtained (the details of the derivation will be reported elsewhere [25]):

$$Y_{11}(\text{sat}) = Y_{11}(3) + Y_{12}(3)\delta_s + \frac{Y_{21}(3) + Y_{22}(3)\delta_s}{1 + Y_{22}(3)\, Z_s(\omega)} \cdot (1 - e^{-j\omega\tau_s} - Z_s(\omega)\, Y_{12}(3))$$

$$Y_{12}(\text{sat}) = Y_{12}(3)\gamma_s + \frac{Y_{22}(3)\gamma_s}{1 + Y_{22}(3)\, Z_s(\omega)} \cdot (1 - e^{-j\omega\tau_s} - Z_s(\omega)\, Y_{12}(3))$$

$$Y_{21}(\text{sat}) = \frac{Y_{21}(3) + Y_{22}(3)\gamma_s}{1 + Y_{22}(3)\, Z_s(\omega)} e^{-j\omega\tau_s}$$

$$Y_{22}(\text{sat}) = \frac{Y_{22}(3)\delta_s}{1 + Y_{22}(3)\, Z_s(\omega)} e^{-j\omega\tau_s}$$

where $\tau_s = v_s/l$ is the transit time of the saturation region, $Z(\omega)$ an impedance specified below, and δ_s and γ_s are two constants given by

$$\gamma_s = 1 - \delta_s = \frac{1}{1 + \beta I_{DC} l A}$$

with

$$A = \frac{2X_S(1-k_s)}{(2k_s - k_s^2)(V_{GS} - V_T)}$$

$$B = \frac{4X_S(1-k_s)^2}{G_{d0s}(2k_s - k_s^2)^2(V_{GS} - V_T)}.$$

Note that $k_s = V_{CS}(X_S)/(V_{GS} - V_T)$ and $G_{d0s} = \mu C_g W_g (V_{GS} - V_T)/X_S$ are the values used for k and the drain conductance g_d, respectively, in the GCA Y-Parameters $Y_{ij}(3)$ given in Section III.

These Y-parameters can be represented by the equivalent circuit given in Fig. 10 where the impedance $Z_s(\omega)$ is approximated by a first-order RC network providing the correct second-order frequency power-series expansion

$$Z_s = R_{s1} + \frac{R_{s2}}{1 + j\omega C_s R_{s2}} \tag{9}$$

with

$$R_{s1} = \frac{\beta I_{DC} l B - \frac{1}{6}\beta l^2}{1 + \beta I_{DC} l A}$$

$$R_{s2} = \frac{2\beta l^2}{3(1 + \beta I_{DC} l A)}$$

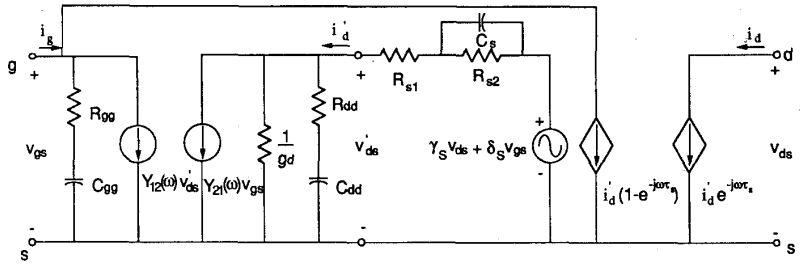
$$C_s = \frac{3}{8}\tau_s \frac{(1 + \beta I_{DC} l A)}{\beta l^2}$$

using $\beta = 1/\epsilon_1 v_s W_g d_s$ [5]. The resulting equivalent circuit provides an optimal first-order non-quasi-static equivalent circuit admitting the correct second-order frequency power expansion as well as a graceful degradation. This is demonstrated in Fig. 11 for an intrinsic MODFET with the parameters given in Table I and for an intrinsic bias of $V_{DS} = 3$ V and $V_{GS} = 0$ V. The phase and amplitude of Y_{21} versus frequency calculated using this first-order RC equivalent circuit (dashed–dotted line, *EQUI*), the exact solution (plain line, *EXACT*), and the frequency power-series approximation (dashed line, *POWER*) are compared in Fig. 11(a) and (b). The optimal first-order RC model (*EQUI*) is seen to hold to a much higher frequency than the frequency power-series approximation (*POWER*).

The development of a large-signal model from this small-signal topology is now conceivable [22].

XII. Conclusion

We have presented a simple RC equivalent circuit for the frequency power-series Y-parameters of the intrinsic three-terminal MOSFET. This first-order RC equivalent circuit was found to hold to higher frequencies than the



$$Y_{12}(\omega) = \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}}$$

$$Y_{21}(\omega) = g_m + \frac{j\omega C_{dg}}{1 + j\omega R_{dg} C_{dg}}$$

Fig. 10. First-order non-quasi-static equivalent circuit for the velocity-saturated MOSFET wave equation.

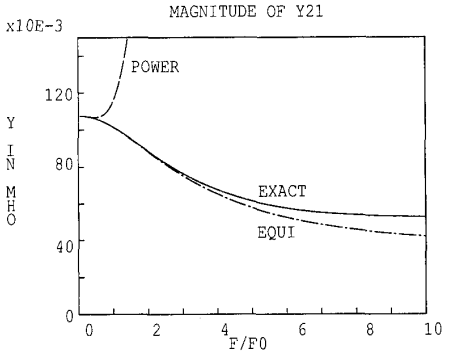


Fig. 11. Comparison of the amplitude (a) and phase (b) of Y_{21} for V_{DS} = 3 V and V_{GS} = 0 V, obtained with the *RC* equivalent circuit (dashed-dotted line, *EQUI*), the exact solution (plain line, *EXACT*), and the frequency power series (dashed line, *POWER*).

frequency power series from which it is derived or the more complicated second-order iterative *Y*-parameters reported by [3]. Like the iterative *Y*-parameters, this *RC* equivalent circuit features a graceful degradation of the small-signal parameters at high frequencies. Although quite simple the *RC* equivalent circuit selected departs from conventional equivalent circuit models which usually rely on a transmission line or *RC* delay for the drain transconductance and a *C* or series *RC* feedback element between the drain and gate and an inductor in series with the drain conductance.

TABLE I
DEVICE PARAMETERS FOR THE INTRINSIC SHORT-CHANNEL MODFET

Parameters		Value
L_g	gate length (μm)	1
W_g	gate width (μm)	290
μ	mobility (cm^2/V · s)	4400
v_s	saturation velocity (m/s)	3.45×10^5
V_T	threshold voltage (V)	−0.3
d	gate-to-channel spacing (Å)	430
d_s	channel width in saturation (Å)	1500
ϵ_1	channel dielectric constant	13.1 ϵ_0
ϵ_2	gate dielectric constant	12.2 ϵ_0

This *RC* equivalent circuit was used to develop a large-signal model and was submitted to four different transient tests. The transient analysis has met with some encouraging success for the unsaturated MOSFET. Some discrepancies were observed when the long-channel MOSFET was operated in the pinchoff (saturation) region. A smoother response was obtained with a modified topology for the current differential equations, inspired by the recent work by Chai and Paulos [6]. This modified large-signal model was shown to enforce charge conservation. This result supports the concept that a non-quasi-static large-signal model conserving charge cannot be implemented with an equivalent-circuit model using voltage-dependent time-invariant resistances and capacitances.

It was demonstrated that the *RC* equivalent circuit reported here can be readily implemented in the long-channel four-terminal MOSFET model reported in [2] since the latter model is based on the same MOSFET wave equation. The *Y*-parameters $Y_{ij}(4)$ of the four-terminal MOSFET can be expressed in terms of the *Y*-parameters $Y_{ij}(3)$ of the three-terminal MOSFET and the constants δ and H_i given in [2].

Similarly we extended this non-quasi-static small-signal equivalent circuit model to the short-channel velocity-saturated MOSFET wave equation [5]. The resulting equivalent circuit provided a graceful degradation of the small-signal *Y*-parameters at high frequencies.

To conclude note that the equivalent circuits reported here were derived for the ideal MOSFET/MODFET model which assumes that the gate capacitance, the threshold voltage, the mobility, and the saturation velocity are not bias-dependent. Useful FET models can usually be obtained (see [2], [5], and [6]) by introducing *a posteriori* the effective bias dependence or state equations (if frequency-dependent [26]) of these parameters.

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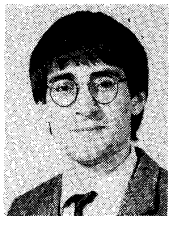

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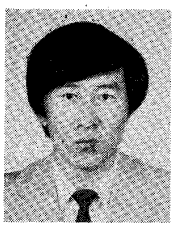

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