Improved Space Vector Modulation for Neutral-Point Balancing Control in Hybrid-Switch-Based T-Type Neutral-Point-Clamped Inverters With Loss and Common-Mode Voltage Reduction

Hongwu Peng, Zhao Yuan, Xingchen Zhao, Balaji Narayanasamy, Amol Deshpande,
Asif Imran Emon, Fang Luo, and Cai Chen

Abstract—This paper compares different space vector modulation (SVM) strategies for neutral-point voltage balancing (NPVB) control in three-level (3-L) T-type neutral-point-clamped (TNPC) inverters, and proposes an improved SVM trimmed for NPVB control in hybrid-switch-based 3-L TNPC inverter with the features of loss and common-mode voltage (CMV) reduction. The proposed SVM strategy uses a new principle of small vector selection and vector sequence, and thus, it can balance the neutral point (NP) potential and achieve soft-switching of clamping leg simultaneously. The paper includes detailed analysis for circuit commutation mode, loss breakdown, and common-mode voltage patterns under different operation conditions. The circuit simulations and experiments are carried out in the last part of this paper to validate the proposed SVM strategy.

Index Terms—Electromagnetic interference (EMI), neutral-point (NP) voltage balance, Si-SiC hybrid switch, space vector modulation (SVM), T-type neutral-point-clamped (TNPC) inverter, wide bandgap (WBG) devices.

I. INTRODUCTION

THREE-LEVEL T-type neutral-point-clamped (3-L TNPC) inverter has higher efficiency and lower total harmonic distortion (THD) compared to two-level inverter, and it has become popular in high-speed motor drives and all-electric aircraft applications [1]–[5]. Emerging silicon carbide (SiC) MOSFET has lower losses and high switching speed compared to Si IGBT and enables higher efficiency and power density in power converters [6]–[11]. SiC MOSFET is becoming a major competitor and
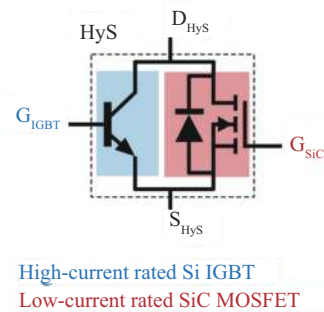
Fig. 1. Structure of the hybrid switch.

replacement for Si IGBT in power electronics systems.

However, the state-of-the-art die size limit and the high cost of SiC MOSFET are the bottlenecks for its high-current commercial applications. Therefore, [13] proposed a hybrid switch concept, as shown in Fig. 1. By adjusting the switching sequence of the two switches, the T-type inverter with the hybrid switch (hybrid structure 1) [14]–[16], which is shown in Fig. 2, can have low switching loss from SiC MOSFET switching, and low conduction loss from IGBT conduction. However, due to the long discharging time of the carriers inside the IGBT, the Si-SiC hybrid switch operation mode have a minimum duty cycle limitation [17], which deteriorates the output total harmonic distortion performance. Furthermore, the hybrid-switch-based 3-L TNPC increases the system complexity in terms of the gate driver and power loop design [18]–[20]. Because of more paralleled semiconductors, more gate drivers and more gating signals are required. [12] mentioned that the Si-SiC hybrid switch structure should ensure the safe operation area (SOA) of the SiC MOSFET. Table I illustrates the current dependent operation in [12].

To reduce the system complexity as well as improve the output THD performance, M_1, M_4, Q_2, Q_3, D_2 and D_3 in hybrid structure 1 are selected to operate, and the new structure is shown in Fig. 3 [21]. The hybrid structure 2 utilizes Si IGBT and SiC Schottky diode as clamping leg switches and SiC
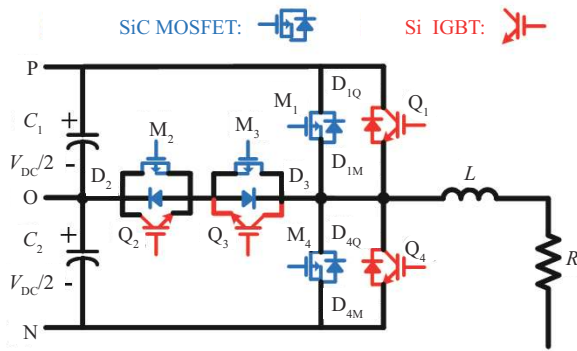
Fig. 2. T-type inverter with hybrid switch structure 1 [13].

TABLE I
CURRENT DEPENDENT OPERATION OF THE HYBRID-SWITCH-BASED INVERTER [12]

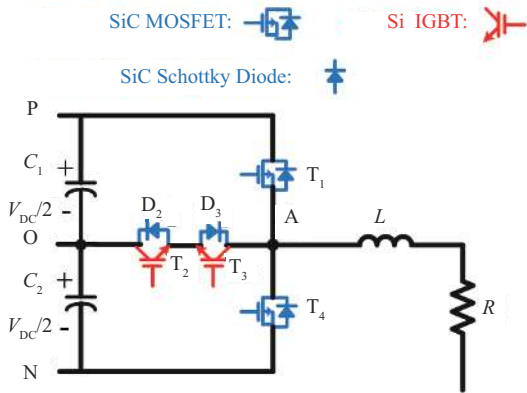| Condition	Operation
SiC MOSFET voltage drop is lower than Si IGBT threshold	Only SiC MOSFET is turned on
Load current is within SOA of SiC MOSFET	Hybrid switch operation
Load current exceed SOA of SiC MOSFET	Only IGBT is turned on

Fig. 3. T-type inverter with hybrid switch structure 2 [21].

MOSFET for half-bridge switch positions. With SPWM, the clamping switches are soft-switching under the unity power factor, and thus, the utilization of Si IGBTs does not increase the switching loss. Therefore, the total semiconductor cost of this hybrid switch combination 3-L TNPC is lower than that of the all-SiC 3-L TNPC inverter. While the cost is low, the efficiency is higher than that of the all-SiC 3-L TNPC inverter.

Although hybrid structure 2 possesses the merits of low complexity and high efficiency, it has not been fully validated in the 3-phase 3-L TNPC system yet. One of the main challenges is to design a proper space vector modulation (SVM) scheme, which needs to consider the soft switching feature of

the clamping leg, neutral point balancing (NPB) [22]–[25] and the common-mode voltage (CMV) performance. This paper provides a criterion to choose the appropriate SVM for T-type inverter with hybrid structure 2 under different conditions. Firstly, this paper obtains the switching energy of T-type inverter with hybrid structure 2 by experimental double pulse test (DPT) result, then 3 different SVM schemes are discussed in terms of switching loss, NPB, and output CMV voltage performance.

The organization of the paper is as follows. Section II summarizes the soft-switching conditions for 3-L TNPC with hybrid structure 2, then loss analysis, neutral point balancing capability and common-mode noise voltage comparison of 3 different SVM schemes are discussed. In Section III, a 20 kVA hardware is built, the DPT is firstly performed to obtain exact switching loss, and followed by the analysis and comparison of semiconductor loss breakdown, EMI spectrum and neutral point voltage ripple for three SVMs. Section IV presents the conclusion of the preferred modulation scheme.

II. ANALYSIS OF DIFFERENT MODULATION ON HYBRID SWITCH BASED 3-PHASE 3-L TNPC

For switching loss reduction [21] and NPB [22]–[25] in 3 phase 3-L TNPC inverter with hybrid switch combination, SVM 1 with NPB [23], SVM 2 with NPB [24], and improved SVM 2 with NPB are compared, and 1st sector of the space vector modulation hexagon is given as an example. The nearest three space vector (NTSV) [26] and discontinuous pulse width modulation (DPWM) [27] are adopted to track the reference vector and further reduce the switching loss.

In this chapter, switching loss and soft-switching condition of clamping leg is discussed first in 3-L TNPC with the hybrid switch combination. Then three different SVM schemes are compared in terms of switching losses, neutral point balancing capability, and CMV performance, which gives guidance for hardware design and PWM modulation choice.

A. Preferred Switch Pairs in Terms of Switching Loss Reduction

Since switching loss of Si IGBT is much higher than SiC MOSFET, hard switching of Si IGBT on clamping leg in 3-L TNPC inverter with hybrid switch combination should be avoided or minimized. As shown in Fig. 4(a), when the phase current is positive, and the phase output voltage is transitioning from positive to neutral, T_1 is hard switching off, and then T_2 and D_3 are soft switched on. From Fig. 4(b) we can know that when phase current is positive, and the phase output voltage is transiting from neutral to positive, clamping leg devices are soft switched off, and T_1 is hard switched on. Moreover, when the phase current is negative, and phase output is transitioning from positive to neutral or from neutral to positive, T_3 is hard switched on and hard switched off.

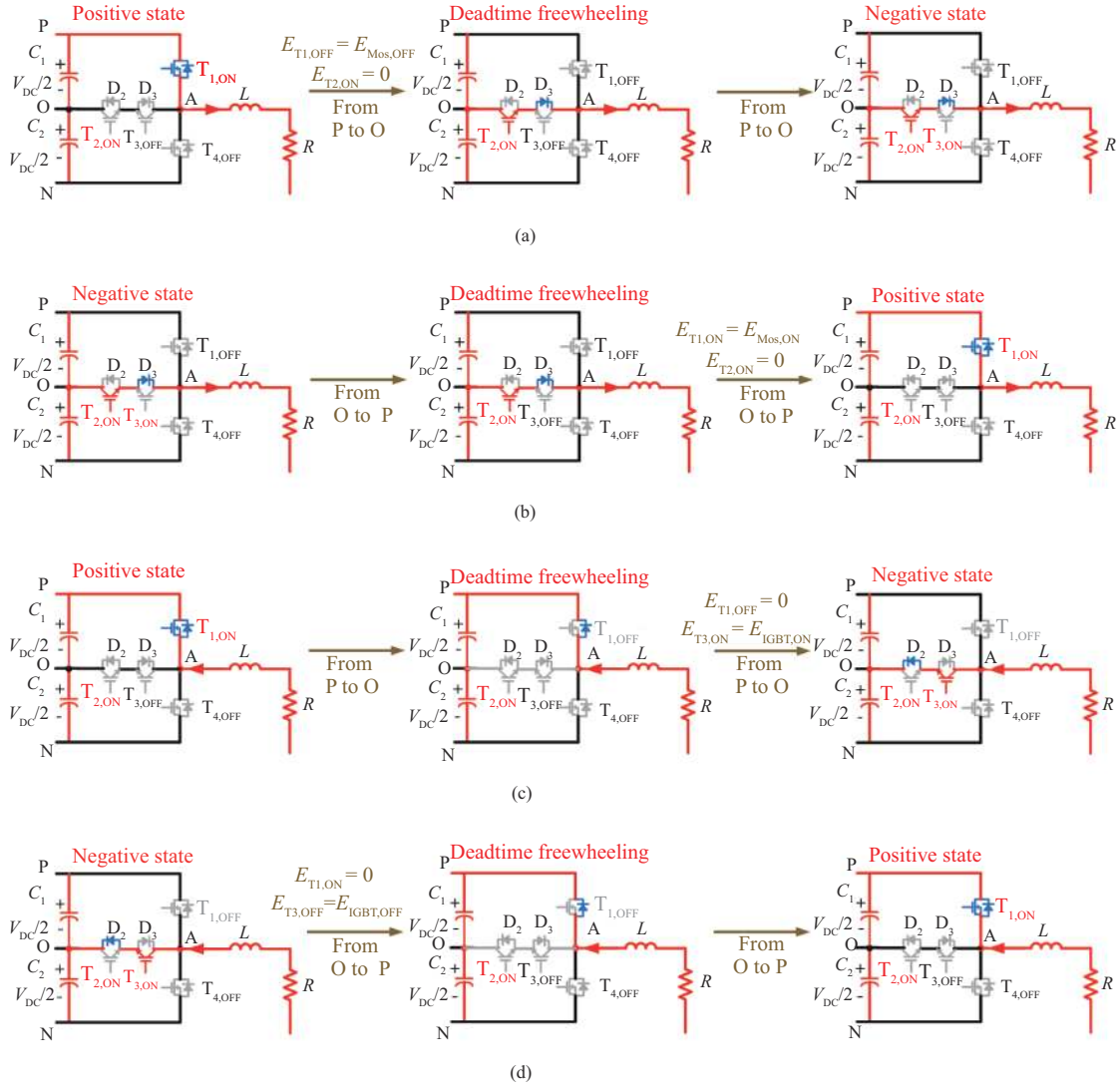In summary, when phase current is positive, switch pair 1

Fig. 4. Different switching transitions when the phase output is positive or neutral. (a) Switch transition 1 (positive phase current). (b) Switch transition 2 (positive phase current). (c) Switch transition 3 (negative phase current). (d) Switch transition 4 (negative phase current).

and 0 is preferred since the clamping leg is soft-switching, as shown in Fig. 4(a) and (b). Switch pair 0 and −1 should be avoided since clamping leg switch T_2 is hard switching. Symmetrically when phase current is negative, switch pair 0 and −1 is preferred to obtain the soft-switching character of clamping leg, and switch pair 1 and 0 should be avoided or minimized to reduce the switching loss of Si IGBT, as shown in Fig. 4(c) and (d). Based on the aforementioned analysis, different SVMs can be compared in terms of switching loss, more detailed information will be given in the later section.

B. Common-Mode Voltage of 3-L TNPC Inverter

Assuming that only heatsink is grounded, the equivalent model of 3 phase 3-L TNPC [28]–[33] is drawn in Fig. 5, with the consideration of all the semiconductor's junction to heatsink and output to ground capacitance. Also, a simplified model is given in Fig. 6, which indicates that the CMV noise

can be modeled through (1).

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3 \qquad (1)$$

Space vectors in sector 1 of the modulation hexagon, which is shown in Fig. 7, are given as an example for CMV calculation. As shown in Table II, small vector V_1 and V_5 have the largest CMV, while zero vector V_8 and medium vector V_3 do not contribute to CMV.

C. Switching Loss Reduction, NPB and CM Voltage Analysis for Different SVM Schemes

Firstly, space vectors of sector 1 are marked out in Fig. 7 and small vectors' influence on neutral point potential are stated in Table III. For simplicity, the regions 3 and 2 are analyzed and compared for three kinds of SVM schemes, choices of small vectors and alignment in the regions 1 and 4 are similar to the
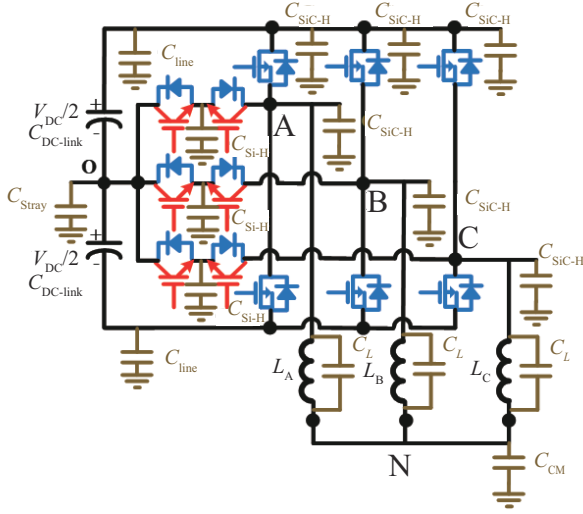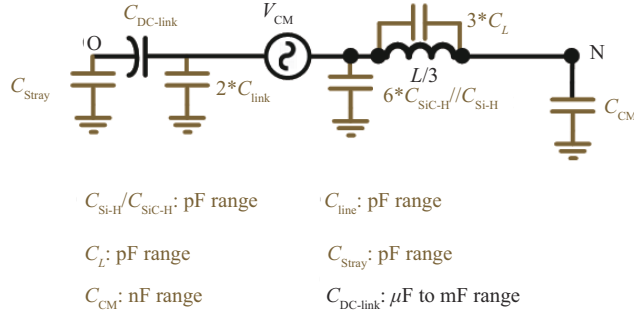
Fig. 5. Three-phase 3-L TNPC model with the parasitic capacitor.

C_{Si-H}/C_{SiC-H}: pF range C_{line}: pF range

C_L: pF range C_{Stray}: pF range

C_{CM}: nF range $C_{DC-link}$: μF to mF range

Fig. 6. Three-phase 3-L TNPC CMV path.

1: Connected to positive rail
0: Connected to clamping leg
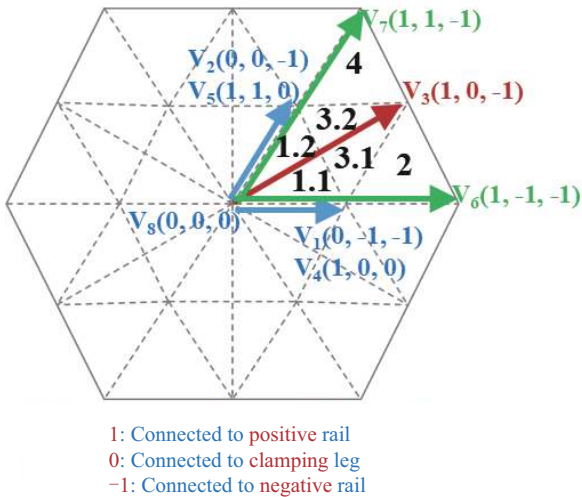−1: Connected to negative rail

Fig. 7. Three-phase three-level space vector hexagon.

regions 3 and 2. From Table II it is known that small vectors V_2 and V_4 have lower CM voltage than V_1 and V_5, less small vectors like V_2 and V_4 are chosen, smaller CM voltage the SVM schemes can get.

TABLE II
CMV OF SPACE VECTORS

Space vector	V_1	V_2	V_3	V_4
CMV	$-1/3V_{dc}$	$-1/6V_{dc}$	0	$1/6V_{dc}$
Space vector	V_5	V_6	V_7	V_8
CMV	$1/3V_{dc}$	$-1/6V_{dc}$	$1/6V_{dc}$	0

TABLE III
SMALL VECTOR'S INFLUENCE ON NP POTENTIAL

Small Vector Angle	Discharge NP	Charge NP
0º	V_4	V_1
60º	V_5	V_2

TABLE IV
SPACE VECTOR CHOICE AND ALIGNMENT IN SECTOR 3

The region 3 of Sector 1	Discharge NP	Charge NP
SVM 1	V_3-V_2-V_1-V_2-V_3	V_3-V_4-V_5-V_4-V_3
SVM 2 & 0º~30º	V_1-V_2-V_3-V_2-V_1	V_2-V_3-V_4-V_3-V_2
SVM 2 & 30º~60º	V_4-V_3-V_2-V_3-V_4	V_5-V_4-V_3-V_4-V_5
Improved SVM 2 & $I_b < 0$	V_1-V_2-V_3-V_2-V_1	V_2-V_3-V_4-V_3-V_2
Improved SVM 2 & $I_b > 0$	V_4-V_3-V_2-V_3-V_4	V_5-V_4-V_3-V_4-V_5

1) The Region 3 of Sector 1

The space vector choice and alignment for SVM 1, SVM 2, and improved SVM 2 are shown in Table IV. For SVM 1 scheme, both of the small vectors V_1, V_2, V_4, and V_5 are used for balancing the neutral point potential, and B phase switching state changes between 1 and 0 plus 0 and −1. Since SVM 1 does not consider the B phase current direction, B phase has hard switching operations on the clamping leg. For SVM 2 scheme, the region 3 is divided into the region 3.1 and the region 3.2 according to B phase voltage polarity. In the region 3.1, only V_1 and V_4 small vectors are used for balancing the neutral point potential. In the region 3.2, only V_2 and V_5 small vectors are used for balancing the neutral point potential. B phase clamping leg is always soft-switching under unity PF. Improved SVM 2 scheme is proposed to reduce the switching loss under the wider power factor range. When the B phase current is negative, V_1 and V_4 small vectors are used for balancing the neutral point potential. V_2 and V_5 small vectors are used when the B phase current is positive. Improved SVM 2 scheme is basically the same as SVM 2 scheme under the unity power factor, and since it considers the phase current direction for choosing the small vector, and thus, it has lower losses on clamping leg under the non-unity power factor case.

2) The Region 2 of Sector 1

For region 2, modulation strategies of SVM 1, SVM 2, and improved SVM 2 are the same, which is shown in Table V.

TABLE V
SPACE VECTOR CHOICE AND ALIGNMENT IN SECTOR 2

The region 2 of Sector 1	Discharge NP	Charge NP
SVM 1	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6
SVM 2	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6
Improved SVM 2	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6

TABLE VI
DEVICE PARAMETERS

Device	Voltage (V)	Current (A)
SiC MOSFET (Wolfspeed-C3M0075120K)	1200	30
Si IGBT (ROHM-RGCL60TS60D)	600	30
SiC Shottky diode (Wolfspeed-C3M0075120K)	650	23

V_1 and V_4 are chosen to discharge and charge the neutral point voltage, and alignments are V_6-V_3-V_4-V_3-V_6 and V_1-V_6-V_3-V_6-V_1 when the neutral point voltage is lower and higher than half of the DC-link voltage. Soft switching can be achieved on the clamping leg of B phase under the unity power factor.

3) Summary of Different SVM Schemes

In general, the improved SVM 2 scheme has the lowest switching loss on clamping leg. Moreover, under the non-unity power factor condition, SVM 1 has better neutral point balancing ability than SVM 2 and improved SVM 2. According to Table II, V_1 and V_5 have the highest CM voltage. Since SVM 2 and improved SVM 2 exclude V_1 or V_5 for reducing the switching loss, and SVM 1 employs both of the V_1 and V_5 for NPB, SVM 2 and improved SVM 2 have relatively lower CMV than that of SVM 1.

III. EXPERIMENTAL TEST AND LOSS BREAKDOWN

A 6 kVA 3-phase 3-L TNPC prototype is built to evaluate the efficiency and CM voltage noise spectrum with different SVM, upper and lower DC-link capacitors are 150 μF each. As shown in Table VI, we have chosen 1200 V/30 A SiC MOSFET, C3M0075120K from Wolfspeed, and 600 V/30 A Si-IGBT IKZ50N65EH5 from ROHM, and FFSH1665A SiC Schottky diode, for experiment validation. Top leg and bottom leg switches are rated for 1.2 kV, and DC-link voltage is set to be 800 V to remain some safety margin. Output RMS voltage is set to 208 V to meet one of the grid standards. Switching frequency is set to be 70 kHz to reduce the passive components' volume. The prototype is composed of three 2kVA single-phase 3-L TNPC, as shown in Fig. 8.

A. Switching Energy Evaluation of the Three-Level Inverter

Switching energy calculation based on the devices' voltage and devices' current waveform is comprehensively evaluated in [34]–[36]. DPT is firstly performed to obtain the switching
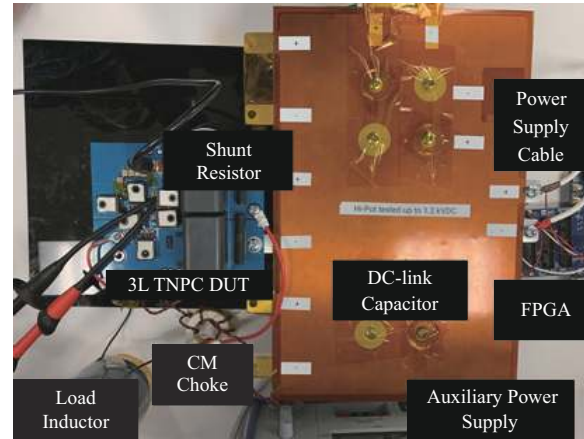

Fig. 8. Test setup of DPT.

transitions of both SiC MOSFET and IGBT devices. As mentioned in [37], switching energy in 3-L phase leg is different from 2L half-bridge due to the device's junction capacitance, so the double pulse test in this paper is performed based on the single-phase 3-L TNPC platform. In this way, loss analysis using switching energy data from the double pulse test on the 3-L TNPC platform gives more accurate results. The accurate switching energy information for SiC MOSFETs and Si IGBT switch is shown in Fig. 9.

B. Semiconductor Loss Breakdown and EMI Performance Evaluation

Switching energy from DPT and device conduction performance in the component datasheet are used, and a detailed semiconductor loss breakdown can be obtained in simulation. While the total power level is 6 kVA, and the switching frequency is 70 kHz.

For the near unity PF case, the loss breakdown for different modulation schemes is listed in Fig. 10(a), and total semiconductor loss using SVM 1, SVM 2, and improved SVM 2 are respectively 17.1 W, 16 W, and 16 W. As shown in the diagram, under the unity power factor case, total loss of the SVM 2 and the improved SVM 2 are 6.4% lower than using SVM 1. All of the SVMs have the same neutral point voltage ripple, which is around 2 V due to the hysteresis control algorithm at half of the switching frequency and switching actions at switching frequency.

However, for PF = 0.8 (lead or leg) case, loss breakdown for different modulation schemes are listed in Fig. 10(c), and total semiconductor loss using SVM 1, SVM 2 and improved SVM 2 are respectively 22.7 W, 18.9 W, and 17.9 W. It can be seen that by adopting SVM 1, clamping leg devices have excessive switching loss. In this condition. SVM 2 and improved SVM 2 have respectively 4.2 times and 5.3 times lower clamping leg devices' switching loss than that of SVM 1. Neutral point ripple voltage using SVM 1, SVM 2, and improved SVM 2 are respectively 2.3 V, 8.5 V, and 15 V.
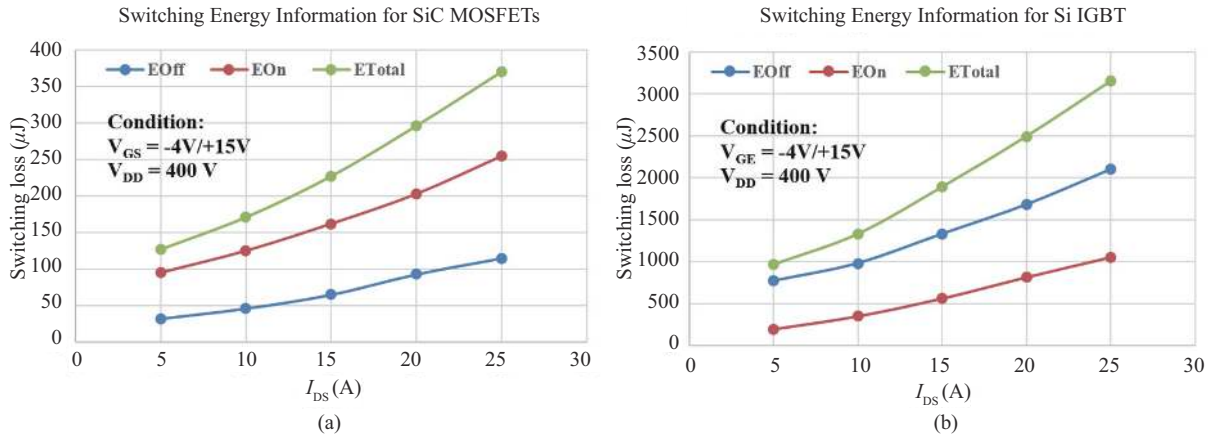
Fig. 9. Switching loss information for SiC MOSFET position and Si IGBT position. (a) Switching energy information for SiC MOSFET position. (b) Switching energy information for Si IGBT position.
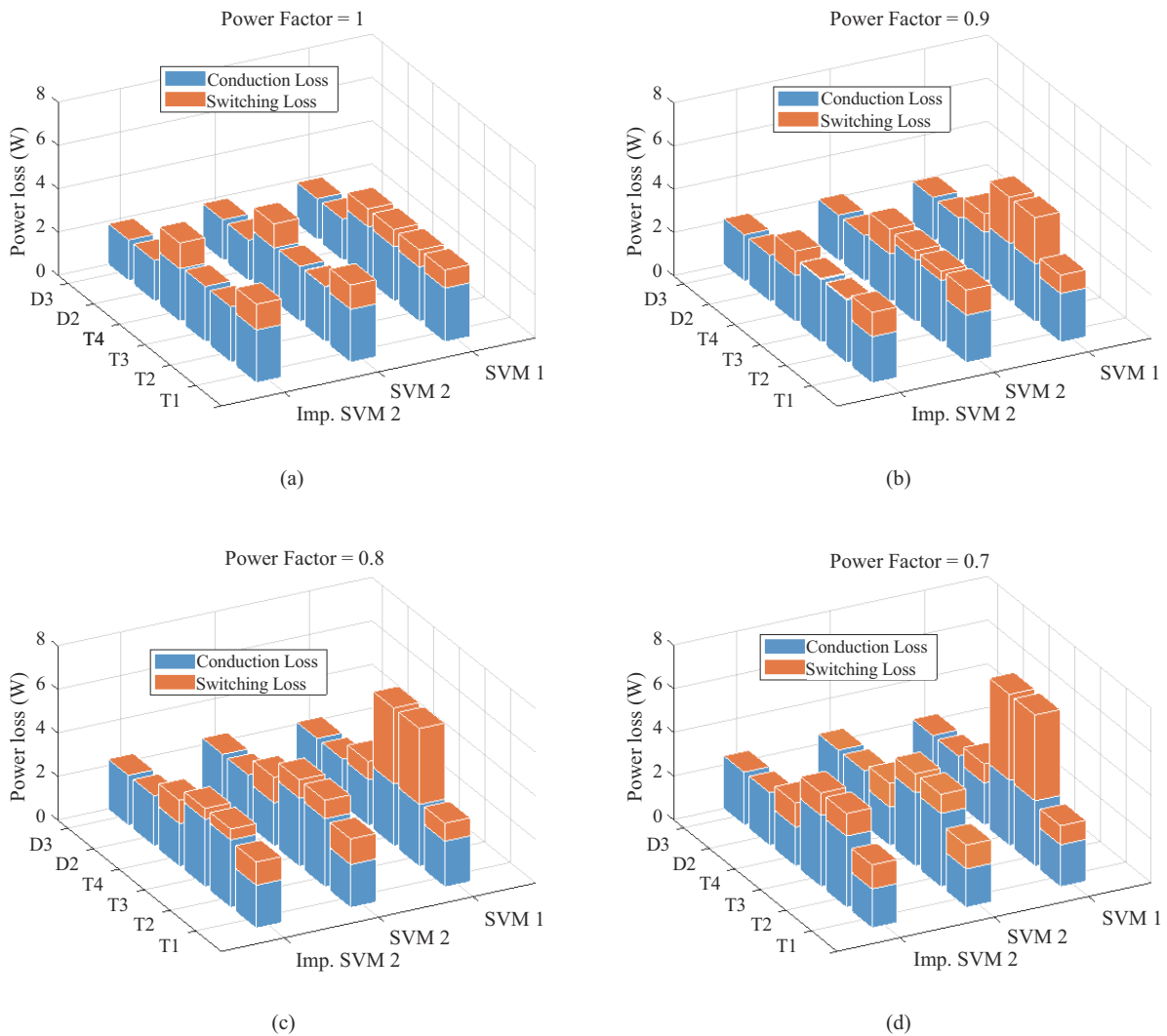
Fig. 10. Loss breakdown of semiconductor devices at different power factors. (a) Loss breakdown when PF = 1. (b) Loss breakdown when PF = 0.9. (c) Loss breakdown when PF = 0.8. (d) Loss breakdown when PF = 0.7.

The difference of SVM schemes is the switching transitions and soft-switching conditions of the clamping leg switches under different conditions, the average duty ratio for each switch does not change a lot for different SVM schemes. So even the conduction loss of different modulations have some difference, this difference in conduction loss is not as much as

Fig. 11. Neutral point ripple voltage.

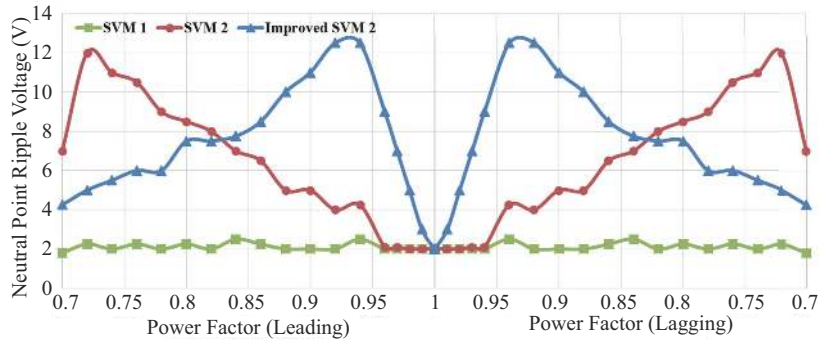in switching loss, and its not obvious in the figures.

In summary, with the power factor decreasing from 1 to 0.7, SVM 1 has a much higher loss on clamping leg devices than SVM 2 and improved SVM 2, which may result in device overheat issue. And it can be seen in Fig. 10 that under different power factor cases, SVM 2 and improved SVM 2 have more equal loss distribution among switching devices, so SVM 2 and improved SVM 2 are preferred in terms of semiconductor loss reduction and the semiconductor loss distribution point of view.

The neutral point voltage ripple versus power factor relationship is shown in Fig. 11. We can know that when the power factor is in the region of 0.85 to 1 (lead or lag), the SVM 1 and improved SVM 2 have higher neutral point voltage than SVM 2. When the power factor is high enough, SVM 2 also has as good clamping leg loss reduction capability as improved SVM 2. So when the power factor is between 0.85 and 1, it is better to use the SVM 2 modulation scheme for both clamping leg loss reduction as well as NPB purpose.

When the power factor is in the region of 0.7 to 0.85 (lead or lag), the SVM 1 still possesses the best NPB capability, and in the meantime, the improved SVM 2 has better NPB performance than the SVM 2. Moreover, when the power factor is relatively lower, improved SVM 2 has better clamping leg loss reduction capability than the SVM 2. When the power factor is between 0.85 and 1, the improved SVM 2 serves better for both clamping leg loss reduction and NPB purpose.

As shown in Fig. 12, comparison is made for evaluating the trade-off between NPB and loss performance using the improved SVM 2. Hysteresis width for neutral point balancing algorithm is controlled for obtaining different neutral point voltage ripple. It can be seen from Fig. 12 that, when neutral point ripple is increasing within a certain range, the total loss is decreasing due to less number of changing space vector alignment actions. However, when neutral point voltage ripple increases, the commutation voltage of the device is higher due to the unbalanced neutral point, which deteriorates the loss performance. It is recommended that the hysteresis width should be kept within 30 V for a neutral point balancing control algorithm.

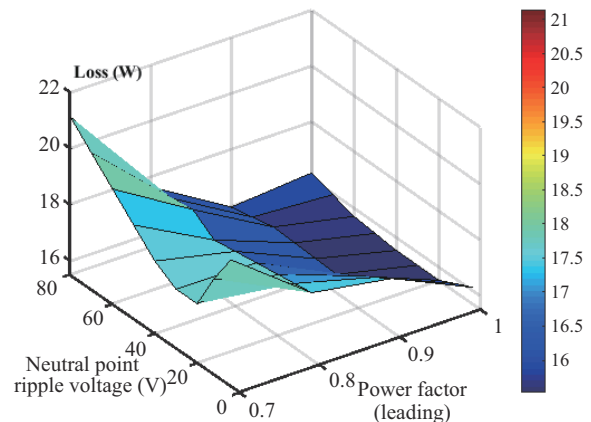MATLAB simulation has been conducted to compare EMI

Fig. 12. Trade-off between NPB and loss performance for improved SVM 2.

performance of different SVM schemes. In this simulation, V_{asw} represents the output phase voltage switching waveform, I_{ph} represents the phase current, V_{np} is the NP voltage, and V_{cm} shows the common-mode voltage. As shown in Fig. 13, when PF = 0.8, SVM 1 has a higher CM voltage ripple than SVM 2, and improved SVM 2. Under PF = 1 and PF = 0.8 cases, CM voltage and phase leg output voltage spectrum are shown in Fig. 14. As shown in Fig. 14(a) and (c), from 10 to 100 kHz range which is of great significance in EMI filter design, SVM 2 and improved SVM 2 have lower CM noise than SVM 1, especially at relatively low power factor case. It is shown in Fig. 14(b) and (d), since SVM 2, and improved SVM 2 have higher neutral point unbalanced voltage under non-unity power factor, their phase leg voltage has slightly larger harmonics (300 Hz, 420 Hz, etc.) than SVM 1. In terms of common-mode filter and output filter design, SVM 2 and improved SVM 2 are preferred due to their lower better common-mode voltage harmonics as well as comparable phase output voltage spectrum.

In summary, SVM 2 and improved SVM 2 have better performance regarding semiconductor loss and common-mode voltage reduction than SVM 1, but SVM 1 has the best neutral point balancing capability. When the power factor is between 0.85 and 1, SVM 2 is adopted for better overall performance,
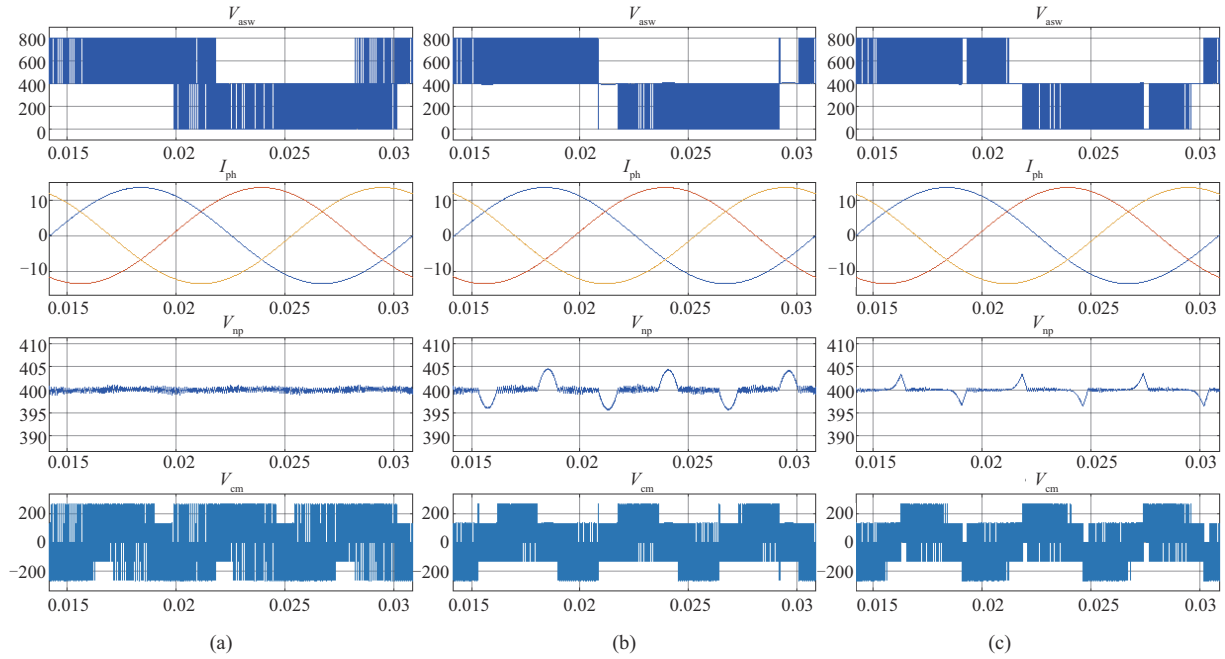
Fig. 13. Phase leg output voltage, phase current, NP voltage, and CM voltage waveform when PF = 0.8. (a) Waveform for the SVM 1. (b) Waveform for the SVM 2. (c) Waveform for improved SVM 2.
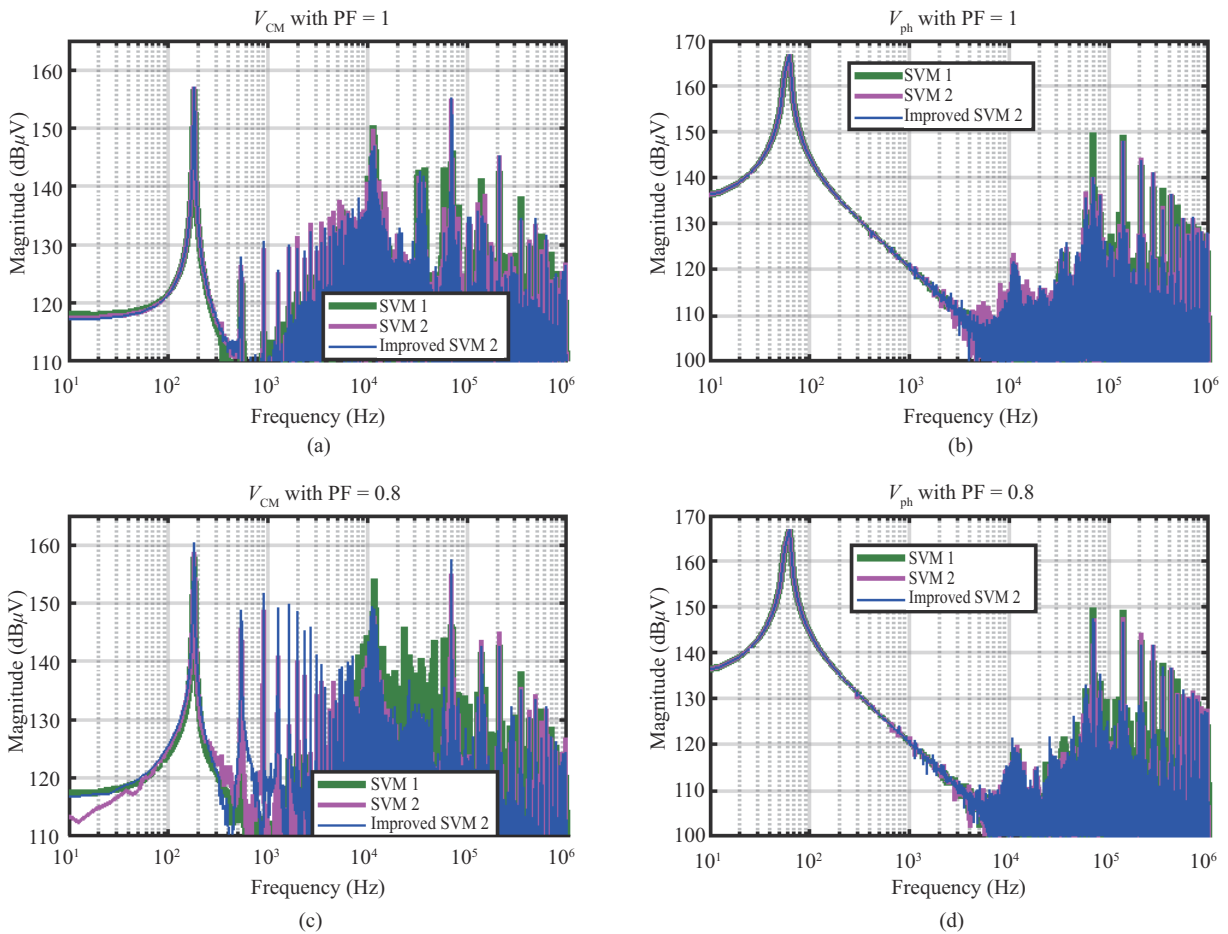

Fig. 14. CMV and phase voltage spectrum at different power factors. (a) CMV when PF = 1. (b) Phase voltage spectrum when PF = 1. (c) CMV when PF = 0.8. (d) Phase voltage spectrum when PF = 0.8.

and when the power factor is between 0.7 to 0.85, improved SVM 2 can be utilized for its' overall better loss reduction as well as neutral point balancing performance.

IV. Conclusion

In this paper, semiconductor losses of different commutation loops in hybrid switch combination TNPC are analyzed and compared. Based on different switching loss of commutation loops, SVM 1 and SVM 2 themes are utilized and compared in this topology comprehensively in terms of their influences on switching loss, NPB and EMI spectrum, and then improved SVM 2 is proposed to further push the converter to higher efficiency at relatively low power factor.

Comparing to SVM 1, SVM 2, and improved SVM 2 schemes have better loss performance and CM noise performance, while improved SVM 2 scheme has the lowest power loss and lowest CM noise. As for neutral point balancing capability, SVM 1 is better than SVM 2 and improved SVM 2 under non-unity power factor, and their neutral point balancing capabilities are the same under the unity power factor.

Hybrid-switch-based 3 phase 3-L TNPC is comprehensively studied in this paper, and it gives guidance for hybrid switch topology design consideration and the choice of SVM strategy.

References

[1] H. Peng, Z. Yuan, B. Narayanasamy, X. Zhao, A. Deshpande, and F. Luo, "Comprehensive analysis of three-phase three-level t-type neutral-pointclamped inverter with hybrid switch combination," in *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019, Xi'an, China, pp. 816–821.

[2] J. Rosero, J. Ortega, E. Aldabas, and L. Romeral, "Moving towardsa more electric aircraft," in *IEEE Aerospace and Electronic Systems Magazine*, vol. 22, no. 3, pp. 3–9, 2007.

[3] R. DelRosario, "A future with hybrid electric propulsion systems: Anasa perspective," 2014.

[4] Y. Chen, Z. Yuan, and F. Luo, "A model-based multi-objective optimizationfor high efficiency and high power density motor drive inverters foraircraft applications," in *NAECON 2018-IEEE National Aerospace andElectronics Conference*, 2018, pp. 36–42.

[5] Z. Yuan, H. Peng, A. Deshpande, B. Narayanasamy, A. I. Emon, F. Luo,and C. Chen, "Design and evaluation of laminated busbar for 3-levelt-type npc power electronics building block with enhanced dynamiccurrent sharing," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[6] G. Li, H. Li, A. Deshpande, X. Li, L. Xu, F. Luo, and J. Wang,"Comparison between 1.7 kv sic sjt and mosfet power modules," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications(WiPDA)*, 2016, pp. 17–22.

[7] C. Chen, F. Luo, and Y. Kang, "A review of sic power module packaging:Layout, material system and integration," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 170–186, 2017.

[8] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An sic based half-bridge module with an improved hybrid packaging methodfor high power density applications," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8980–8991, 2017.

[9] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible pcb-based 3-d integrated sic half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," in *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5579–5593, 2018.

[10] Z. Huang, C. Chen, Y. Xie, Y. Yan, Y. Kang, and F. Luo, "A high

[11] Z. Wang, M. H. Mahmud, M. H. Uddin, B. McPherson, B. Sparkman,Y. Zhao, H. A. Mantooth, and J. R. Fraley, "A compact 250 kw siliconcarbide mosfet based three-level traction inverter for heavy equipment applications," in *2018 IEEE Transportation Electrification Conferenceand Expo (ITEC)*, 2018, pp. 1129–1134.

[12] J. He, R. Katebi, and N. Weise, "A current-dependent switching strategyfor si/sic hybrid switch-based power converters," in *IEEE Transactions onIndustrial Electronics*, vol. 64, no. 10, pp. 8344–8352, 2017.

[13] A. Deshpande, Y. Chen, B. Narayanasamy, A. S. Sathyanarayanan, and F. Luo, "A three-level, t-type, power electronics building block using sisic hybrid switch for high-speed drives," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2609–2616.

[14] A. Deshpande and F. Luo, "Design of a silicon-wbg hybrid switch," in *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*, 2015, pp. 296–299.

[15] A. Deshpande and F. Luo, "Multilayer busbar design for a Si IGBT and SiC MOSFET hybrid switch based 100 kW three-level T-type PEBB," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 20-24.

[16] A. Deshpande and F. Luo, "Comprehensive evaluation of a silicon-WBG hybrid switch," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

[17] A. Deshpande and F. Luo, "Practical design considerations for a Si IGBT + SiC MOSFET hybrid switch: parasitic interconnect influences, cost, and current ratio optimization," in *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 724-737, Jan. 2019.

[18] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao and H. A. Mantooth, "An intelligent versatile model-based trajectory optimized active gate driver for silicon carbide devices," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[19] S. Zhao, A. Dearien, Y. Wu, C. Farnell, A. U. Rashid, F. Luo, andH. A. Mantooth, "Adaptive multi-level active gate drivers for sic powerdevices," in *IEEE Transactions on Power Electronics*, 2019.

[20] H. Gui, Z. Zhang, R. Chen, J. Niu, L. M. Tolbert, F. F. Wang, D. Costinett, B. J. Blalock, and B. B. Choi, "Gate drive technology evaluation and development to maximize switching speed of sic discretedevices and power modules in hard switching applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[21] A. Anthon, Z. Zhang, M. A. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of sic mosfet s in a t-type inverter forgrid-tie applications," in *IEEE Transactions on Power Electronics*, vol. 32,no. 4, pp. 2808–2821, 2017.

[22] H. Chen, M. Tsai, Y. Wang, and P. Cheng, "A Modulation technique for neutral point voltage control of the three-level neutral-point-clamped converter," in *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2517–2524, May-June 2018.

[23] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-levelnpc converter with neutral point voltage balance and switching loss reduction," in *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5579–5591, 2014.

[24] U.-M. Choi, J.-S. Lee, and K.-B. Lee, "New modulation strategy tobalance the neutral-point voltage for three-level neutral-clamped inverter systems," in *IEEE Transactions on Energy Conversion*, vol. 29, no. 1, pp.91–100, 2014.

[25] J. Holtz, M. Holtgen, and J. O. Krah, "A space vector modulator forthe high-switching frequency control of three-level sic inverters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2618–2626, 2014.

[26] N. Babu and P. Agarwal, "Nearest and non-nearest three vector modulations of npci using two-level space vector diagram—A novel approach,"in *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2400–2415, 2018.

[27] Y. Jiao, "High power high frequency 3-level neutral point clamped

performance embedded sic power module based on a dbc-stacked hybrid packaging structure," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

powerconversion system," Ph.D. dissertation, Virginia Polytechnic Institute and State University, 2015.

[28] H. Zhang, L. Yang, S. Wang, and J. Puukko, "Common-mode emi noisemodeling and reduction with balance technique for three-level neutralpoint clamped topology," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7563–7573, 2017.

[29] A. Deshpande, B. Narayanasamy, and F. Luo, "Analysis of conducted emi in si igbt + sic mosfet hybrid switch based converters," in *2018 IEEE International Symposium on Electromagnetic Compatibility and2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/ APEMC)*, 2018, pp. 127–127.

[30] B. Narayanasamy, F. Luo, and Y. Chu, "Modeling and stability analysisof voltage sensing based differential mode active emi filters for ac-dc power converters," in *2018 IEEE Symposium on ElectromagneticCompatibility, Signal Integrity and Power Integrity (EMC, SI & PI)*, 2018, pp. 322–328.

[31] B. Narayanasamy, A. S. Sathyanarayanan, A. Deshpande, and F. Luo, "Analysis and mitigation of reflected wave voltages and currents inwbg devices based motor drives," in *2016 IEEE 4th Workshop on WideBandgap Power Devices and Applications (WiPDA)*, 2016, pp.297–301.

[32] B. Narayanasamy, A. S. Sathyanarayanan, A. Deshpande and F. Luo, "Impact of cable and motor loads on wide bandgap device switching and reflected wave phenomenon in motor drives," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 931–937.

[33] B. Narayanasamy, F. Luo and Y. Chu, "High density EMI mitigation solution using active approaches," in *2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, Washington, DC, 2017, pp. 813–818.

[34] D. Christen and J. Biela, "Analytical switching loss modeling based ondatasheet parameters for mosfets in a half-bridge," in *IEEE Transactionson Power Electronics*, vol. 34, no. 4, pp. 3700–3710, 2019.

[35] Z. Zhang , "Characterization and realization of high switching-speed capability of SiC power devices in voltage source converter." Ph.D. dissertation, University of Tennessee, 2015.

[36] Z. Chen, "Characterization and modeling of high-switching-speed behaviorof sic active devices," Ph.D. dissertation, Virginia Tech, 2009.

[37] B. Liu, R. Ren, E. A. Jones, H. Gui, Z. Zhang, R. Chen, F. Wang, and D. Costinett, ""Effects of Junction Capacitances and Commutation Loops Associated With Line-Frequency Devices in Three-Level AC/DC Converters," in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6155-6170, July 2019.

Hongwu Peng Received the B.S. degree in Electrical Engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2018. He is currently working toward the Ph.D. degree in the University of Arkansas at Fayetteville, AR, USA.

His research interests include high-efficiency motor drive with WBG devices and active EMI cancellation.

Zhao Yuan was born in Jiaozuo, China, in 1992. He received the B.S. degree in Electrical Engineering from Huazhong University of Science and Technology and the master degree in Electrical Engineering from Arizona State University, Tempe, USA, in 2015 and 2017 respectively. He is currently working toward the Ph.D. degree at University of Arkansas, Fayetteville, Arkansas, USA. He is a graduate researching assistant involved in the research project with the National Science Foundation (NSF) Engineering Research Center for Power Optimization of Electro-thermal Systems (POETS). In 2019, he was a research intern at United Technologies Research Center, East Hartford, CT, USA.

His research interests include design and electro-thermal optimization of high-power converters for traction systems, high-voltage power module packaging. He received 2nd place student paper award at the 2018 National Aerospace & Electronics Conference (NAECON).

Xingchen Zhao was born in Jiangsu, China, in1993. He received the B.S. degree and M.S. degree in Electrical Engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2015 and 2018, respectively. He is currently pursuing the Ph.D. Degree with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA. His research interests include motor drive, multi-level inverters, and applications of wide bandgap devices.

Balaji Narayanasamy received his bachelor's degree in Electrical and Electronics Engineering from Amrita University, India in 2012, and master's degree in Electrical Engineering from The Ohio State University, Columbus, Ohio in 2016. He is currently pursuing his Ph.D. degree in Electrical Engineering at the University of Arkansas, Fayetteville, Arkansas. He was a Research Assistant from August 2015 to July 2018 at The Ohio State University and the University of Arkansas. He is currently serving as a Teaching Assistant at the University of Arkansas. Before joining his master's degree, he worked as a Product Engineer at L&T Kobelco, India from 2012 to 2014.

His research interests include analysis and mitigation of EMI in Wide Bandgap devices-based power converters. He has authored and co-authored twelve papers which were presented in different international conferences.

Amol Deshpande was born in Vadodara, India, in 1991. He received a B.Tech degree in Electrical Engineering from Nirma University in India and an M.S. degree in Electrical and Computer Engineering from The Ohio State University, Columbus, OH, in 2013 and 2016, respectively. He is currently working toward the Ph.D. degree in Electrical Engineering with the University of Arkansas, Fayetteville, AR. He is currently a graduate research assistant and involved in research projects with the National Science Foundation (NSF) Engineering Research Center for Power Optimization of Electro-thermal Systems (POETS). In 2018, he was a research intern at Kilby Labs, Texas Instruments, Santa Clara, CA, USA.

His current research interests include high-voltage power module packaging and electro-thermal design of high-power density inverters for traction and aircraft applications using wide-bandgap power semiconductor devices.He received a Best Paper Award at the 2016 IEEE Energy Conversion Congress and Exposition (ECCE).

Asif Imran Emon was born in Chittagong, Bangladesh in 1993. He received his B.Sc. degree in Electrical and Electronic Engineering from Chittagong University of Engineering and Technology in 2015. He is currently a Ph.D. student at the University of Arkansas, Fayetteville, Arkansas, USA.

His research interests include power module packaging of wide band gap devices, Electro-magnetic Interference and Compatibility in high power application.

Fang Luo received the bachelor's and Ph.D. degrees in Electrical Engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2003 and 2010, respectively. He is currently an Assistant Professor with the University of Arkansas, Fayetteville, AR, USA. From 2007 to 2010, he was a joint Ph.D. student at the Center for Power Electronics Systems (CPES), Virginia Tech, supported by the Chinese Scholarship Council and CPES. From 2010 to 2014, he was with CPES, Virginia Tech, first as a Postdoctoral Researcher and then as a Research Scientist. From 2014 to 2017, he was a Research Assistant Professor with The Ohio State University. In July 2017, he joined the University of Arkansas as a Tenure Track Assistant Professor.

His research interests include turbo electric propulsion converters, high-power-density converter design, high-density electromagnetic interference filter design, and power module packaging/integration for wide-bandgap devices.

Cai Chen is an Associate Research Fellow at Huazhong University of Science and Technology. He received the B.S. degree and Ph.D. degree in Electrical and Electronic Engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2014, respectively. From March 2013 to December 2013, he was an Intern in GE Global Research Center, Shanghai, China. From 2014 to 2016, he joined the Advanced Semiconductor, Packaging and Integration Lab, Huazhong University of Science and Technology, Wuhan, Hubei, China as a Postdoctoral Researcher. From 2016 to Oct. 2017, he was a visiting scholar in the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2017 to Oct. 2018, he was a visiting scholar in the College of Engineering, University of Arkansas, Fayetteville, AR, USA. In 2019, Dr. Chen joined the Huazhong University of Science and Technology, Wuhan, China, as an Associate Research Fellow.

His research interests include WBG devices packaging, integration, pack-aging EMI issues, packaging reliability and high-density applications.