Research Article

Improved Switching Energy Reduction Approach in Low-Power SAR ADC for Bioelectronics

Xingyuan Tong and Tiantian Sun

School of Electronic Engineering, Xi'an University of Posts & Telecommunications, Xi'an 710121, China

Correspondence should be addressed to Xingyuan Tong; mayxt@126.com

Low-power analog-to-digital converter (ADC) is a crucial part of wearable or implantable bioelectronics. In order to reduce the power of successive-approximation-register (SAR) ADC, an improved energy-efficient capacitor switching scheme of SAR ADC is proposed for implantable bioelectronic applications. With sequence initialization, novel logic control, and capacitive subconversion, 97.6% switching energy is reduced compared to the traditional structure. Moreover, thanks to the top-plate sampling and capacitive subconversion, 87% input-capacitance reduction can be achieved over the conventional structure. A 10-bit SAR ADC with this proposed switching scheme is realized in 65 nm CMOS. With 1.514 KHz differential sinusoidal input signals sampled at 50 KS/s, the ADC achieves an SNDR of 61.4 dB and only consumes power of 450 nW. The area of this SAR ADC IP core is only 136 μm $\times$ 176 μm, making it also area-efficient and very suitable for biomedical electronics application.

1. Introduction

With the feature size of integrated circuits downscaled to nanoscale, the integration level of System-on-Chip (SoC: System-on-Chip) has been increased dramatically. For some special applications, such as battery-powered or wireless-powered implantable bioelectronics, low-power consumption and miniaturized size have become the key factors of the system. In these applications, the successive-approximation-register (SAR) ADCs, especially charge scaling SAR ADCs, are prevalent options for low-power A/D conversion. Recently, many publications are about the research on reducing the switching power of the D/A network in SAR ADC [1–8]. In [1], energy saving is achieved by splitting the most-significant bit (MSB) into several binary scaled capacitors. Monotonic downward switching scheme is proposed in [2], while V_{cm} is used in [3] for energy reduction. V_{cm}-based and monotonic switching are combined; hence more energy is saved in [4]. For the switching scheme in [5], no energy is consumed during generating the first 3 bits, making it more energy-efficient. Moreover, the method in [6] also achieves very low switching energy by using multiple references and sequence initialization. However, the static power consumed

during generating these additional subreferences diminishes its attraction. In this paper, an improved energy-efficient capacitor switching procedure for charge scaling SAR ADC is proposed. Instead of the resistive subreference generator used in [6], capacitive subconversion is used to generate the last 2 bits without any static power. For power-efficiency, area reduction, and easy realization in CMOS process, two 1-bit capacitor arrays are combined to generate the last 2 bits. This innovation comes from the attenuation capacitor based dual-array charge scaling structure [7], in which the attenuation capacitor would be an integral multiple of unit capacitor, $2C$, only when the LSB array just converts 1 bit [8]. Moreover, to verify the applicability of this proposed scheme, a 10-bit 50 KS/s SAR ADC that can be used in multichannel neural recording implant is realized in 65 nm CMOS. The application of this proposed SAR ADC in multichannel neural recording analog front-end is shown in Figure 1.

The rest of this paper is organized as follows. Section 2 shows the proposed switching scheme. The switching energy analysis and comparison are provided in Section 3. In Section 4, the design results of a 10-bit SAR ADC with this proposed scheme are given. Finally, Section 5 concludes this paper.
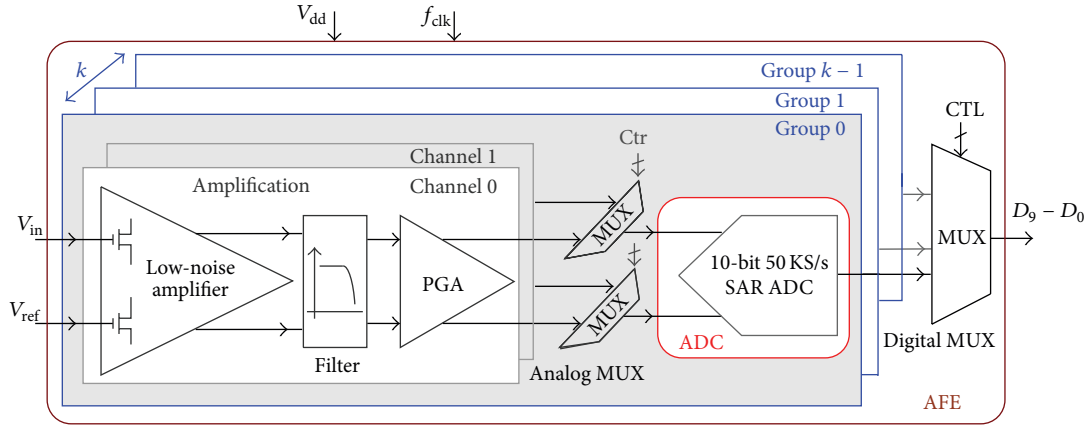
FIGURE 1: The application of SAR ADC in multichannel neural recording implant.

TABLE 1: Comparison with previous works for 10-bit SAR ADC.

Switching scheme	Area (C)	Average energy (CV_{ref}^2)	Accuracy requirement on subreferences
Conventional [1]	2048	1363.4	Not used
Cap splitting [1]	2048	852.3	Not used
Monotonic [2]	1024	255.5	Not used
V_{cm}-based [3]	1024	170.2	From MSB
Zhangming [4]	512	31.9	From MSB
Xingyuan [5]	512	−0.135	From the 3rd bit
Xingyuan [6]	256	31.4	The last 2 bits
Proposed	268	32.5	Not used

2. Proposed Switching Procedure

Figure 2 illustrates the proposed scheme in detail for a 5-bit SAR A/D conversion, which is realized by differential 2-bit capacitor arrays. Different from [6], subreferences $V_{ref}/2$, $V_{ref}/4$, and $3V_{ref}/4$ are generated capacitively for power-efficiency improvement.

During the sampling phase, the top-plates of these two differential capacitor arrays are connected to V_{ip} and V_{in} separately, while the connection of the bottom-plates is initiated to "0 1 1 1 1." This means the bottom-plate of the most-significant bit (MSB) capacitor is set to ground (Gnd), and these bottom-plates of the other capacitors are connected to V_{ref}. The sampling switches turn off and the first comparison starts at the end of the sample phase to generate the MSB. The switching energy consumed in each conversion step is shown in Figure 2. Thanks to the top-plate sampling, there is no switching energy taken from reference V_{ref} during the MSB generation. After the MSB is determined, the MSB capacitor on the lower voltage potential side is switched to V_{ref} to produce the 2nd bit. Since all these bottom-plates of this capacitor array are connected to the same DC voltage, V_{ref}, still no switching energy is taken from V_{ref} in the production of the 2nd bit. Once the 2nd bit is produced, the monotonic switching presented in [2] will be utilized in the subsequent conversion. According to [6], an improvement over [2] is that the variation of input common-mode voltage of the

comparator can be reduced because of $V_{ref}/2$ increase on the lower voltage potential side during the 2nd generation.

Figure 2(b) shows the generation of the last 2 bits in the proposed conversion. Since the operation of the proposed scheme is symmetrical, which can be seen from Figure 2(a), A1–B2 is used for this description. Additional reference voltage levels ($V_{ref}/2$, $V_{ref}/4$, and $3V_{ref}/4$) are needed. For energy reduction, we introduce a capacitive method, which is similar to a segmented charge redistribution conversion, to generate these subreferences. As shown in Figure 2(b), each segmented subarray is only used to generate 1 bit. Then, these two attenuation capacitors would be $2C$, making the process realization and matching of the subarray easier than a normal 2-bit array, in which the attenuation capacitor should be a non-integral multiple of unit capacitor, $4C/3$.
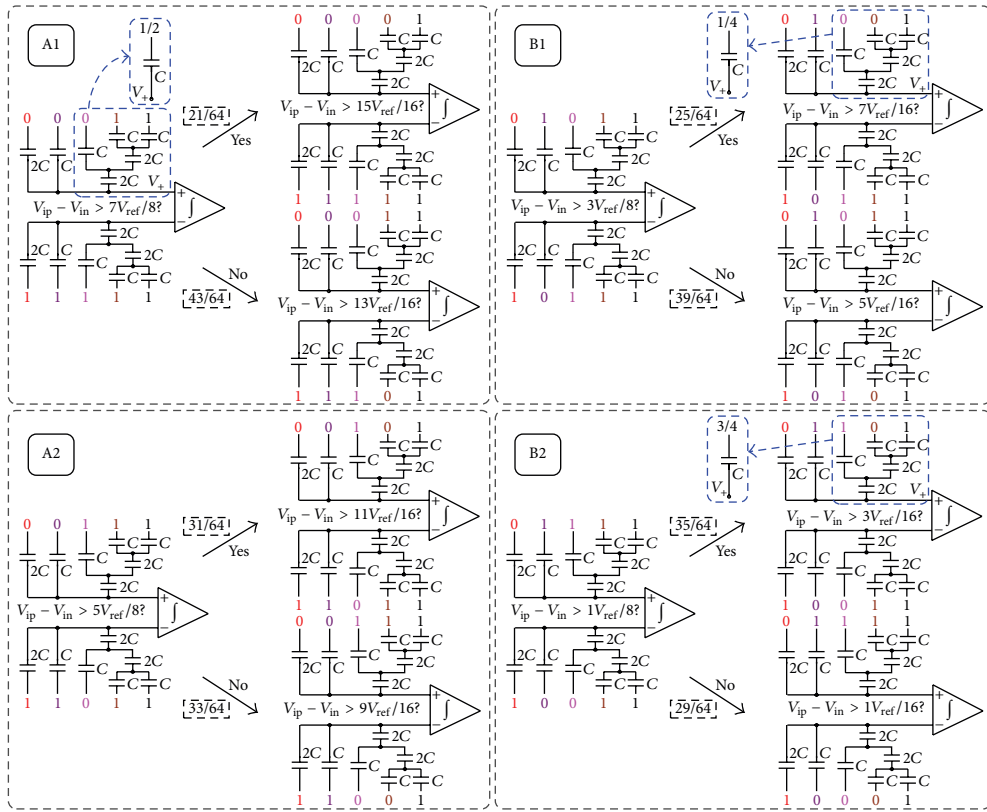
3. Switching Energy Analysis

The behavioral simulation in Matlab was performed for 10-bit SAR ADCs with different switching schemes. In the proposed scheme, 10-bit resolution is realized by a "7 + 1 + 1" 3-step segmented capacitor array. Figure 3 plots the switching energy versus digital code. Compared to the conventional architecture, the average energy and total capacitance of the proposed scheme are reduced by 97.6% and 87%, respectively.

Table 1 shows the comparison of different schemes with respect to the average switching energy and the capacitor
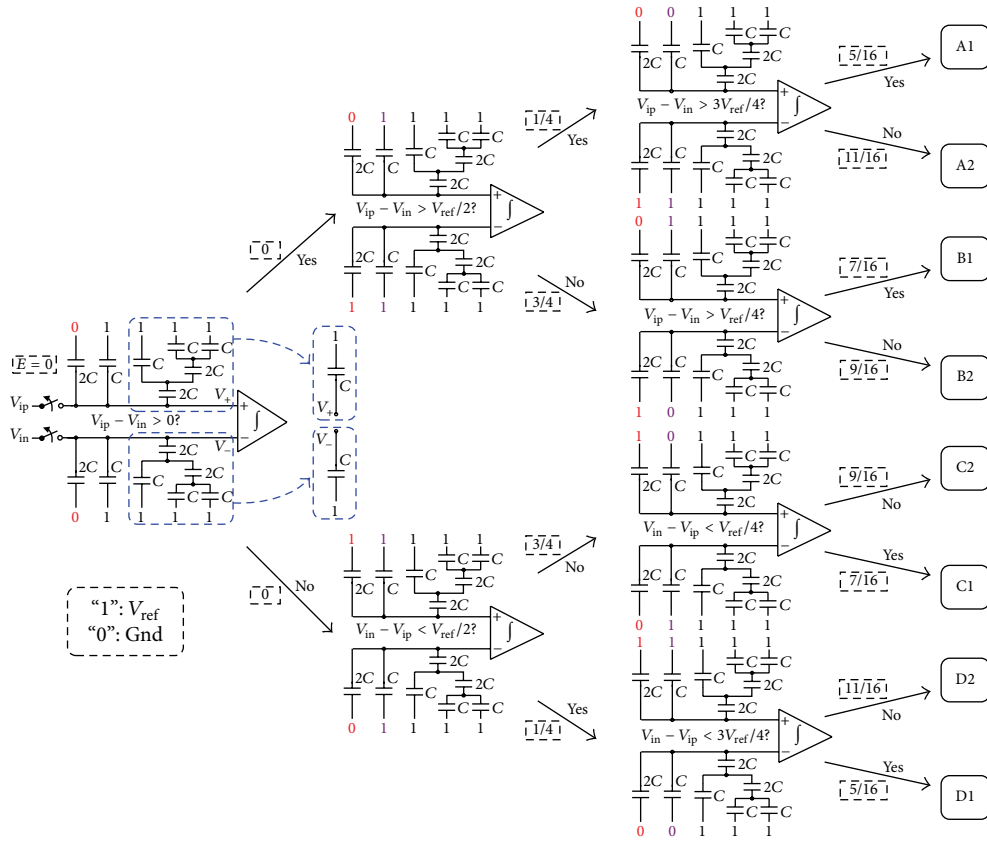
(a)

(b)

FIGURE 2: Proposed switching scheme and the energy consumption for 5-bit ADC.
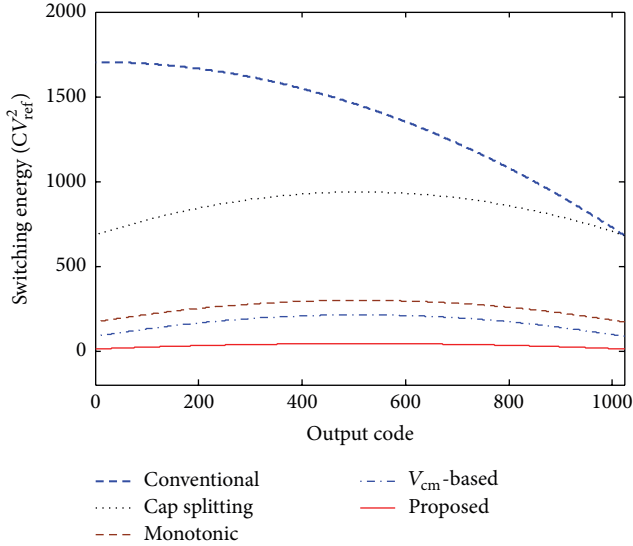
FIGURE 3: Switching energy versus output code.

array area. Compared with previous two-level schemes [1, 2], the proposed switching procedure is more efficient in energy and area. Compared with these schemes in [3–6], the advantage of this proposed scheme is two-level switching. This is similar to that in [1, 2], but the energy consumption has been dramatically reduced. For comprehensive comparison with the scheme proposed in [6], we also consider the static power consumed by the resistive subreference generator, which is only used for generating the last two bits. If the intermittent-mode reference generator proposed in [6] is utilized, the static power of the resistor string would be $P_{static} = kV_{ref}^2/R_{total}$, where R_{total} represents the total resistance of the resistor string and k is used to represent the power-on duty cycle of the intermittent reference generator. For biomedical application such as multichannel neural recording systems, if each recording channel has its own in-channel ADC, at least 20 KS/s sampling rate is needed for each ADC. Taking a 10-bit SAR ADC with 50 fF unit capacitor as an example, R_{total} should be around 100 KΩ for settling requirement. Taking $k = 0.2$ for 10-bit A/D conversion with 10 clock cycles and $V_{ref} = 1$ V, the static power consumed by the subreference generator is 2 μW, much more than nW-level switching power of the capacitor array. Obviously, significant improvement has been achieved in the proposed switching scheme over that in [6].

4. 10-Bit SAR ADC with the Proposed Scheme

Shown in Figure 4 is the architecture of a 10-bit SAR ADC with the proposed switching scheme. This fully differential SAR ADC is composed of sample switches, capacitor arrays, dynamic comparator, and SAR logic. Besides the proposed switching procedure in Section 2, dynamic comparator is also used in this design for power reduction [2]. To improve the switch linearity, bootstrapped switches are utilized to fix the gate-source voltages of the sampling MOSFETs at a constant voltage level [2].

In the structure proposed in Figure 5, combined C-$2C$ structure acts as the subconversion to generate subreferences $V_{ref}/2$, $V_{ref}/4$, and $3V_{ref}/4$. The attenuation capacitor is an integral multiple of unit capacitor, $2C$, which facilitates the matching to some extent in the layout design. However, the DC performance is sensitive to the parasitic capacitance of the attenuation capacitor, which has been proved in [7]. As shown in Figure 5, parasitic capacitance, C_{t1}, between the top-plate of C_{a1} and substrate will result in gain error of the ADC. Since it cannot affect the capacitors' binary ratio, it will not cause any nonlinearity. In Figure 5, C_{b0} is composed of the top-plate parasitic capacitance of C_0 and C_1 and the bottom-plate parasitic capacitance of C_{a0}, while C_{b1} is made up of the top-plate parasitic capacitance of C_{a0} and C_2 and the bottom-plate parasitic capacitance of C_{a1}. These two parasitic capacitors, C_{b0} and C_{b1}, will lead to nonlinearity of SAR ADC, because they can affect the equivalent capacitance of the subconversion array. However, the subconversion array is only used to generate the last 2-bit output of the ADC, so the requirement for the accuracy of these subreferences is not too stringent.

A 10-bit SAR ADC with this proposed switching scheme is realized in a 65 nm CMOS process. To analyze the effect of parasitic capacitance on the ADC performance, comparison is made from the simulated results in Figure 6. Shown in Figure 6(a) is the simulation result of a 10-bit ADC without any parasitic capacitance in the capacitor array, while Figure 6(b) shows the simulation result with 10% bottom-plate parasitic capacitance and 5% top-plate parasitic capacitance. There is only 2 dB decrease in the SNDR, which would be acceptable for a 10-bit ADC.

This 10-bit SAR ADC IP core occupied a total active area of 136 μm × 176 μm. Metal-Oxide-Metal (MOM) capacitors are used in this ADC. To improve the matching performance and make the input noise much less than the quantization noise, the unit capacitance is selected to be 32.3 fF. Each capacitor array has 134 unit capacitors. Therefore, the input capacitance of each capacitor array is around 4.3 pF. Furthermore, during the layout design, these capacitors in the subarray are carefully placed and connected to reduce the effect of C_{b0} and C_{b1} on the linearity performance of the ADC. Shown in Figure 7 is the simulated linearity performance of this 10-bit SAR ADC with proposed switching procedure. The differential nonlinearity (DNL) is 0.61 LSB/−0.92 LSB, and the integral nonlinearity (INL) is ±0.88 LSB. When 1.514 KHz differential sinusoidal input signals are sampled at 50 KS/s, the ADC achieves an SNDR of 61.4 dB. The power consumption is less than 450 nW. The Figure-of-Merit (FoM) is around 9.5 fJ/conversion step.

5. Conclusion

An improved energy-efficient capacitor switching scheme has been presented for low-power SAR ADC in implantable bioelectronic applications. By using capacitive subconversion, this proposed two-level scheme achieved higher resolution, smaller area, and higher energy-efficiency, compared with other two-level schemes in previous works. Compared to the conventional scheme, over 97.6% of average switching
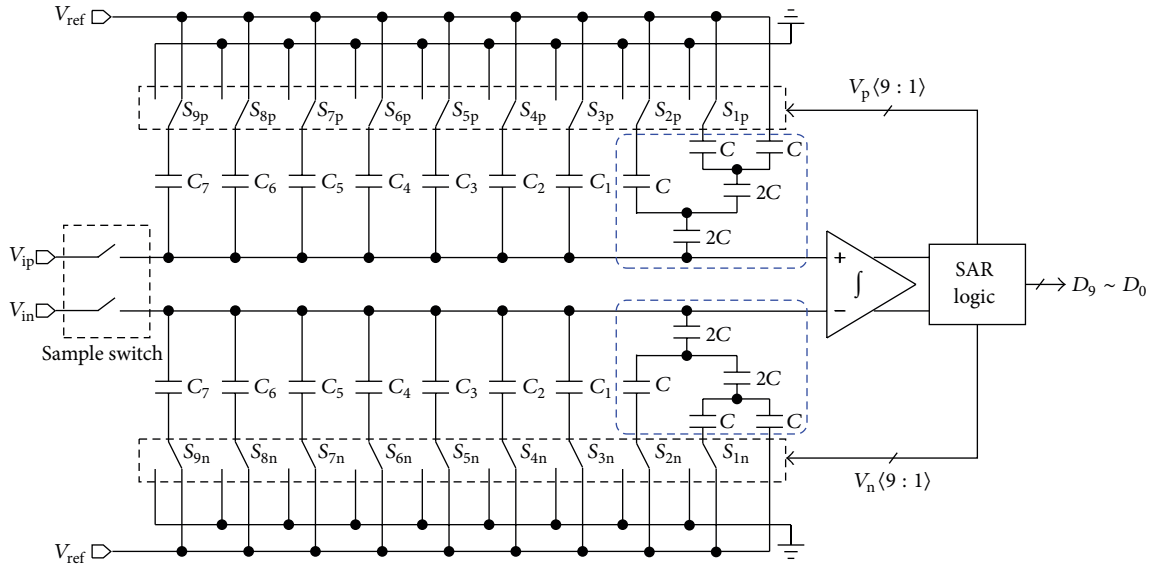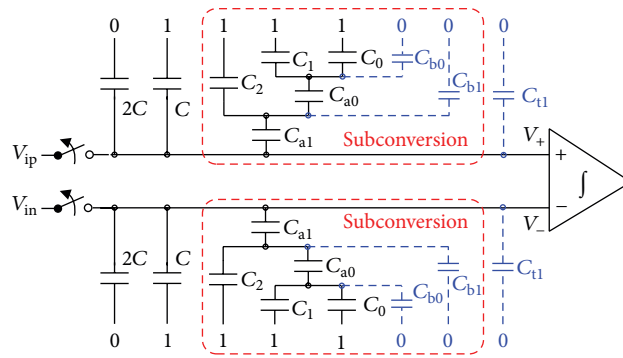
FIGURE 4: A 10-bit SAR ADC with the proposed scheme.

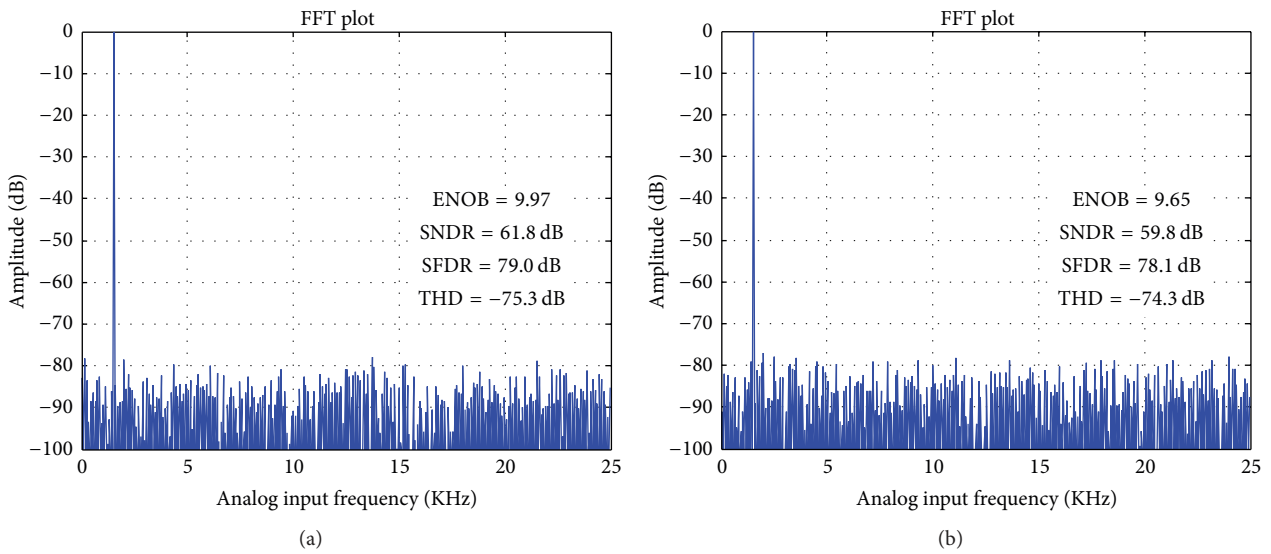FIGURE 5: Illustration of the parasitic capacitance in C-$2C$ subconversion.

(a)

(b)

FIGURE 6: The simulation results of a 10-bit ADC with this proposed switching scheme (a) without parasitic capacitance and (b) with parasitic capacitance.
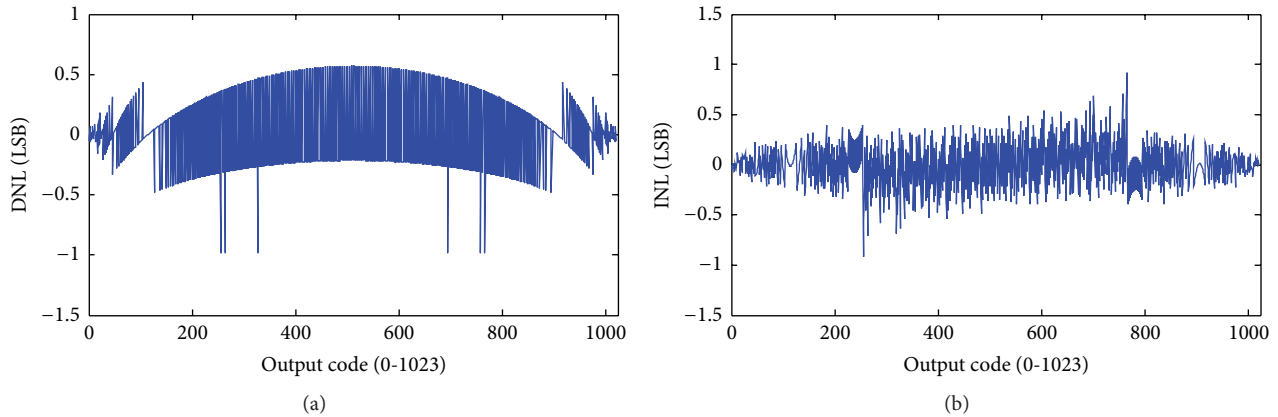
(a)

(b)

FIGURE 7: Nonlinearity of the 10-bit SAR ADC: (a) DNL and (b) INL.

energy and about 87% of unit capacitors in the capacitor array have been reduced. The superiority and applicability of this proposed switching scheme were also proven by the realization of a 10-bit 65 nm CMOS SAR ADC.
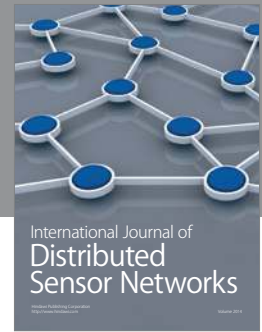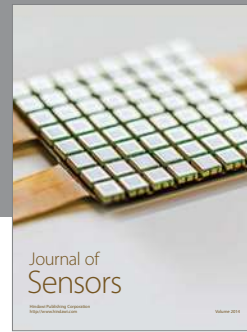
Competing Interests

The authors declare that they have no competing interests.

Acknowledgments

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