IMPROVEMENTS IN BIASING AND COMPENSATION OF CMOS OPAMPS

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ABSTRACT

In this paper, we present modifications to the constant-gm bias circuit and the Miller-lead compensation technique which eliminate or minimize some of their shortcomings. First, we demonstrate how parasitic pad capacitance can cause instability in the constant-gm bias circuit, and show that the transconductance is constant only for specific bias conditions. Next, we suggest a new circuit topology that requires 75% less compensation capacitance to achieve stability. We also discuss problems with Miller-lead compensation that arise from temperature, process, and load variations. Finally, we present a new biasing technique to correct these problems, and, through simulation, demonstrate a 40º improvement in phase margin over load current variations.

1. INTRODUCTION

Operational amplifiers are typically biased and compensated to minimize temperature and process variations in their open loop response. Although *constant-gm* biasing and *Miller-lead* compensation remain useful for this purpose, the sensitivity of these techniques can be improved over temperature, process, and load variations.

To understand how the open loop characteristics of an opamp can vary, consider the opamp in Figure 1.

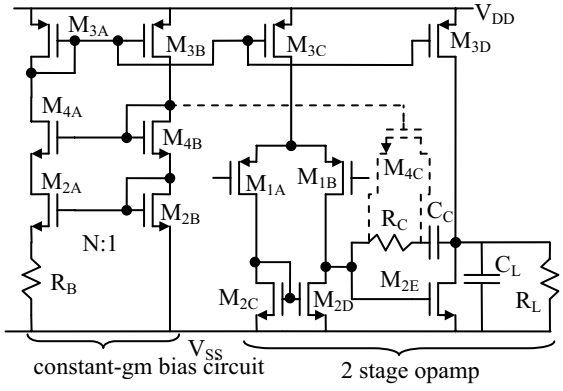

Figure 1: A 2 stage opamp with constant-gm biasing. In all figures, devices with the same numeric index are matched devices.

The pole and zero locations of the open loop response are given by (1)-(3), where R_C is either a passive resistor, or implemented using the channel resistance of M_{4C} operating in the triode region [1]. Typically, the opamp is designed such that $f_T < f_Z < f_2$. Assuming dominant pole behavior, f_T is given by (4).

$$f_1 = \frac{1}{2\pi gm_{2E} C_C R_{O1} R_{O2}} \quad (1) \qquad f_2 = \frac{-gm_{2E}}{2\pi(C_C + C_L)} \quad (2)$$

$$f_Z \approx \frac{-1}{2\pi R_C C_C} \quad (3) \qquad f_T \approx \frac{gm_1}{2\pi C_C} \quad (4)$$

Clearly, changes in gm_1, gm_2, R_C, and I_{D2E} caused by process, temperature, and load variations will affect the relationship between f_T, f_Z, and f_2. In contrast, an ideal biasing scheme would render f_1, f_2, f_Z, and f_T constant.

The constant-gm bias circuit and the use of a MOSFET R_C for compensation have numerous disadvantages. In Section II, we show that the constant-gm bias circuit does not always keep gm constant, and indicate exactly how variations in *gm* arise. We also demonstrate that the constant-*gm* bias circuit can be unstable. In Section III, we introduce a new constant-gm bias circuit with improved stability. Section IV discusses disadvantages of the MOSFET implementation of R_C shown in Figure 1, and introduces an improved technique for biasing M_{4C} for compensation.

2. LIMITATIONS IN TRACKING GM

Ideally, the constant-gm bias circuit in Figure 1 forces all MOSFETs (n/p-channel) to have constant *gm* over process and temperature [1,2]. Unfortunately, the application of constant-*gm* biasing to CMOS opamps is complicated by the MOSFET I-V characteristics. While one equation governs the I-V characteristics of the BJT for the entire active region, the I-V characteristics of the MOSFET change from weak to strong inversion. In this section, we investigate variations in gm caused when a constant-*gm* bias circuit with MOSFETs operating in a particular region of operation is used to bias other MOSFETs in either the same, or a different, region of operation.

Case A. Strong Inversion Only

Traditionally, all MOSFETs were biased in strong inversion where the I_D-V_{GS} relationship was governed by the square law. In such a case, consider any MOSFET M_X biased by the constant-*gm* circuit in Figure 1. The drain current of M_{2B} (I_{D2B}) and gm_X are given by (5) and (6) respectively, where μ_X is either μ_n or μ_p depending on the device type. Substituting (5) into (6) yields (7), an expression for gm_X. If M_X and M_{2B}

are both n-channel MOSFETs, then (7) is independent of process and temperature. On the other hand, if M_X is a p-channel MOSFET, then the final term in (7) (μ_p/μ_n) varies extensively with process and slightly with temperature.

$$I_{D2B} = \frac{1}{R_B^2}\left(1-\frac{1}{\sqrt{N}}\right)\left(\frac{2}{\mu_n C_{OX}(W/L)_{2B}}\right) \quad (5)$$

$$gm_X = \sqrt{2\mu_n C_{OX}(W/L)_X I_{DX}} \quad (6)$$

$$gm_X = \sqrt{\frac{2}{R_B^2}\left(1-\frac{1}{\sqrt{N}}\right)\left(\frac{(W/L)_X}{(W/L)_{2B}}\right)\left(\frac{\mu_X}{\mu_n}\right)} \quad (7)$$

Case B. Strong Inversion (M_{2B}) and Weak Inversion (M_X)
Consider the case where M_X is in weak inversion and M_{2B} is in strong inversion. In weak inversion, gm_X is given by (8), where ϕ_t is the thermal voltage, and n is the slope factor ($n \approx 1.2$) [3].

$$gm_X = \frac{I_{DX}}{n\phi_t} \quad (8)$$

Substituting the original expression for I_{D2B} (and therefore I_{DX}) into (8), yields (9) which again depends on temperature (ϕ_t, μ_n) and process (μ_n).

$$gm_X = \frac{1}{n\phi_t R_B^2}\left(1-\frac{1}{\sqrt{N}}\right)\left(\frac{2}{\mu_n C_{OX}(W/L)_{2B}}\right) \quad (9)$$

Case C. Weak Inversion Only
If M_{2B} is also in weak inversion, the expression for I_{D2B} (and therefore I_{DX}) is given by (10), and the resulting expression for gm_X given by (11). Clearly, gm_X is constant once again, with an advantage over strong inversion (case A): *the ratio μ_X/μ_n is absent from the expression for gm_X.* Therefore, gm_X is independent of process and temperature, *even if M_X and M_{2B} are different types*.

$$I_{D2B} = \frac{n\phi_t}{R_B}\ln(N) \quad (10)$$

$$gm_X = \frac{1}{R_B}\ln(N) \quad (11)$$

Case D. Weak Inversion (M_{2B}) and Strong Inversion (M_X)
When M_{2B} is in weak inversion and M_X is in strong inversion, gm_X is given by (12).

$$gm_X = \sqrt{2\mu_n C_{OX}(W/L)_X \frac{n\phi_t}{R_B}\ln(N)} \quad (12)$$

Once again, gm_X varies with process and temperature. However, on account of the square root dependence of gm on I_D in strong inversion, the variations in (12) are less than in (10). Note that if R_B is integrated on chip, process variations in R_B influence (12) less than (7), (9), or (11).

In addition to our analysis, we simulated cases A-D in a 0.8µm BiCMOS process using HSPICE. In our simulations, all MOSFETs had identical drain currents regardless of their region of operation. Furthermore, all MOSFETs in a given region of operation had the same $V_{GS} - V_{T0}$, regardless of their type (p or n channel). We swept the simulator temperature from 0ºC to 50ºC, and used corner models to simulate process variations. Table 1 shows our results. Except where indicated, M_{2B} and M_X in Table 1 are n-channel MOSFETs.

Table 1. Process and temperature variations in the gm of MOSFETs biased with a constant-gm bias circuit.

Case	M_{2B} (n-channel)	M_X	Temp (0ºC-50ºC)	Process
A	str. inv.	str. inv.	0.5%	0.1%
A	str. inv.	str. inv. (p-channel)	1%	13%
B	str. inv.	weak inv.	8%	7%
C	weak inv.	weak inv.	0.2%	1%
C	weak. inv.	weak inv. (p-channel)	0.2%	5%
D	weak inv.	str. inv.	5%	4%

Based on our analysis and simulations we can draw several conclusions:

- M_X and M_{2B} must *always* have the same bias point (same V_{GS} - V_{T0}) to keep gm_X constant over temperature and/or process [4].
- For MOSFETs in strong inversion, M_X and M_{2B} must be the same type (n or p-channel) to obtain constant gm over temperature *and* process.
- To obtain *only temperature independence* of gm_X in strong inversion, M_X and M_{2B} may be different types, *provided that the ratio μ_X/μ_n does not vary significantly with temperature.*
- For MOSFETs in weak inversion (and BJTs in general), temperature *and* process independence may be achieved even when M_X and M_{2B} are different types.

3. STABILITY IN CONSTANT-GM BIASING

Another problem with the constant-gm bias circuit is that it can oscillate if not designed correctly. Typically, R_B is implemented off-chip, and therefore a capacitance of several pF may be present in parallel with R_B, as shown in Figure 2 [5].

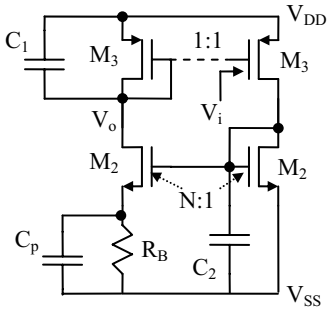

Figure 2: A simplified schematic of the constant-gm bias circuit, useful for small signal analysis.

Consider breaking the feedback loop between the gates of M_{3A} and M_{3B}, and applying an input signal at the gate of M_{3B}. Using small signal analysis, V_o/V_i is given by (13). Note that the loop gain from V_i to V_o is positive.

$$\frac{V_o}{V_i} = \frac{\overbrace{(gm_{2B}/gm_{2A})}^{\text{DC gain}}\overbrace{(sC_PR_B+1)}^{z_1}}{\underbrace{(sC_1/gm_3+1)}_{p_2}\underbrace{(sC_2/gm_{2B}+1)}_{p_3}\underbrace{(sC_PR_B+gm_{2A}R_B+1)}_{p_1}} \quad (13)$$

Typically, parasitic capacitances C_1 and C_2 are very small compared to C_P. In this case, p_1 and z_1 form a dominant pole-zero doublet, where the zero is always lower than the pole. If gm_{2A} is too large, then z_1 and p_1 move further apart, and $|V_o/V_i|$ can become greater than 0dB, as shown in Figure 3. When $|V_o/V_i| > 0$dB, the phase lag introduced by p_2 and p_3 can cause instability.

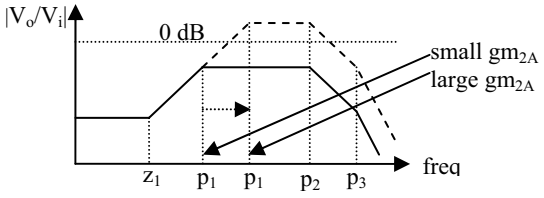

Figure 3: Magnitude plots for the constant-gm open loop function in (13)

To ensure stability, a compensation capacitor can be added to increase either C_1 or C_2, thereby creating a pole dominant over p_1. Unfortunately, p_2 and p_3 are formed by low impedance nodes, necessitating a compensation capacitance on the order of C_P. For example, to ensure stability with C_2, inequality (14) must be satisfied.

$$C_2 > \left(\frac{gm_{2A}R_B}{gm_{2A}R_B+1}\right)C_P \approx C_P \quad (14)$$

4. A NEW CONSTANT-GM BIAS CIRCUIT

Modifying the constant-*gm* circuit in Figure 2 to include a high impedance node reduces the size of the compensation capacitor needed to ensure stability. Shown in Figure 4 is the modified constant-*gm* circuit, which was originally presented in [5].

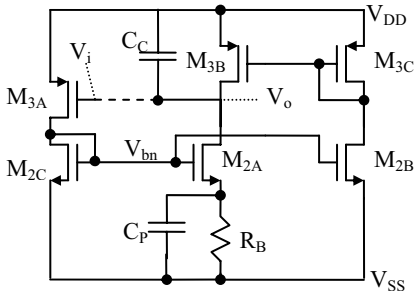

Figure 4: A new constant-gm bias circuit with a high impedance node.

MOSFETs M_{3B}, M_{3C}, M_{2A}, and M_{2B} form the original constant-*gm* circuit. However, the addition of M_{3A} and M_{2C} makes V_o a high impedance node. A compensation capacitor (C_C) is placed at the high impedance node. Ignoring the degeneration of ro_{2A}, the open loop transfer function of the new constant-gm circuit is approximately given by (15).

$$\frac{V_o}{V_i} = \frac{\overbrace{\left(\frac{gm_3}{gm_{2A}R_B}\left(\frac{gm_{2A}}{gm_{2B}}-1\right)^2[ro_3 // ro_{2A}]\right)}^{\text{DC gain}}\overbrace{\left(sC_P\left[\frac{gm_{2A}-gm_{2B}}{gm_{2B}gm_{2A}}\right]-1\right)}^{z_1}}{\underbrace{(1+sC_C[ro_3 // ro_{2A}])}_{p_D}\underbrace{(sC_PR_B+gm_{2A}R_B+1)}_{p_1}} \quad (15)$$

The new transfer function contains the original pole formed by C_P and R_B, but also has a new dominant pole formed by C_C and $ro_{2B}//ro_3$. Alternatively, C_C can be connected between V_o and V_{bn} instead of between V_o and V_{DD}. Connecting C_C to V_{bn} takes advantage of the Miller effect introduced by the voltage gain from V_o to V_{bn}. If necessary, a resistor can be added in series with C_C to introduce lead compensation.

To demonstrate the improved stability of the proposed constant-*gm* bias circuit, we simulated the circuits in Figure 2 and Figure 4 with C_2=4pF and C_C=1pF compensation capacitors, respectively. We designed both circuits to have the same bias currents and transistor sizes. As shown in Figure 5, the proposed circuit is stable, despite its smaller compensation capacitor.

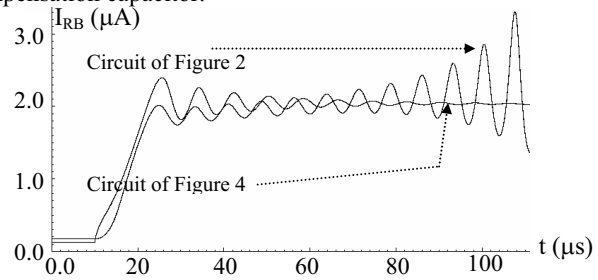

Figure 5: Start-up simulations showing instability in the traditional constant-gm bias circuit. C_P = 40pF in both cases.

5. A GM-TRACKING LEAD COMPENSATION BIASING TECHNIQUE

The non-dominant pole (f_2) and the zero (f_Z) of a 2 stage miller-lead compensated opamp depend on gm_{2E} and R_C, respectively.

$$f_Z \approx \frac{-1}{2\pi R_C C_C} \qquad f_2 = \frac{-gm_{2E}}{2\pi(C_C+C_L)}$$

If R_C could be forced to track $1/gm_{2E}$ over process and temperature, then f_Z would track f_2, thereby improving phase margin. Typically, this is accomplished through the use of stacked diode-connected MOSFETs as shown in Figure 1, where $V_{GS2B} = V_{GS2E}$, so that $V_{GS4C} = V_{GS4B}$. At steady state the effective resistance of M_{4C} in the triode region tracks $1/gm_{2E}$. However, during transience ($I_L \neq 0$), the gate-source voltages of the biasing transistors do not track V_{GS2E}. Shown in Figure

6 is an alternative circuit that forces R_{DS4C} to track gm_{2E} directly, even when $V_{GS2E} \neq V_{GS2B}$.

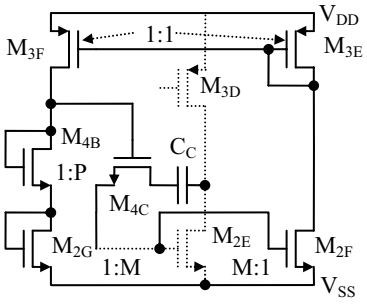

Figure 6: A new gm-tracking lead compensation resistor.

M_{2E} and M_{3D} once again form the 2nd stage of an amplifier like the one in Figure 1. M_{2F} mirrors the current in M_{2E}, and forces the same current through M_{3F}, M_{4B}, and M_{2G}. Therefore $V_{GS2G} = V_{GS2E}$, and R_{DS4C} is given by (16), which is always independent of process, temperature, and load variations. Parameters M and P represent the transistor width ratios shown in Figure 6.

$$R_{DS4C} = \frac{1}{gm_{2E}}\left(\frac{M}{P}\right) \tag{16}$$

To test the *gm*-tracking performance and stability of the circuit proposed in Figure 6, we designed three 2-stage opamps. All opamps have the architecture of the opamp in Figure 1 but use different lead compensation biasing techniques:

- Opamp A: passive R_C, as shown in Figure 1.
- Opamp B: MOSFET R_C, as shown in Figure 1.
- Opamp C: MOSFET R_C, as shown in Figure 6.

We tested the phase margin and stability of the opamps over load current variations by simulating them in open loop with current sinks attached to their outputs. Although opamps are rarely loaded with ideal current sources, the constant current source provides a convenient method of obtaining the frequency response under a variety of load conditions. We recorded the phase margin as we increased I_L from 0μA to 110μA, or 95% of the 2nd stage bias current. As shown in Figure 7 the phase margin for opamp C (where f_Z tracks f_2) is better under load than opamps A and B.

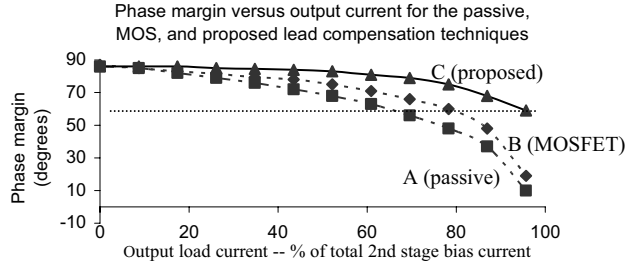

Figure 7: Phase margin vs. I_{LOAD} for opamps A, B, and C.

To test the step response of the proposed circuit, we connected opamps B and C in non-inverting configuration with a closed loop gain of 6dB. We applied an input voltage pulse of 1.0V, and recorded the output voltages of the opamps, which are shown in Figure 8. Opamp B shows oscillations that arise because M_{4C} enters saturation. The oscillations are not present in the proposed circuit.

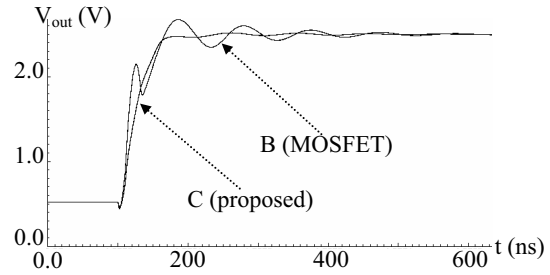

Figure 8: Output voltages for opamps B, and C during a step response simulation

Note that rising steps such as the one in Figure 6 can cause an opamp to slew if M_{2E} enters cutoff. In our proposed circuit in Figure 6, M_{2F} and M_{2G} would also enter cutoff, causing M_{4C} to become an open circuit. In this situation, the opamp would lose compensation and become unstable, but *only for the duration of the rising edge*. This problem has two simple yet effective solutions: (1) A constant bias current much smaller than I_{D3F} can be introduced in parallel with M_{3F}, or (2) a diode connected MOSFET with high channel resistance (large *L*) can be added in parallel with M_{4C} *or* between M_{4B} and the gate of M_{4C}.. The simulation results in Figure 8 were obtained after implementation of the first solution.

6. CONCLUSION

We have shown that, in general, the use of a constant gm bias circuit does not ensure constant transconductance throughout an integrated circuit, and have provided specific guidelines to minimize any variation. We have also demonstrated improved stability by adding a high impedance node to the constant-gm bias circuit. In fact, the same general technique and architectural modification can be applied to other current and voltage reference circuits. Finally, we have proposed a lead compensation biasing technique that improves opamp large signal settling time, and stability under load.

7. REFERENCES

[1] K. Martin, D.A. Johns, *Analog integrated circuit design*, New York: John Wiley & Sons Inc., 1997.

[2] A. McLaren, and K. Martin, "Generation of Accurate On-Chip Time Constants and Stable Transconductances," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, April 2001.

[3] A.I.A. Cunha, M.C. Schneider, C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, Oct. 1998.

[4] J. M. Steininger, "Understanding wide-band MOS transistors," *IEEE Circuits and Devices*, vol. 6, pp. 26-36, May 1990.

[5] T. Pialis, "Design and Analysis Techniques for Low-Voltage, Low-Jitter Voltage-Controlled Oscillators," *M.Eng. Design Project Report*, University of Toronto, Department of Electrical Engineering, Toronto, 2002.