Improving Accuracy and Energy Efficiency of Pipeline Analog to Digital Converters

by

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To Mom and Dad

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Abstract

Analog-to-Digital converters (ADC) are key building blocks of analog and mixed-signal processing that link the natural world of analog signals and the world of digital processing. This work describes the analysis, design, development and test of novel high-resolution (≥12-bit), moderate speed (10-100MS/s), energy-efficient ADCs. Such ADCs are typically used for communication, imaging and video applications.

CMOS process scaling is typically aimed at enabling fast, low-power digital circuits. Scaling leads to lower supply voltages, and to short channel devices with low gain and poor matching between small devices. On the other hand, to process and amplify analog signals analog circuits rely on wide signal swing, large transistor gain and good component matching. Hence, analog circuit performance has lagged far behind digital performance. Analog circuits such as ADCs are therefore nowadays performance bottlenecks in many electronic systems.

The pipeline ADC is a popular architecture for implementing ADCs with a wide range of speed and resolution. This work aims to improve the accuracy and energy efficiency of the pipeline architecture by combining it with more accurate or more energy efficient architectures such as Sigma-Delta (ΣΔ) and Successive-Approximation (SAR). Such novel, hybrid architectures are investigated in this work.

In the first design, a new architecture is developed which combines a low-OSR resetting ΣΔ modulator architecture with the pipeline architecture. This architecture

enhances the accuracy and energy efficiency of the pipeline architecture. A prototype 14-bit 23MS/s ADC, based on this new architecture, is designed and tested. This ADC achieves calibration-free 14-bit linearity, 11.7-bit ENOB and 87dB SFDR while dissipating only 48mW of power.

In the second design, new hybrid architecture based on SAR and pipeline architecture is developed. This architecture significantly improves the energy efficiency of the pipeline architecture. A prototype 12-bit 50MS/s ADC is designed based on this new architecture. “Half-gain” and “half-reference” pipeline stages are also introduced in this prototype for the first time to further reduce power dissipation. This ADC dissipates only 3.5mW power.

CHAPTER 1

INTRODUCTION

1.1 Background

Since the advent of digital solid-state electronics in the early 1950s, digital processing power has grown by leaps and bounds fueled by the advances in integrated-circuit (IC) technology. Moore's law [1] predicts that, the number of transistors that can be placed inexpensively on an IC, doubles every two years. This exponential increase in digital processing power over the last half century, or so, is expected to continue for at least another decade [2].

All naturally occurring signals in the world e.g. sound, images, pressure, temperature, etc., have stubbornly remained analog in nature. This means that information in these signals is represented by continuous variables, having an infinite number of possible values. Most of the processing, storage and transmission of electronic data, nowadays, is digital in nature. Therefore, naturally occurring analog signals, having an infinite number of possible levels, need to be converted to digital signals with distinct quantized levels and vice-versa. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) perform these functions, respectively. Although this thesis pertains to the design of ADCs and not DACs, ADCs employ DACs is some form or

another to function. Fig. 1.1 shows the silicon egg concept [3] where the real analog world communicates with digital processing through a thin eggshell representing mixed-signal processing of which ADCs are an integral part. Thus ADCs are indispensible, key components of many electronic systems that require a link between the natural 'analog' world and the world of digital processing. Examples of such electronic devices are cell phones, digital still and video cameras, computers, digital music players, etc. DACs compliment ADCs in such data communications.

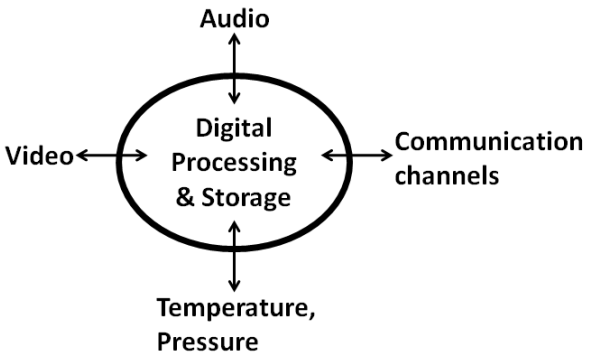

Fig. 1.1: The silicon egg concept proposed by Prof. Paul Gray [3]

This work concentrates on high-resolution (≥12-bits), moderate-speed (10–100MHz), low power ADCs that are typically used for communication, imaging and video applications.

1.2 Analog Design Challenges

CMOS technology has been the predominant choice for implementing digital circuits because of advantages such as near-zero static power, high density and device scalability.

Aggressive device scaling in modern CMOS technology enables the high-speed and high-density digital circuits that have sustained Moore's law for the past half century. On the other hand, analog circuits, such as ADCs, have not been able to take advantage of this aggressive scaling. This is because of the following reasons:

A. Low Voltage Supply

Device scaling requires the supply voltage to scale down in order to keep electric fields within the device unchanged and hence maintain device reliability [4]. This is disadvantageous for analog circuits as they rely on large signal swings in order to obtain large signal power and a wide dynamic range.

B. Poor Matching

As devices get smaller with scaling, matching between them becomes poorer [5]. Analog circuits rely on good component matching to process analog signals [6]. For example, comparators rely on good matching between transistors to give accurate decisions.

C. Poor Linearity

Short channel transistors in scaled CMOS processes suffer from low and non-linear output resistance [7]. This degrades the gain and linearity of the transistor. Analog circuits rely on large transistor gain and linearity to process and amplify analog signals.

These three issues significantly affect analog design in advanced CMOS technologies. It has been shown [8] that the clock rate of the digital circuits doubles every 2.3 years and the performance in MIPS (Million Instructions Per Second) doubles every 1.5 years. On the other hand, the relative performance of analog circuits, measured as the

product of ADC sampling rate and resolution, doubles every 4.7 years. Over the last 15 years, digital performance has increased 150 times more than analog performance (Fig. 1.2).

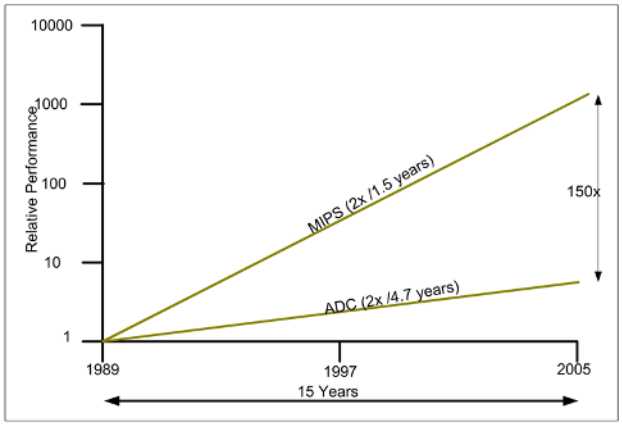

Fig. 1.2: Analog digital performance comparison [8]

1.3 Analog Design Techniques

Some of the important analog design techniques, that are used to overcome the above mentioned design constraints, include the following:

A. Offset Compensation

Offset compensation techniques reduce offsets present due to transistor mismatches [9]. In these techniques, the offset of the transistor is estimated in an idle phase and is compensated in the active phase. These techniques are well suited for circuits having an idle phase of operation e.g. switched capacitor circuits.

B. Digital Calibration

Technology scaling has helped digital circuits tremendously as compared to analog circuits. Hence, there is a trend of shifting design complexity from the analog

domain to the digital domain. Digital calibration techniques [10] have been able to compensate for poor analog gain, linearity and matching.

C. Digital Selection

In this novel technique [11], redundant analog circuits are built and the good ones are selected to achieve good performance. This technique is well suited for analog circuits that are limited in performance because of device mismatches alone e.g. comparators and flash ADCs.

D. Time Domain Resolution

Technology scaling has enabled fast transistors while reducing supply voltages. This implies that scaling improves 'time-resolution', but degrades 'voltage-resolution'. This idea has led to a technique in which time, rather than voltage, is resolved in a scaled CMOS process [12].

Despite such novel techniques, analog performance has still lagged far behind digital performance (Fig. 1.2).

1.4 Basic ADC Architecture

The flash ADC architecture is the simplest of ADC architectures. Most other ADC architectures are either derivatives of the flash ADC or employ it in some form or the other. An N-bit flash ADC (Fig. 1.3) consists of 3 main components:

- Comparator bank consisting of 2^N-1 comparators
- Reference ladder which provides 2^N-1 reference voltages
- Thermometer to binary encoder

Each comparator in the comparator bank has 2 inputs. One connected to the ADC input, the other connected to the reference ladder. If the input signal exceeds the reference voltage of a comparator, the output of the comparator will be 'high', otherwise it will be 'low'. The output of the comparator bank forms a thermometer code, where the transition between the 'high' and 'low' output comparators gives a measure of the input voltage with respect to the reference voltage (V_{ref}). A thermometer-to-binary encoder encodes the 2^N-1 bit thermometer code into an N-bit binary code.

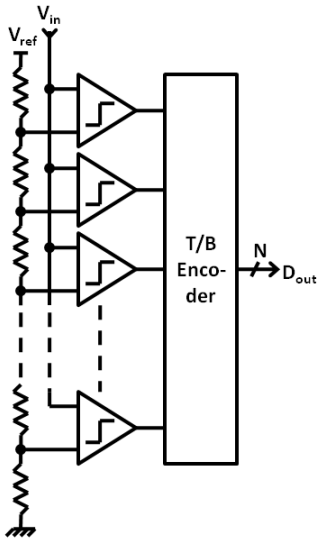

Fig. 1.3: N-bit flash ADC

1.5 ADC Performance Parameters

The most important ADC parameters are its resolution and conversion speed. These parameters are useful in specifying the ideal characteristics of an ADC. However, in practice ADC performance deviates from its ideal performance. Therefore, other

performance parameters [13] have been devised to characterize ADCs. They are divided into two categories of static and dynamic parameters.

A. Static Parameters

Static parameters, as the name suggests, pertain to the performance of the ADC with respect to some static or dc input voltage. These parameters are namely, the differential non-linearity (DNL) and integral non-linearity (INL). ADC step-size is defined as the smallest change in input voltage required, to obtain a unit change in the output code. For an ideal ADC, the step-size is uniform. DNL, for the i^{th} code transition, is defined as the difference between the actual step-size and the ideal step size that causes the transition:

$$DNL_i = \text{Actual step-size for } i^{th} \text{ code transition} - \text{Ideal step-size} \quad (1.1)$$

INL, for the i^{th} code, is defined as follows (assuming ADC codes start from i=0):

$$INL_i = \sum_{j=0}^{i} DNL_j \quad (1.2)$$

Thus DNL and INL parameters capture the deviation in step sizes of the ADC. Both DNL and INL are measured in LSB (Least Significant Bit). One LSB corresponds to the ideal step size of the ADC.

B. Dynamic Parameters

Dynamic parameters are a measure of the ADC performance with respect to a time-varying input signal. Some of the important dynamic performance parameters are SNR (Signal-to-Noise Ratio), SNDR (Signal-to-Noise and Distortion Ratio), ENOB (Effective Number Of Bits), and SFDR (Spurious Free Dynamic Range). To measure

these parameters, a pure sinusoid input is fed to the ADC and the ADC output spectrum is analyzed using techniques such as Fast Fourier Transform (FFT). The ratio of sinusoid power to total noise power at the output is the SNDR of the ADC. SNR is the ratio of sinusoid power to total noise power excluding harmonic distortion. From the SNDR (in dB) we can calculate ENOB as follows:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR(dB)} - 1.76}{6.02} \tag{1.3}$$

The ratio of the sinusoid power to the largest interferer power is the SFDR of the ADC.

C. Figure of Merit (FOM)

Another important ADC parameter is the power consumption of the ADC. Usually a high-speed, or high-resolution ADC will consume more power as compared to its low-speed or low-resolution counterpart. To compare ADCs with different speeds and resolutions a figure-of-merit (FOM) has been devised [14] that normalizes an ADC's speed, resolution and power consumption to a single performance parameter. This FOM is given by:

$$\mathrm{FOM} = \frac{\mathrm{P}}{(2\mathrm{BW}) * 2^{\mathrm{ENOB}}} \tag{1.4}$$

Where P is the power consumption of the ADC, ENOB is calculated from SNDR (equation 1.3) and BW is the effective bandwidth or Nyquist frequency (whichever is smaller) of the ADC. This FOM has units of energy per conversion-step.

1.6 Contributions of this Work

Hybrid ADC architecture is a combination of two or more conventional ADC architectures such as pipeline, flash, successive-approximation (SAR) or sigma-delta (ΣΔ) architectures. The major contributions of this work are the development, analysis and design of hybrid ADC architectures that improve the accuracy and energy efficiency of the pipeline architecture. The pipeline ADC architecture is well suited for implementing ADCs over wide ranges of speed and resolution. But, high accuracy (≥12-bits) and high energy efficiency (<100fJ/conv.-step) is difficult to achieve. This works presents two high-resolution pipeline ADC architectures, implemented as a 14-bit 23MS/s ADC (first prototype) and a 12-bit 50MS/s ADC (second prototype). The key advancement are:

- The creation of a low-OSR, high-resolution, calibration-free, low-power ADC architecture based on resetting ΣΔ modulators. In this work, the ΣΔ ADC architecture is combined with the pipeline ADC architecture, to create a hybrid architecture with enhanced accuracy and energy-efficiency.
- The development of modeling techniques that predict the optimum design architecture for pipeline ADCs, based on resetting ΣΔ modulators.
- The creation of a high-resolution, low-power pipeline ADC architecture based on the SAR (Successive Approximation) architecture. In this ADC, the SAR architecture is combined for the first time with the pipeline architecture to achieve high energy efficiency with high-resolution.

1.7 Thesis Outline

The motivation for investigating design techniques and architectures to enhance the speed, resolution and energy efficiency of ADCs in scaled digital CMOS processes is discussed in this chapter. Some of the major ADC architectures, such as pipeline, ΣΔ and SAR, are discussed in chapter 2. Recent ADC publications, with respect to different ADC architectures and their performances, are also reviewed in chapter 2. Chapter 3 presents the design, implementation and measurement results of the first prototype. This first prototype is a 14-bit 23MS/s ADC based on the resetting ΣΔ modulator. Chapter 4 presents the design and implementation of a 12-bit 50MS/s ADC (second prototype). This second prototype is based on a new hybrid pipeline-SAR architecture. Conclusions and suggestions for future work are given in Chapter 5.

CHAPTER 2

REVIEW OF ADC ARCHITECTURES

2.1 Introduction

The flash ADC architecture, discussed in section 1.4, is conceptually the simplest ADC architecture. This architecture is well suited for high-speed applications as all comparators see the input signal and give decisions simultaneously. The number of comparators required to implement an N-bit flash ADC is 2^N-1 which is the main drawback of the flash architecture. As N increases, the number of comparators required increases exponentially. Moreover, as ADC resolution becomes finer for larger N, the comparator offset requirements becomes smaller. Thus the number and accuracy of the comparators required to implement an N-bit flash ADC increases exponentially as N increases. This is why the flash ADC architecture has been limited to resolutions of ≤8-bits.

Other ADC architectures exist that do away with the large number of comparators requirement of the flash architecture. All architectures have their own advantages and disadvantages, making them suitable for specific ranges of resolutions and speeds. Some of the other popular ADC architectures are the pipeline, successive-approximation (SAR) and oversampling (or ΣΔ) architectures. Fig 2.1 shows the approximate suitable range of

resolution and speed for different architectures. Sections 2.2, 2.3 and 2.4 discuss the pipeline, ΣΔ and SAR ADC architectures respectively. Section 2.5 reviews some recent ADC publications.

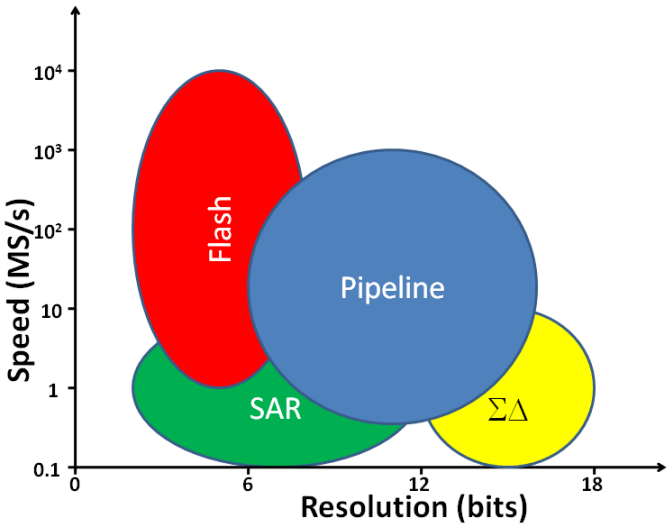

Fig. 2.1: Speed-resolution range of ADC architectures

2.2 The Pipeline Architecture

A pipeline ADC quantizes input voltage in a number of stages. Fig. 2.2 shows the block diagram of a conventional 14-bit pipeline ADC architecture, with a front-end sample-and-hold (S/H), followed by 5 stages, each with 2.5-bit (2-bit effective + 0.5-bit redundant) resolution, and finally, a 4-bit flash sub-ADC. Each stage of a pipeline ADC has a resolution much lower than the overall resolution of the whole ADC. Thus the number of comparators required to implement an N-bit ADC is much less than 2^N-1. In this example of 14-bit pipeline ADC, only 45 comparators are required (2.5-bit stages and 4-bit flash stage require 6 and 15 comparators respectively). The input V_{in} is

quantized to 2.5-bits by the first stage. After this, the amplified quantization error of the first stage called the residue V_{res}, passes to the second stage. While the second stage is quantizing the residue V_{res} of the first stage, the first stage processes the next sample. This ADC architecture has a high throughput, as the input is quantized in a pipeline fashion. But it suffers from a large latency, which is proportional to the number of stages in the pipeline.

Fig. 2.2 also shows the block diagram of a single pipeline stage, also known as a Multiplying-DAC (MDAC). Each pipeline stage contains a low-resolution sub-ADC, which quantizes the input. The sub-ADC output is subtracted from the input to obtain the quantization error. The quantization error is gained up to form the residue V_{res}. Because of this gain each stage has large input signal amplitude, therefore the resolution requirement of sub-ADCs is relaxed.

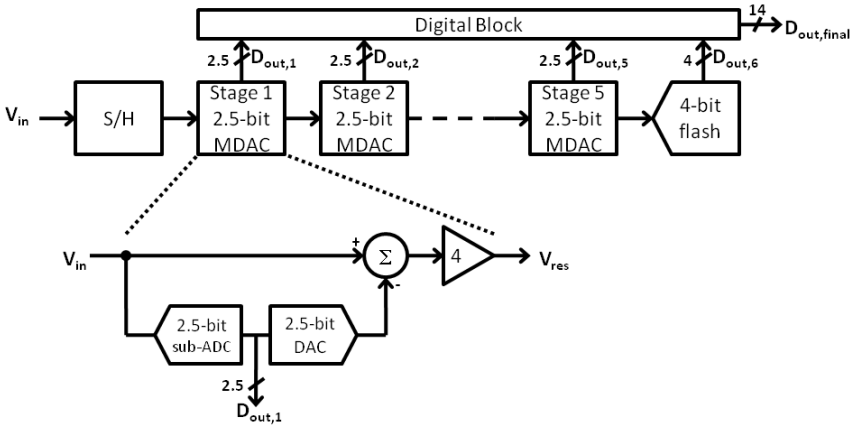

Fig. 2.2: 14-bit pipeline ADC block diagram

Fig. 2.3 shows the single-ended version circuit implementation of a 2.5-bit MDAC [15]. The input V_{in} is sampled onto capacitors C_1-C_4. Then the charge stored in capacitors C_1-C_3 is transferred to capacitor C_4, to gain up the input signal by a factor of 4. The bottom plates of capacitors C_1-C_3 are connected to the sub-ADC output simultaneously to implement the DAC subtraction.

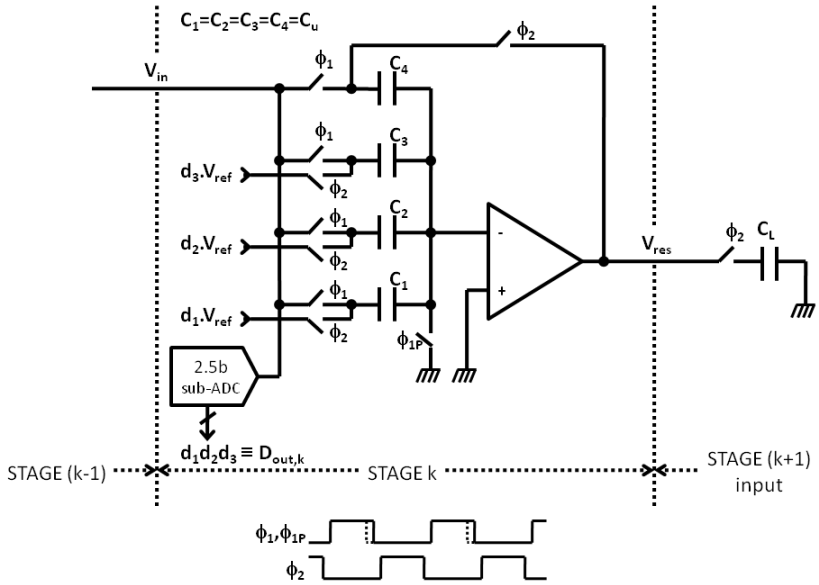

Fig. 2.3: 2.5-bit MDAC stage circuit implementation

Fig. 2.4 shows the ideal V_{out} versus V_{in} plot of a pipeline stage, also popularly known as the residue plot. This plot is governed by the following equation:

$$V_{res} = 4V_{in} - D_{out}V_{ref} \tag{2.1}$$

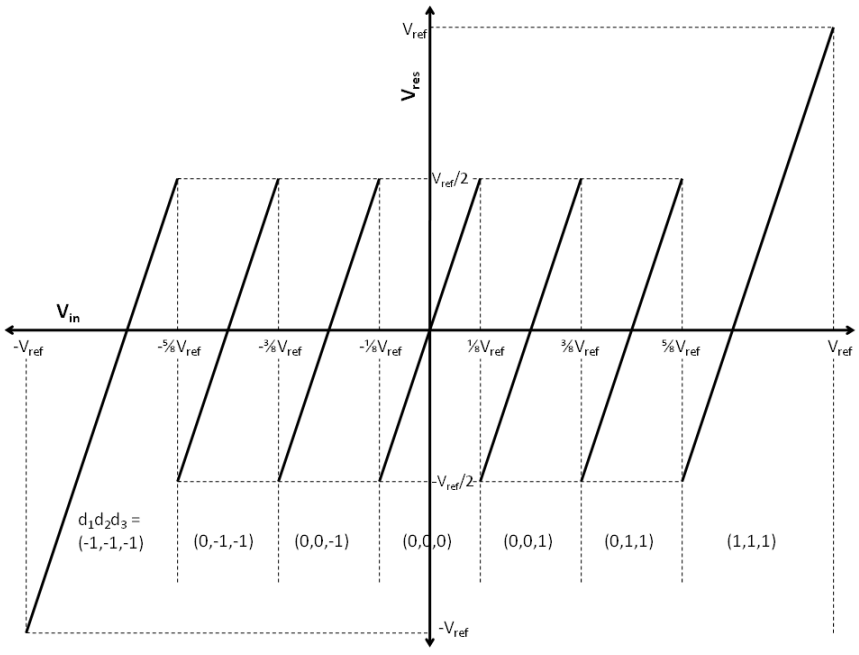

Fig. 2.4: Ideal residue plot for 2.5-bit MDAC stage

A. Advantages of the Pipeline Architecture

The pipeline architecture is well suited to implementing ADCs with moderate to high resolutions (8–14-bit) and moderate to high speeds (10-200MHz). The high throughput nature of the architecture makes it a good candidate for implementing high-speed ADCs. The presence of redundancy and gain relaxes the comparator offset requirements.

B. Disadvantages of the Pipeline Architecture

Although each pipeline stage has a very low resolution as compared to the overall resolution of the ADC, a pipeline stage needs to be as accurate as the sum of its own resolution and the resolution of the stages following it. Because of this the pipeline ADC suffers from the following disadvantages:

- High gain op-amps are required in the initial stages of the pipeline to reduce errors due to finite op-amp gain. This is difficult to achieve in low-voltage nanometer CMOS processes.
- Large op-amp bandwidth is also required to reduce errors due to finite settling. Thus op-amps dissipate a considerable amount of power in a pipeline ADC.
- Good capacitor matching is also required in the initial stages of the pipeline. Capacitor matching in modern CMOS processes is limited to about 11-bits. This makes the implementation of pipeline ADCs with resolutions >12-bits difficult without the use of calibration for capacitor mismatch.
- A front-end S/H is usually required in a high-resolution, high-speed pipeline ADC to reduce aperture errors between the signal sampled by the input sampling

capacitors (C_1-C_4 in Fig. 2.3) and the sub-ADC. The front-end S/H dissipates considerable power and also eats into the noise budget of the whole ADC.

2.3 ΣΔ Architecture

The oversampling or ΣΔ architecture [16] enhances ADC resolution by trading speed for accuracy. This architecture is especially attractive as process scaling enables faster transistors and thus higher speed converters. This architecture is well suited to implementing high-resolution, low-speed ADCs.

Fig. 2.5 shows the circuit diagram of a first order ΣΔ modulator. Capacitors C_1-C_2 and the op-amp form an integrator. The input signal is sampled onto capacitor C_1 and later integrated onto feedback capacitor C_2; this integration is the 'Σ' operation. The sub-ADC, connected to the output of the op-amp, quantizes the integrator output to D_i. This sub-ADC output is later subtracted at the input; this is the 'Δ' operation. For static input V_{in} and 0 initial condition, it can be shown that after N clock cycles, the input can be estimated as:

$$V_{in} \approx V_{ref} \sum_{i=1}^{N} D_i \Big/ N \tag{2.2}$$

Thus, as N increases, the estimate of V_{in} given by D_i (i = 1 to N) gets better.

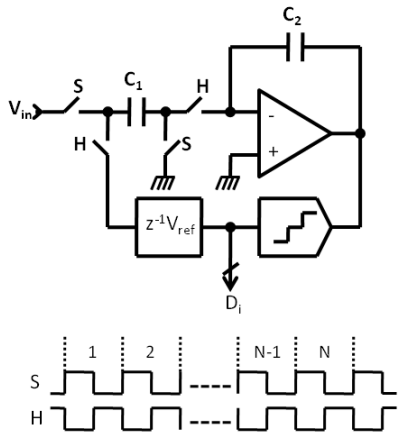

Fig. 2.5: 1st order ΣΔ modulator

Fig. 2.6a shows a block diagram, with a plot of the 'z-transform' transfer function, of a 1st order ΣΔ ADC. The sub-ADC is modeled as an addition of quantization noise E(z). The output of the ADC, in the z-domain, is given as:

$$D(z) = V_{in}(z) + (1 - z^{-1})E(z) \tag{2.3}$$

The sub-ADC quantization noise E(z) sees a high pass transfer function ($1-z^{-1}$) at the output of the ADC. This high pass transfer function is also known as the noise transfer function (NTF) and is shown in Fig. 2.6b. In the frequency domain, the sub-ADC quantization noise is pushed to higher frequencies. This is called 'noise-shaping', which is a powerful tool for enhancing the resolution of an ADC. If the input V_{in} is a low-frequency signal, the high-frequency quantization noise at the output can be filtered out with a low-pass digital filter, such as an averaging or $Sinc^1$ filter. Thus ADC speed or bandwidth is traded for higher accuracy or lower quantization noise.

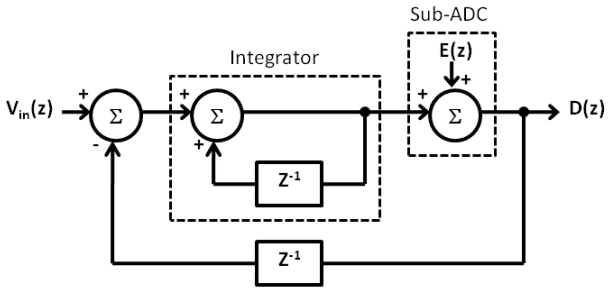

Fig. 2.6a: 1st order ΣΔ ADC block diagram

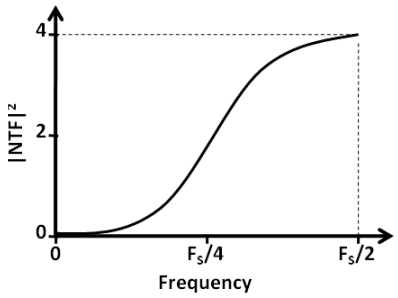

Fig. 2.6b: NTF characteristics

Higher order ΣΔ ADC architectures employ larger number of integrators to obtain a higher order high-pass transfer function for the quantization noise. Generally an N^{th} order ΣΔ ADC will have an NTF of $(1-z^{-1})^N$. Thus a higher order ΣΔ ADC can push more of its in-band (low-frequency) quantization noise to high frequencies.

A. Advantages of the ΣΔ Architecture

The main advantages of ΣΔ architecture are:

- Errors due to circuit non-idealities, e.g. feedback DAC mismatches [17] and quantizer errors, can be pushed to high frequencies and filtered out by using a digital filter at the output of the ADC.
- CMOS scaling enables fast transistors but transistor gain and linearity suffers with scaling. In this scenario the trade-off between speed and accuracy presented by the ΣΔ architecture is attractive.
- The ΣΔ architecture can be modified to implement band-pass ΣΔ ADCs which can be useful for RF receiver applications to filter and select a particular frequency channel [18].

- A continuous-time (CT) implementation of ΣΔ ADCs [19] is possible and is becoming popular because of the anti-alias filtering at the input of the ADC and the lower power consumption.

B. Disadvantages of the ΣΔ Architecture

The ΣΔ architecture's disadvantages mainly stem from its elaborate and complicated circuit implementation. They are as follows:

- ΣΔ ADCs require a high-speed digital filter at the output of the ADC to filter out high-frequency noise. These digital filters can dissipate a considerable amount of power.
- More aggressive noise-shaping requires higher order ΣΔ modulators. The number of integrators to implement N^{th} order ΣΔ ADC is N, thus analog complexity and power consumption increases as N increases.
- Higher order ΣΔ modulators suffer from stability issues. ADCs employing such modulators need to be designed and simulated carefully to avoid instability.

Despite these disadvantages the ΣΔ architecture is still the most attractive choice for implementing high-resolution ADCs.

2.4 SAR Architecture

The successive approximation or SAR ADC architecture uses a binary search algorithm to quantize the input. A single comparator is used in a serial fashion to resolve the input. Because of its serial nature, this architecture is suited for low-to-moderate speeds. This architecture has low analog complexity and low power consumption because it uses only one comparator. Fig. 2.7 shows the circuit diagram of a 6-bit SAR ADC [20]. In the 'sample' phase, V_{in} is sampled onto the bottom plate of the capacitor array, also

called capacitor DAC or CDAC, with the top plate grounded. In the 'search' phase, the bottom plate is grounded with the top plate floating. This produces a potential equal to $-V_{in}$ at the top plate. Now the 'search' proceeds by switching the bottom plate of each binary weighted capacitor to either $+V_{ref}$ or $-V_{ref}$, such that the top plate voltage eventually goes to zero.

For example, depending on the sign of top plate potential at the start of the 'search' phase i.e. $-V_{in}$, the MSB (Most Significant Bit) i.e. d_1 is assigned +1 (-1) if its negative (positive). After this the bottom plate of the most-significant capacitor is connected to $+V_{ref}$ ($-V_{ref}$), making the top plate voltage shift up (down) by $V_{ref}/2$. Subsequently, the other bits d_i (i = 2 to 6) are decided and their corresponding capacitor bottom plate switched. Thus the top plate potential progressively approaches zero. The conversion ends when the LSB i.e. d_6 is decided, so there are no capacitors corresponding to d_6.

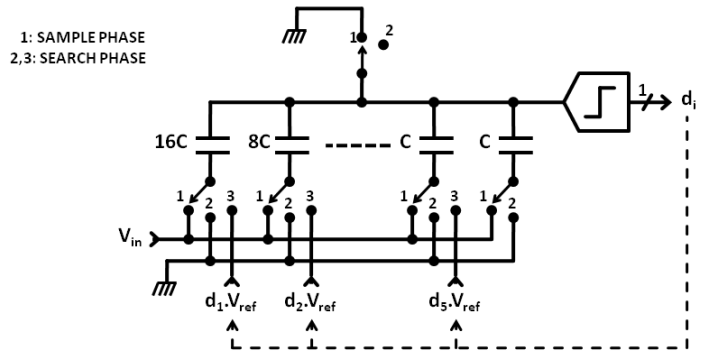

Fig. 2.7: A 6-bit SAR ADC

A. Advantages of the SAR Architecture

All the advantages of the SAR architecture come from its architectural simplicity. They are as follows:

- The SAR ADC as shown in Fig. 2.7 uses the same capacitor array for sampling the input signal and for implementing the DAC to estimate the input. Separate S/H and DAC circuits are not required in this particular implementation of a SAR ADC.
- The architecture uses only one comparator.
- No op-amps are required for implementation. Thus the architecture has minimum analog complexity.
- Comparator offset can be modeled as an input referred offset for the whole ADC. Thus comparator offsets don't cause non-linearity as in the case of other ADC architectures.
- It has very low power consumption because of the absence of op-amps and the use of only one comparator.
- This architecture shows excellent scalability with process because of the lack of analog building blocks.

B. Disadvantages of the SAR Architecture

The SAR ADC architecture suffers from a few but serious disadvantages that have prevented it from being used in high-speed, high-resolution ADCs. They are as follows:

- The serial nature of SAR architecture limits its speed.
- The number of unit capacitors required for an N-bit SAR ADC is about 2^{N-1} (for differential implementation it is 2^N). This becomes prohibitively large for N>10. Capacitors can be connected in series or a 2C/C capacitor array can be used to

reduce the number of unit capacitors required, but their accuracy gets compromised because of the presence of parasitic capacitors.

- Comparator noise causes performance degradation of the ADC because of the lack of gain in the ADC architecture. One can put a preamplifier before the comparator to reduce this noise, but at the expense of burning more power in the preamplifier.

Because of these reasons, low-power SAR ADCs have been limited to resolutions of ≤ 10-bits.

2.5 Recent ADC Publications

Pipeline ADCs published in the last 5 years have resolutions ranging from 8-bits up to 16-bits and speeds ranging from 8MS/s up to 500MS/s. Digital calibration has been used in many of these ADCs to compensate for capacitor mismatches [21-24] and op-amp gain and linearity errors [10, 22, 23, 25]. Switched op-amp technique [26-28] of switching off the op-amp during their passive phase to save power has been reported. Another useful technique involves reusing the same op-amp for different stages of the same pipeline ADC [29, 30] to save power consumption and chip area. In this technique, a stage having the active phase coinciding with the passive phase of another stage and vice-versa, share the same op-amp. Use of a comparator based op-amp [31-33], to replace power hungry analog op-amps, has also been proposed. Time interleaved pipeline ADCs have been able to achieve speeds up to 1GS/s [34, 35].

Oversampling (ΣΔ) ADCs published in the past 5 years have SNDRs ranging from 51dB up to 97dB and signal bandwidths ranging from 20kHz up to 44MHz. High speed transistors, enabled by CMOS scaling, have enabled ΣΔ ADCs with large signal

bandwidths [36-38]. Continuous time (CT) implementation of ΣΔ ADCs [39-41] is now an attractive choice. This is because of the power and speed advantages of CT implementation and the inherent anti-alias filter present at the input. On the other hand, CT ΣΔ ADCs require RC time constant trimming and are sensitive to clock jitter [39-41]. Band-pass and quadrature ΣΔ ADCs [42-44] are also popular choices for wireless applications. Despite the complicated circuit implementation, high resolution ADCs are still preferably implemented using ΣΔ architectures.

Recently published ADCs, with SAR architectures, have resolutions in the range of 9 to 12-bits and speeds in the range of 0.1 to 50 MS/s. The ADC with the lowest ever FOM, published so far, is a SAR ADC [45]. SAR ADCs with asynchronous comparators [46, 47] have better speeds as compared to synchronous comparators. To overcome the low-speed disadvantage of the SAR architecture, time-interleaved SAR architectures [48-50] have been proposed. These ADCs have speeds in the GHz range, but their resolutions have been limited to <6-bits.

Table 2.1 summarizes the performance of all recently published ADCs discussed above.

Resolution (bits)	Effective Speed (MHz)	Technology (µm)	ENOB	Bandwidth (MHz)	Power (mW)	FOM (pJ/conv.-step)	Reference
Pipeline ADCs							
16	125	0.18	12.50	62.5	385	0.532	[21]
14	100	0.09	11.14	50	130	0.576	[22]
10	500	0.09	8.51	250	55	0.302	[23]
10	100	0.065	9.51	50	4.5	0.062	[24]
10	50	0.18	9.00	25	9.9	0.337	[25]
10	50	0.13	9.21	25	15	0.507	[26]
10	50	0.18	8.84	25	35	1.528	[27]
8	200	0.18	7.56	100	30	0.795	[28]
10	50	0.18	8.78	25	18	0.819	[29]
14	100	0.18	11.73	50	230	0.677	[30]
12	50	0.09	10.01	25	4.5	0.087	[31]
8	200	0.18	6.40	100	8.5	0.503	[32]
10	8	0.18	8.68	4	2.5	0.762	[33]
11	1000	0.13	8.35	500	250	0.766	[34]
11	800	0.09	8.68	400	350	1.067	[35]
ΣΔ ADCs							
-	20	0.18	11.83	10	240	3.296	[36]
-	20	0.13	10.17	10	20.5	0.890	[37]
-	40	0.09	11.34	20	27.9	0.269	[38]
-	40	0.13	12.00	20	38	0.232	[39]
-	40	0.13	12.68	20	87	0.293	[40]
-	20	0.18	13.33	10	100	0.486	[41]
-	-	0.09	11.17	20	56	-	[42]

-	-	0.18	11.34	1	4.7	-	[43]
-	-	0.18	12.33	44	375	-	[44]
SAR ADCs							
10	1	0.065	8.74	0.5	0.0019	0.004	[45]
9	50	0.09	7.40	10	0.29	0.086	[46]
9	40	0.09	8.56	20	0.82	0.054	[47]
7	2500	0.045	5.36	1100	50	0.553	[48]
6	1250	0.13	5.75	625	32	0.476	[49]
8	600	0.13	6.85	300	30	0.433	[50]

Table 2.1: Performance summary of recent ADC publications

Recent ADC publications show a trend towards implementation in digital CMOS processes with smaller feature sizes and better energy efficiencies. As discussed in section 1.2, such processes lack good analog performance and these ADCs tend to have lower resolutions. Digital calibration and other novel techniques are utilized to achieve higher resolutions.

CHAPTER 3

HYBRID ΣΔ-PIPELINE ARCHITECTURE

3.1 Introduction

Many applications including wireline and wireless communications, imaging and video, demand high-resolution (>12-bit), low-distortion analog-to-digital conversion with a signal bandwidth of several MHz. System-on-chip (SoC) integration dictates the use of modern nanometer CMOS processes with low-supply voltages. Achieving high-resolution and moderate-speed with pipeline ADCs, in such scenarios, often requires calibration to enhance component matching [10, 21-23]. Furthermore a front-end sample-and-hold (S/H) is usually necessary to remove aperture error and reduce distortion [15, 51, 52]. Pipeline ADCs, without a front-end S/H, usually requires an accurate sampling path matching between the first stage MDAC and its sub-ADC input [53]. On the other hand, continuous-time (CT) ΣΔ ADCs suffer from the requirement of RC time-constant calibration and are sensitive to clock jitter [39-41]. Switched-capacitor (SC) ΣΔ ADCs employ low over-sampling ratio (OSR) and multi-bit feedback DACs to achieve high-bandwidth, but calibration and/or dynamic element matching of the feedback DACs is required to maximize performance [36]. ΣΔ ADCs also require a digital decimation filter

of considerable speed [39]. Such additions increase power consumption, complexity and chip area.

To enhance the accuracy of pipeline ADC architecture, a hybrid architecture based on the pipeline and the resetting ΣΔ architectures is proposed in this chapter. A low-OSR, high-resolution, calibration-free, low-power ADC architecture based on the pipeline of a resetting ΣΔ modulator and a Nyquist ADC is presented. For the first time a resetting ΣΔ architecture is adapted and utilized for a high-speed, high-bandwidth application. The architecture is found to improve the accuracy of the pipeline architecture without requiring any calibration.

This chapter presents the design, analysis, implementation and prototype measurements of a 14-bit 23MS/s ADC [54], which employs a second-order resetting ΣΔ modulator pipelined with a 10-bit cyclic ADC. This ADC uses a resetting ΣΔ modulator with a low OSR of 5 to achieve higher bandwidth, and to eliminate the need for a front-end S/H. Simulations and the prototype measurements show that the architecture is tolerant of circuit non-idealities such as capacitor mismatch, finite op-amp gain and finite op-amp settling. Larger tolerance of settling errors reduces bandwidth requirement op-amps and saves power. Although the architecture is calibration-free and has a low OSR, the prototype ADC achieves 11.7-bit ENOB, 87dB SFDR and no missing codes at 14-bit resolution. The resetting architecture also eliminates the need for power hungry digital decimators and enables the ADC to sample as a Nyquist converter. The ADC achieves a large Nyquist bandwidth of 11.5MHz with a power consumption of 48mW. The power consumption and die area of 0.5mm^2 compares well with other high-resolution high-speed ADCs.

Section 3.2 introduces the concept of a resetting ΣΔ modulator. In section 3.3 we describe the prototype ADC architecture. Section 3.4 analyzes the resetting ΣΔ ADC architecture in detail and explains the advantages of this architecture over the conventional pipeline ADC architecture. Sections 3.5 and 3.6 present circuit details and measured results of the prototype ADC. Section 3.7 proposes an optimum design architecture for designing ADCs based on resetting ΣΔ modulator. Finally, sections 3.8 present the conclusion.

3.2 Resetting ΣΔ Modulator

A resetting ΣΔ converter, also known as single-shot [55] or incremental [56] ΣΔ converter, is essentially a ΣΔ ADC in which the modulator is reset after a pre-determined number of clock cycles. Extended counting converters [57, 58], also a type of resetting ADC ΣΔ converter, employ a first order resetting ΣΔ conversion followed by a Nyquist conversion to quantize the input. Resetting removes the memory of the modulator and enables the converter to sample as a Nyquist converter. In this way a resetting ΣΔ ADC incorporates the advantages of a ΣΔ modulator in a Nyquist-sampling ADC. Fig. 3.1 shows an example of a first order resetting ΣΔ ADC which is reset after 'N' clock cycles.

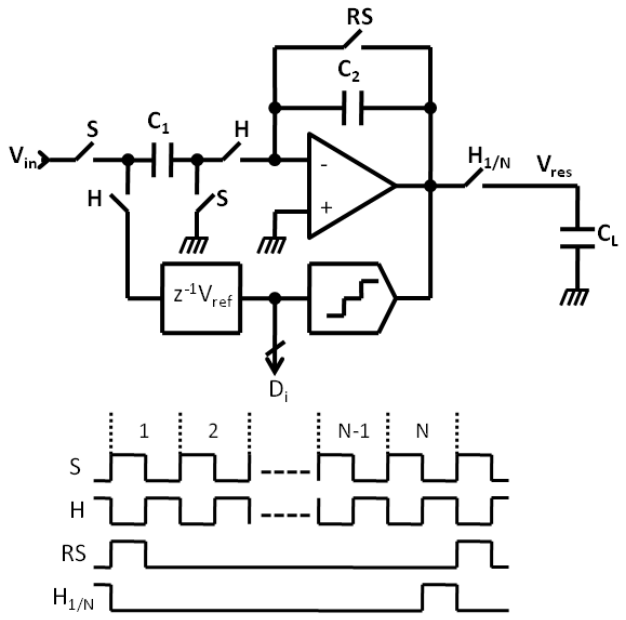

Fig 3.1: 1st order resetting ΣΔ modulator with OSR=N

It can be shown that the estimate of input V_{in} improves as N increases:

$$V_{in} \cong V_{ref} \sum_{i=1}^{N} D_i / N \tag{3.1}$$

Resetting ΣΔ modulator architectures with high OSR have been used for low-frequency or DC input signal applications [55, 56, 59]. Extended counting ADCs [57, 58] generally reuse hardware, which leads to low bandwidths in the KHz range.

3.3 ADC Architecture

The proposed ADC architecture (Fig. 3.2) is a pipeline of a second-order resetting ΣΔ modulator (stage 1) and a 10-bit cyclic ADC (stage 2). This architecture has a low OSR and is different from the feed-forward architectures used in [56, 59] and first order architectures in [57, 58] to enable much higher speed operation. A residue signal V_{res} is passed from the ΣΔ modulator to the cyclic ADC. A 10-bit Nyquist ADC is chosen for

back-end residual error quantization (stage 2), since the maximum achievable resolution in traditional uncalibrated Nyquist ADC architectures (pipeline, SAR, etc.), considering capacitor matching (~11-bits) [60], is about 10-bits [61]. A cyclic ADC architecture is adopted for the second stage for simplicity. A minimum front-end stage resolution of 4-bits and gain of 16 is required to achieve a total ADC resolution of 14-bits. A second-order resetting integrator architecture is chosen for the first stage. With an OSR of 5, this second-order integrator gives a gain of 15, which is less than 16, so the ADC resolution suffers slightly.

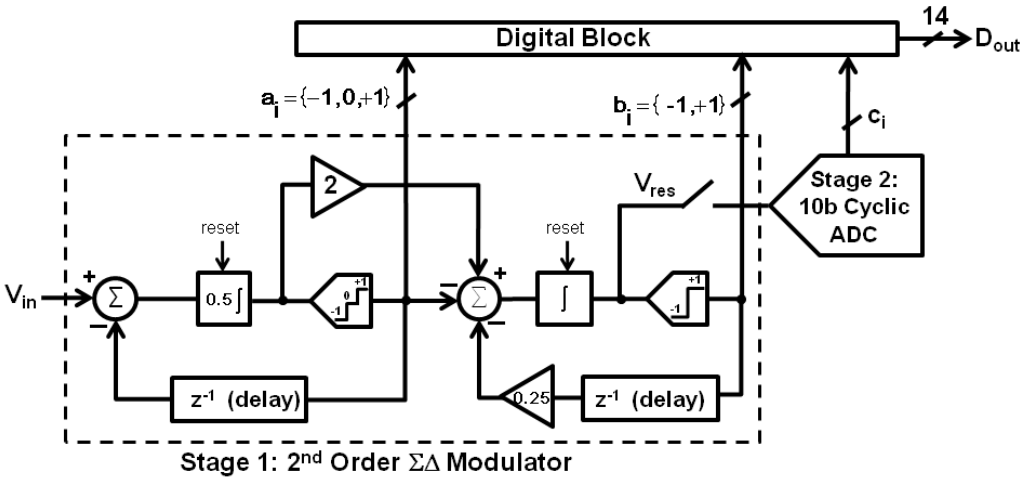

Fig 3.2: ADC architecture

The front-end ΣΔ modulator samples and modulates the input (V_{in}) at 115MHz, or 5 times the effective conversion-rate. After every five samples, the residue (V_{res}) at the output of the ΣΔ front-end is passed to the second-stage cyclic ADC and the ΣΔ modulator is reset. The cyclic ADC then quantizes the residue while the ΣΔ front-end processes the next 5 samples. The cyclic ADC also requires 5 clock cycles to resolve 10-bits, and in this way, as both stages have a matched latency of 5 clock cycles at 115MHz,

perfect two-step pipelining is achieved. The digital outputs from the ΣΔ modulator and from the cyclic ADC are combined by the Digital Block to give overall ADC output, D_{out}. This two-step pipelining leads to a latency of only 1 conversion-rate (23MS/s) clock period.

The second-order ΣΔ front-end is itself a 1-1 MASH [62] cascade of two first-order modulators. The feedback and feed-forward coefficients are chosen to maximize signal gain while avoiding clipping, and also to ensure large unit-capacitors for more practical circuit implementation. The output of the first integrator is 1.5-bit quantized (to a_i) by two comparators with thresholds set at $\pm V_{ref}/4$. An inherently-linear 1.5-bit DAC, driven by a_i, subtracts the input of the first integrator. The output of the second integrator is 1-bit quantized (to b_i) by a single comparator with a differential threshold set at 0. a_i and b_i together drive the input of the multi-bit DAC that feeds the second integrator. Assuming the input signal, V_{in}, is constant, the output residue V_{res} of the second integrator after 5 clocks is:

$$V_{res} = 15V_{in} - V_{ref}\left[\sum_{i=1}^{5}\sum_{j=1}^{i} a_j + \frac{1}{4}\sum_{i=1}^{4} b_i\right] \qquad (3.2)$$

V_{res} is effectively a gained-up version of input signal, less the digital estimation formed by a_i and b_i. From (3.2) we can see that the first stage has an effective gain of 15 of the input signal V_{in}. The double summation indicates second-order integration. The 10-bit cyclic ADC quantizes V_{res} giving a total ADC resolution of 13.9-bits. The total resolution is a little less than 14-bits because of the gain of 15 (instead of 16) from the first stage (equation (3.2)).

For a time-varying input, V_{in} in equation (3.2) is replaced by a linearly-weighted average, which causes low-pass-filtering with attenuation of up to 2.77dB at the 11.5MHz Nyquist frequency. The effect of this filtering is discussed in more detail in section 3.5-C. This filtering can be used to help attenuate signals in some frequency ranges.

3.4 Architecture Advantages

To understand the advantages of a resetting ΣΔ modulator, we compare a first-order resetting ΣΔ modulator and a conventional Multiplying-DAC (MDAC) stage of a pipeline ADC [15]. A first-order modulator is analyzed instead of a second order modulator for simplicity. Although a second-order modulator, such as the one used in our prototype ADC, differs in many ways from a first-order system, analysis of a first-order modulator gives us an intuitive understanding of the basic advantages of such systems, without dwelling too much on the complexity of a higher order system. Qualitative and quantitative comparisons between a first-order resetting modulator and an equivalent MDAC stage with respect to finite op-amp gain error, finite op-amp settling, capacitor mismatches, etc. are discussed in this section.

Fig. 3.1 shows an example of a first-order resetting ΣΔ modulator. As with a conventional ΣΔ stage, capacitors C_1, C_2 and the op-amp form an integrator. The input signal is sampled onto capacitor C_1 and later integrated onto feedback capacitor C_2. In each integrating step i (i = 1 to N) the output of op-amp is quantized to D_i by the sub-ADC. D_i (multiplied by V_{ref}) provides the DAC feedback of the ΣΔ modulator. In the resetting ΣΔ modulator a reset switch across feedback capacitor, C_2, controlled by clock

RS, periodically resets the integrator. In the example shown in Fig. 1, clock RS goes high once every N clock cycles, resetting the modulator, and thus this resetting ΣΔ modulator has an OSR of N.

Assuming that the input of the resetting ΣΔ modulator is constant, the output of the integrator at the end of N clock cycles is given by:

$$V_{res} = N\frac{C_1}{C_2}V_{in} - \frac{C_1}{C_2}V_{ref}\sum_{i=1}^{N-1}D_i \tag{3.3}$$

This final output V_{res} is passed onto a load capacitor C_L, through a switch controlled by clock $H_{1/N}$, just before the integrator is reset.

Fig. 3.3 shows a single-ended circuit implementation of a conventional 2.5-bit MDAC stage. Fig. 3.4 shows the ideal residue plot, output V_{res} versus input V_{in}, for this stage. This plot is governed by the following equation:

$$V_{res} = 4V_{in} - D_{out}V_{ref} \tag{3.4}$$

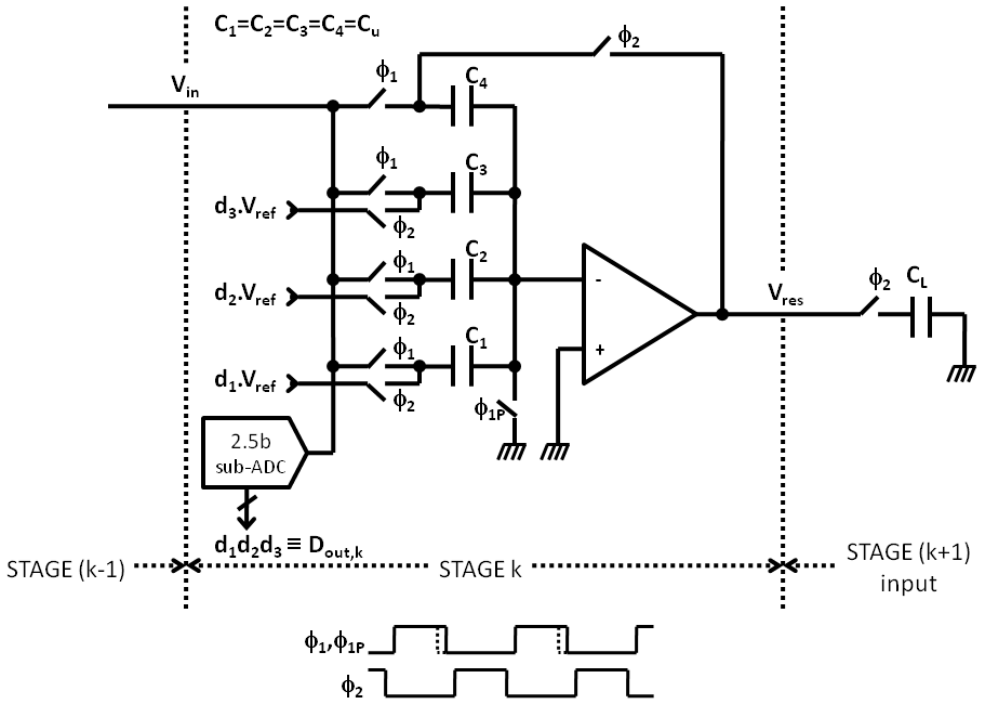

Fig 3.3: 2.5-bit MDAC stage of a conventional pipeline ADC

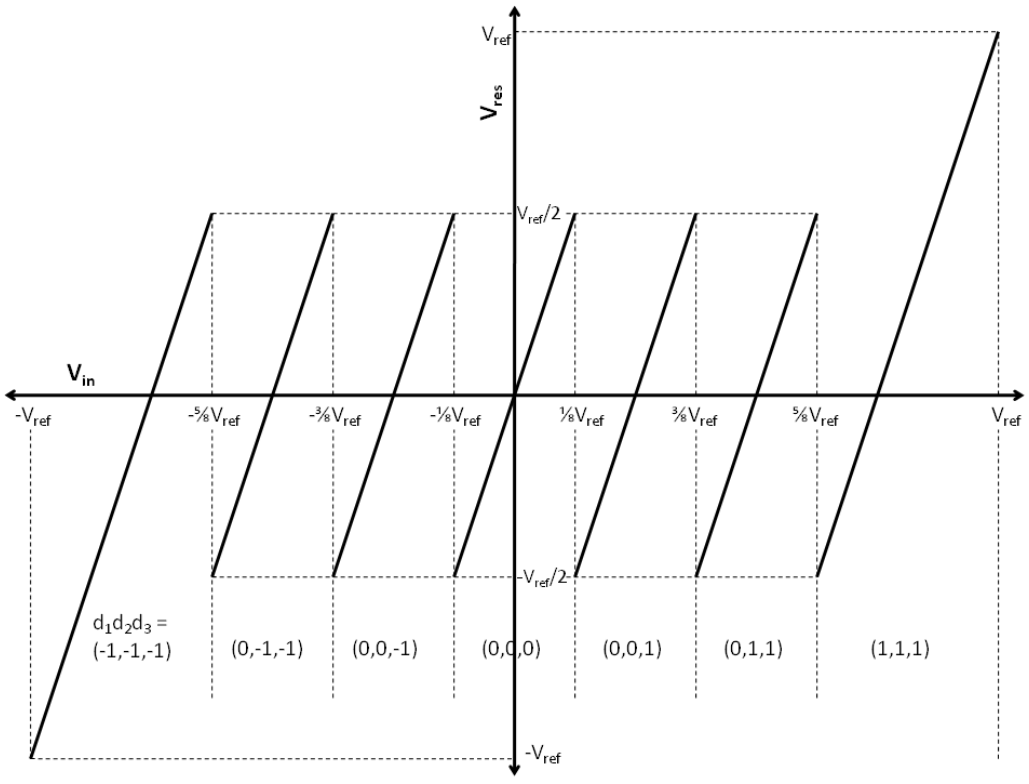

Fig 3.4: Ideal residue plot for 2.5-bit MDAC stage

Fig. 3.5 shows the residue plot equivalent (i.e. V_{res} versus V_{in} from equation (3.3)) for the resetting ΣΔ modulator. The stage gain is the coefficient of V_{in} in equations (3.3) and (3.4). Although the modulator has a different residue plot to that of the MDAC stage, a resetting ΣΔ modulator stage can replace the MDAC stage of a pipeline ADC if the gains are matched and output residue V_{res} lies within the input range of the next stage. For example, a 2.5-bit MDAC with a gain of 4 (Fig. 3), can be replaced with a first-order resetting ΣΔ modulator with $C_2 = 2C_1$ and N=8 (Fig. 3.1).

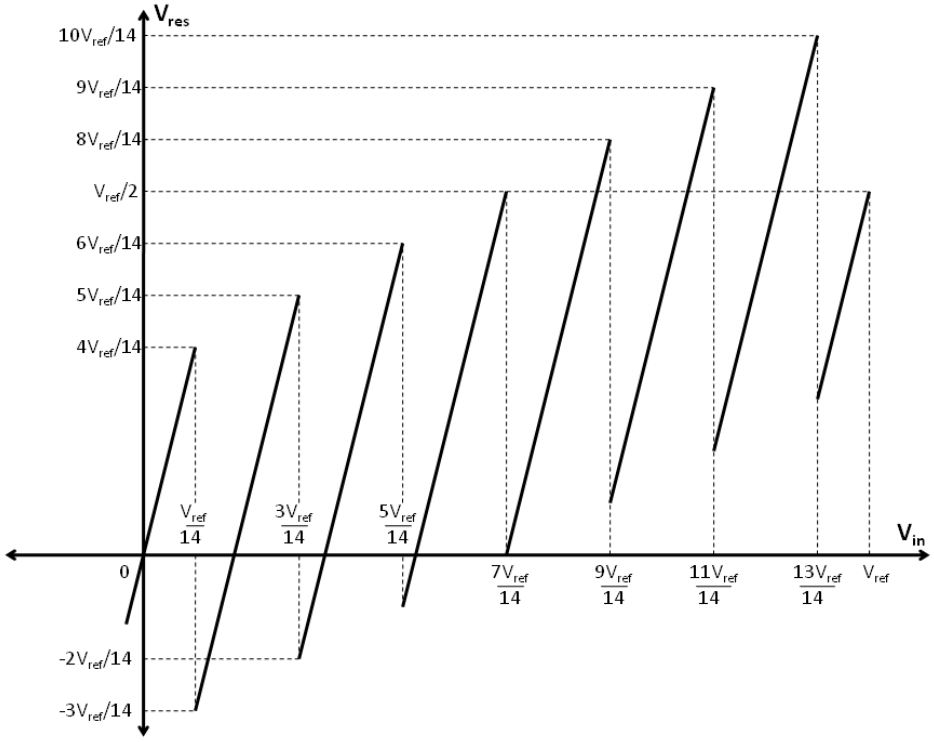

Fig. 3.5: Residue plot for a 1st order resetting ΣΔ modulator. For $C_2 = 2C_1$ and N=8 (only $V_{in}>0$ shown)

The use of an integrator instead of a conventional gain stage brings several advantages, including lower gain error, lower settling error, higher tolerance to capacitor mismatch and elimination of the front-end S/H. These advantages are especially beneficial for the initial pipeline stages where accuracy matters most to the overall ADC

performance. We now explore these advantages in detail, by comparing the use of a conventional MDAC (Fig. 3.3) and a resetting integrator (Fig. 3.1) as the first stage of a 14-bit pipeline ADC. We compare the use of a 2.5-bit MDAC with a gain of 4 with the use of a first-order resetting integrator with $C_2 = 2C_1$ and N=8. We look at circuit non-idealities in the first stage only. To simplify the analysis we assume that all stages after the first stage are ideal, so that the output of the first stage is connected to an ideal 12-bit ADC with a signal range of $-V_{ref}$ to $+V_{ref}$. This assumption is practical as the performance of the first stage of the pipeline ADC usually dominates, and we can gain insight into the contribution of each individual circuit non-ideality towards the performance of the whole ADC.

A. Lower Stage Gain Error

Stage gain-error is less with an integrator as compared to a conventional MDAC stage, because the feedback factor β is much higher for an integrator than for an MDAC stage with the same effective stage-gain. Stage gain-error, due to finite op-amp gain, causes non-linearity errors in a pipeline ADC. This is because finite op-amp gain causes errors in the ideal stage gain of equation (3.4). Fig. 3.6 shows the finite op-amp gain error mechanism. For an input signal V_{in} stored on sampling capacitor C_S and assuming all other capacitors have 0 initial condition, the output voltage across capacitor C_L in the steady state condition is given by:

$$V_{C_L} = V_{out} = \frac{C_S}{C_{FB}} V_{in}\left(1 - \frac{1}{A\beta}\right) \tag{3.5}$$

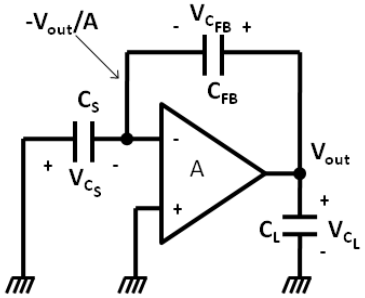

Fig. 3.6: Finite op-amp gain error

In this example with a stage-gain of 4, β is 2/3 for the integrator, compared to 1/4 for the MDAC.

With finite op-amp gain error the output residue equation (3.3) of the integrator becomes:

$$V_{res} = \left(4V_{in} - \frac{V_{ref}}{2} \sum_{i=1}^{N-1} D_i \right) \left(1 - \frac{1.5}{A} \right) \tag{3.6}$$

On the other hand, the MDAC stage residue with finite op-amp gain error is:

$$V_{res} = \left(4V_{in} - D_{out} V_{ref} \right) \left(1 - \frac{4}{A} \right) \tag{3.7}$$

Comparing equations (3.6) and (3.7) we see that the higher feedback factor β of the integrator stage gives the integrator a lower gain error for the same op-amp gain. MATLAB simulations of the 14-bit ADC with a finite op-amp gain of 80dB give a maximum DNL of 0.82LSB in the case of the conventional MDAC stage and a maximum DNL of only 0.27LSB for the integrator stage.

B. Lower Settling Error

Although an integrator stage runs at a higher clock rate, for a given op-amp bandwidth the settling error for an integrator stage is less than that of an equivalent MDAC stage. Finite op-amp bandwidth limits output settling of an op-amp. Finite

settling in an MDAC stage, results in errors of the output residue signal V_{res} that causes degradation of SNDR of the ADC. Considering finite settling in the MDAC stage residue equation (3.4), we get:

$$V_{res} = 4V_{in} - D_{out}V_{ref} + \varepsilon \tag{3.8}$$

and

$$\varepsilon = \Delta V e^{-\omega T_{sett}} \tag{3.9}$$

where ΔV is the voltage difference the op-amp has to settle to, T_{sett} is the time available for the op-amp to settle, $\omega = \beta g_m/C_{Ltot}$ is the op-amp closed loop 3dB bandwidth, C_{Ltot} the total output load capacitance and g_m the op-amp transconductance.

Although, in this example the integrator sampling clock is 8 times faster than the effective sampling rate to give an effective gain of 4, this does not mean that the required op-amp bandwidth is also 8 times larger. In fact, the settling error in the integrator is smaller because of three reasons. Firstly, the feedback factor β is larger for the integrator. Secondly, thanks to the averaging effect of oversampling (section 3.4-E), smaller capacitors can be used which leads to lower C_{Ltot}. Thirdly, during the first N-1 integration steps of the integrator (Fig. 3.1), the load capacitor C_L is not connected to the output of the op-amp, reducing C_{Ltot} for these steps. Because of these three reasons, the bandwidth requirement of the integrator op-amp is lower than that for the op-amp in a conventional MDAC, despite the fact that the integrator clock is 8 times faster than the MDAC clock.

An approximate comparison between a switched-capacitor oversampling and a Nyquist ADC shows that for same thermal noise budget we can decrease the size of the capacitors in the oversampling ADC by the OSR. On the other hand, the time available for the op-amp to settle in an oversampled converter decreases by the OSR. This decrease

in available time and capacitor size implies that for the same op-amp g_m the settling error ε (in equation (3.8) and (3.9)) is the same for both ADCs. Thus power dissipated by the op-amps in both ADCs is approximately the same.

SPICE simulations were done comparing the SNDR deterioration of the MDAC stage and the integrator stage due to finite op-amp settling. The op-amp transconductance, g_m, is the same in both cases, but the capacitor values for the integrator (C_1, C_2 and C_L in Fig. 3.1) are one-third that of the MDAC capacitor values (C_1-C_4 and C_L in Fig. 3.3) because for same thermal noise, the use of smaller capacitors thanks to oversampling, as described in section 3.4-E. Simulations show that SNDR degradation, due to settling error only, is 4.4dB lower in the integrator than in the MDAC.

C. Inherently Linear 1.5-bit DAC

Capacitive DACs used in MDAC stages suffer from non-linearity because of capacitor mismatch. With capacitor matching limited to ~11-bit in modern CMOS processes [60], DAC accuracy can be a limitation of MDAC stages, especially in high resolution (>12-bit) ADCs. On the other hand a resetting $\Sigma\Delta$ stage can always employ an inherently linear 1-bit or 1.5-bit DAC and still attain an overall resolution greater than 1-bit.

In the 2.5-bit MDAC (Fig. 3.3), the bottom plates of capacitors C_1–C_3 are connected to $+V_{ref}$, 0 or $-V_{ref}$ to implement a 2.5-bit feedback DAC. On the other hand, for the integrator stage (Fig. 3.1), the bottom plate of a single capacitor, C_1 is connected to $+V_{ref}$, 0 or $-V_{ref}$ to implement a 1.5-bit feedback DAC. The 1.5-bit sub-ADC of the integrator (Fig. 3.1) makes N (=8) decisions in N clock cycles to attain resolution greater than 1.5-bit, and in this way a 1.5-bit sub-ADC and 1.5-bit DAC are sufficient. The

linearity of the 2.5-bit feedback DAC, in the MDAC stage, depends on matching between four unit capacitors, C_1 to C_4. On the other hand, the 1.5-bit feedback DAC for the integrator, implemented with a single unit capacitor, is inherently linear[1]. This is a big advantage for the integrator architecture.

Extensive Monte-Carlo simulations with MATLAB models were performed to compare the sensitivity of the MDAC stage and of the integrator stage to capacitor mismatch. In these simulations, capacitors are assumed to be 9-bit accurate while everything else is assumed to be ideal. The stage residue is quantized by an ideal 12-bit ADC. A mean SNDR of 69dB and 80dB for the MDAC stage and equivalent integrator stage, respectively, is predicted. The standard deviation in both cases is 5dB.

Better performance of an integrator stage is not restricted to a 1-bit or 1.5-bit feedback DAC. The smaller number of unit capacitors in the feedback DAC of an integrator stage, as compared to an MDAC stage, in general always leads to better linearity. Nevertheless, the use of a 1-bit or a 1.5-bit feedback DAC has the added advantage of being inherently linear. It is important to note, that the use of an inherently linear 1.5-bit feedback DAC in a conventional 1.5-bit MDAC does not give the same advantages. This is because a pipeline ADC with a 1.5-bit first stage MDAC has poorer linearity as compared to a pipeline ADC with a multi-bit first stage MDAC [52]. In general, a resetting ΣΔ stage is more tolerant to capacitor mismatch as it can always employ an inherently linear 1-bit or 1.5-bit DAC and still attain a resolution greater than 1-bit.

[1] Capacitor mismatch between C_1 and C_2 only causes a gain error.

D. Elimination of Front-End S/H

The integrator architecture (Fig. 3.1) does not need a sample-and-hold (S/H), since the sub-ADC is connected to the output of the integrator which is a sampled-and-held signal. This is a big advantage as the input signal can be directly sampled onto the first stage sampling capacitors, without any RC-settling match requirements (explained in the next paragraph), thus completely eliminating the need for a front-end S/H stage. A high-resolution front-end S/H stage usually consumes a considerable amount of power and eats into the noise budget of the ADC. Not all ΣΔ modulator architectures, for example CIFF [63] architecture, enjoy this advantage.

If there is no front-end S/H, the sub-ADC of an MDAC stage (Fig. 3.3) is directly connected to the input signal. This requires a good RC-settling match between sampling of the input signal onto the capacitors C_1-C_4 and sampling of the input by the sub-ADC. Without a front-end S/H, any RC-settling mismatch between the input signal sampling onto the capacitors C_1-C_4 and sub-ADC sampling of the input, can cause an incorrect decision by the sub-ADC[2], and this decision error can be large for a high frequency input signal [53]. To avoid such errors a front-end S/H is often used, especially in the case of high-resolution converters.

E. Oversampling Advantage

Oversampling in a resetting integrator stage brings advantages compared to an MDAC stage. The resolution of any ADC can be enhanced by oversampling. For example, oversampling by 8 reduces the noise power by a factor of 8, assuming that noise is uniformly distributed in frequency, and that an ideal brick-wall digital filter filters

[2] Sub-ADC decision errors are tolerable to some extent because of comparator redundancy in an MDAC stage, but errors greater than sub-ADC step-size cannot be corrected.

noise between $F_S/16$ to $F_S/2$ (Fig. 3.7). However, oversampling results in a reduction of the usable input signal bandwidth, or alternatively a faster ADC is required to achieve the same signal bandwidth.

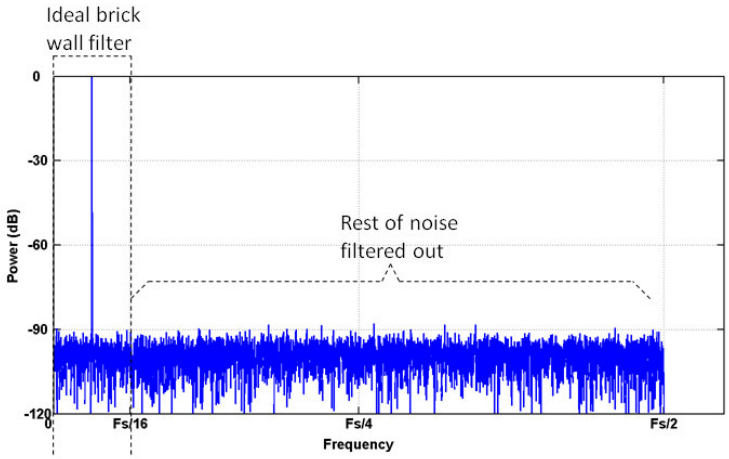

Fig. 3.7: The oversampling advantage

In our example, running the integrator clock 8 times faster is equivalent to oversampling the input by 8. This oversampling leads to an 8 times increase in the signal-to-noise power ratio of the ADC. Alternatively 8 times smaller capacitors can be used for the same ADC resolution. To account for non-ideal noise filtering, the non-decimated noise from following stages, larger input referred op-amp noise (because of larger β), etc., the capacitors are scaled down by a factor less than the OSR. Thus the integrator (Fig. 3.1) might use smaller capacitors 3 times smaller in size as compared to the MDAC (Fig. 3.3) capacitors. As a corollary to this advantage, the aperture error due to timing jitter is also reduced. For the same aperture error budget, the RMS jitter tolerance for an

8x sampling clock is enhanced by factor of √8, as compared to the RMS jitter tolerable in the 1x clock used for sampling in the MDAC stage[3].

F. Comparison Summary

Table 3.1 compares the use an MDAC and an integrator, as the first stage of a 14-bit pipeline ADC based on MATLAB and SPICE simulations. Stage 2 onwards of the pipeline is modeled as an ideal 12-bit ADC.

	Stage 1: Conventional 2.5-bit MDAC (Fig. 3.3)	**Stage 1: Integrator Stage with $C_2 = 2C_1$ and N=8 (Fig. 3.1)**
Finite Op-Amp Gain (=80dB) Error (DNL)	0.82LSB	0.27LSB
Finite Op-amp Settling Error	-	4.4dB higher SNDR*
Capacitor Matching (9-bit) Error (SNDR)	High (μ=69dB, σ=5dB)	Low (μ=80dB, σ=5dB)
Front-end S/H	Required	Not Required
Capacitor Sizes	Large	Small
Jitter Tolerance	Low	High (√8 larger)
Input Clock	Slow	Fast (x8 faster required)

*Same op-amp transconductance 'g_m' and one-third the load capacitance as the MDAC

Table 3.1: Comparison between a conventional MDAC stage and an integrator stage

[3] Noise due to sampling clock jitter, averaged over N samples, gives a √N advantage if jitter is random.

3.5 Circuit Details

For the prototype ADC architecture (Fig. 3.2), using a first-order modulator (Fig. 3.1) even with $C_2 = C_1$ for the first stage, would require an OSR of 16 which translates to 368MHz clock for a 23MS/s conversion speed. Such a high-speed clock for first stage would be impractical. Therefore, a second-order integrator architecture is chosen for the first stage, relaxing the OSR requirement to only 5.

Extensive MATLAB simulations were done to investigate the robustness of the prototype ADC architecture (Fig. 3.2). Simulations show that the architecture has a large tolerance to circuit non-idealities. 9-bit capacitor matching and a 75dB op-amp gain are sufficient to ensure no missing codes at 14-bit resolution. This tolerance comes from a combination of the two advantages that we discussed in section 3.4-A and C. A relaxed settling requirement helps reduce op-amp power consumption (section 3.4-B). This proposed modulator architecture was chosen over the CIFF modulator used in [56, 59] to eliminate the need for front-end S/H (section 3.4-D). Oversampling in the front-end reduces capacitor size requirements for the first stage and leads to a high clock jitter tolerance of up to 3ps (section 3.4-E). All of the above leads to a calibration-free, power-efficient and area-efficient design.

A. Front-End ΣΔ Modulator

Schematic of the ΣΔ front-end, which is a SC implementation of stage 1 of the ADC (architecture discussed in section 3.3), is shown in Fig. 3.8. A single-ended schematic is shown for clarity. The first and second integrators are implemented using op-amps A_1 and A_2 respectively. The outputs of first integrator (x_i) and second integrator

(y_i) are 1.5-bit and 1-bit quantized to a_i and b_i, respectively by the two sub-ADCs shown. The input sampling switches are bootstrapped for low distortion [64].

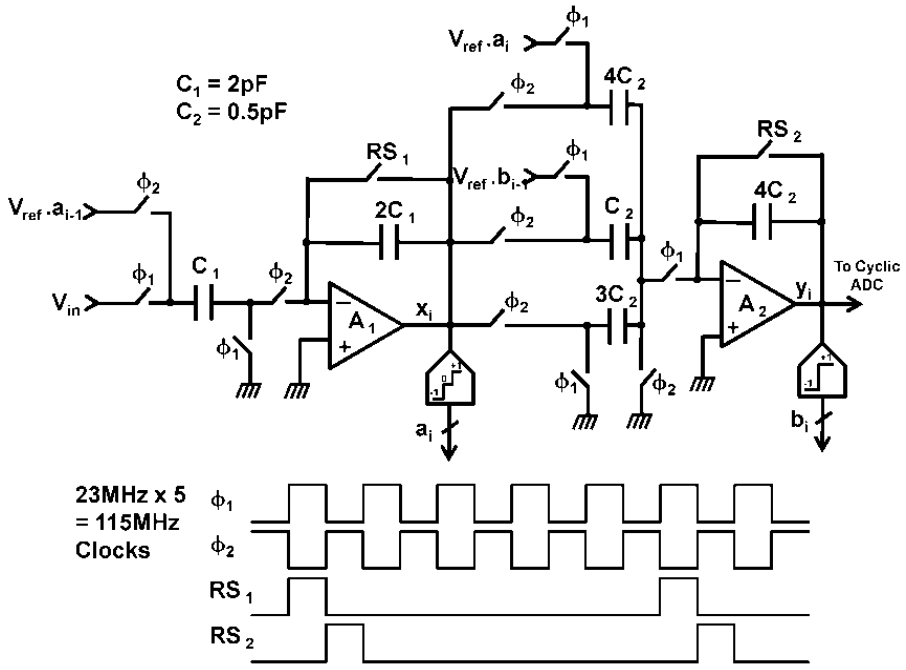

Fig. 3.8: SC implementation of 2nd order ΣΔ modulator

Both op-amps are implemented as folded, single-stage, triple-cascode, NMOS-input amplifiers, each with a gain of at least 75dB across all process-temperature variations. The maximum output swing is 1.4Vpp and 1.5Vpp at the outputs of first and second integrators (x_i and y_i), respectively. With a 2V supply and MOSFETs biased near sub-threshold with typical V_{DS} of 200mV, these op-amps support a total differential signal swing of 1.6Vpp so that the op-amps have sufficient signal swing margins for this ADC architecture. Simulations show that the on-chip bias network maintains a sufficient V_{DS} across process-temperature variations to keep the MOSFETs in saturation.

Digital estimation of the input, by the front-end modulator, has a total resolution of about 5-bit (over 5 clock cycles) which is larger than the 4-bit effective resolution required from the front-end stage. This redundancy relaxes the offset requirements of the

comparators forming the two sub-ADCs. The comparators are implemented as preamplifiers followed by latches to reduce input referred offset and kickback. The comparators have thresholds set at $\pm V_{ref}/4$ and 0 for the 1.5-bit and 1-bit sub-ADCs, respectively.

B. 10b Cyclic ADC

Fig. 3.9 shows the SC implementation, and again a single-ended version is shown for clarity. The cyclic ADC [65] is implemented using a single op-amp. This ADC resolves 1.5-bit[4] in each half-clock-period to yield 10-bit resolution in 5 clock cycles, thus matching the front-end ΣΔ modulator latency. The cyclic ADC consumes 8mW, or about 17% of the total power. This power consumption can be further reduced by using a more power efficient ADC architecture, such as an SC SAR, but at the expense of more complexity.

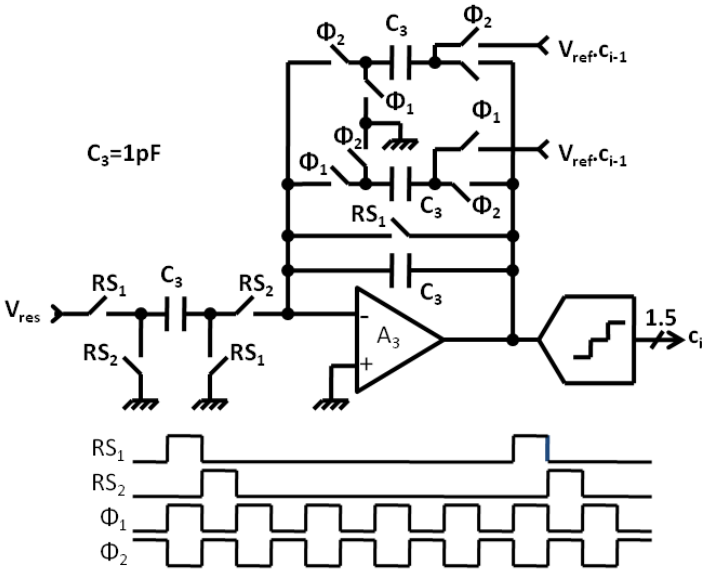

Fig. 3.9: SC implementation of 10-bit cyclic ADC

C. Digital Block

The digital block of the ADC combines all the sub-ADC outputs (a_i's, b_i's and c_i's) to give the final digital output D_{out}. The logic governing the combination, based on equation (3.2), is given by the following:

$$D_{\Sigma\Delta mod} = (5a_1 + 4a_2 + 3a_3 + 2a_4 + a_5) + \frac{b_1 + b_2 + b_3 + b_4}{4} \tag{3.10}$$

$$D_{cyclic} = 2^8 c_1 + 2^7 c_2 + 2^6 c_3 + 2^5 c_4 + 2^4 c_5 + 2^3 c_6 + 2^2 c_7 + 2^1 c_8 + 2^0 c_9 \tag{3.11}$$

$$D_{out} = 512 D_{\Sigma\Delta mod} + D_{cyclic} \tag{3.12}$$

We see that high-speed multi-bit digital integrators are not required as decimation already occurs within the ADC while the residue signal V_{res} is passed from the first stage to the second stage. This greatly simplifies implementation of the digital block.

The digital block, as described above, is a linearly weighted averaging FIR filter (Fig. 3.10). This filter operates on the final output digital code, and thus the input signal V_{in} sees the same filtering effect at the ADC output. For time-varying input signal, V_{in} in the equation (3.2) is replaced by $V_{in,fil}$, by the following filter equation:

$$V_{in,fil} = \frac{5z^{-4} + 4z^{-3} + 3z^{-2} + 2z^{-1} + 1}{15} V_{in} \tag{3.13}$$

---

[4] This includes a 0.5-bit comparator redundancy.

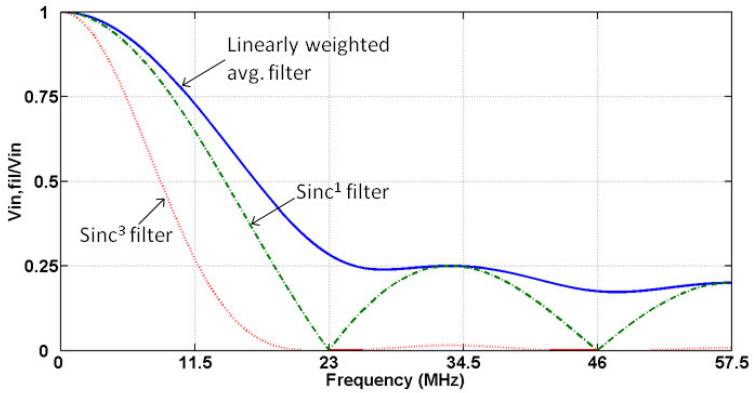

Fig. 3.10: Digital filter characteristics

Table 3.2 summarizes the difference between this linearly weighted averaging digital filter (equation (3.13)), an ideal brick-wall filter, a $sinc^1$ filter and a $sinc^3$ filter. A $sinc^3$ filter, traditionally used in second-order ΣΔ ADCs [18], has a very good noise decimation factor of 8.9 but suffers from a large worst-case pass-band droop of 11.34dB, which severely limits the usable bandwidth of the ADC. The simple linearly weighted averaging filter has a relatively poor noise decimation factor of 4.1 but has a low pass-band droop of only 2.77dB, enhancing the usable bandwidth of the ADC. To compensate for the poorer noise decimation, capacitor sizes are slightly increased to decrease thermal noise.

	Ideal Brick Wall Filter	Sinc[1] Filter	Sinc[3] Filter (e.g. second-order ΣΔ)	Linearly Weighted Averaging Filter (This work)
Attenuation @ Nyquist	0dB	3.78dB	11.34dB	2.77dB
Noise Decimation Factor	5.0	5.0	8.9	4.1
Normalized 3dB Bandwidth	1.0	0.9	0.533	1.04
Complexity	N/A	Simple	Complex	Simple

Table 3.2: Comparison between different digital filters

3.6 Measurement Results

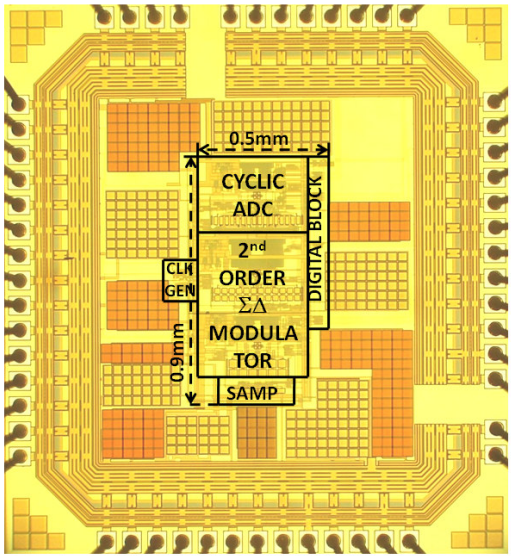

Fig. 3.11: Die micrograph

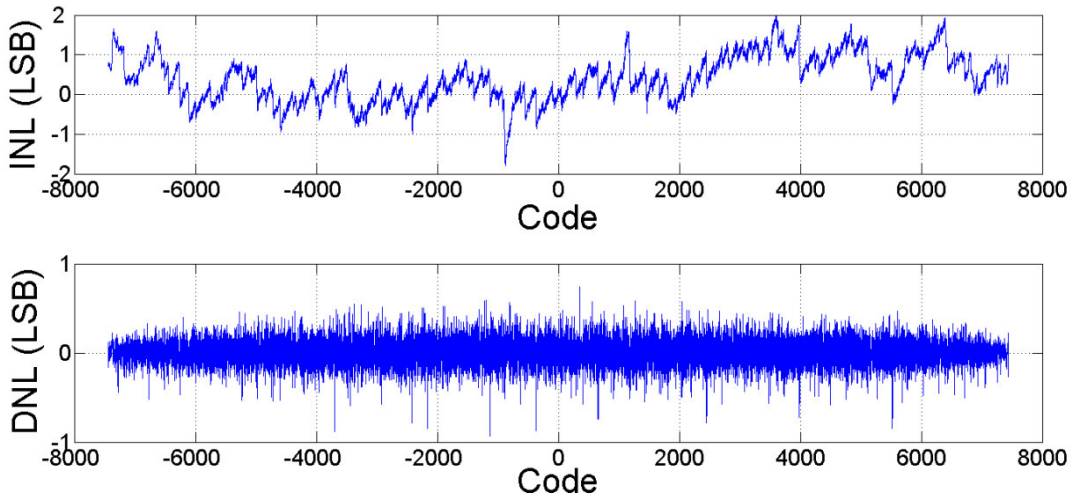

Fig. 3.12: Measured INL and DNL at 14-bit level

The prototype ADC is fabricated in a 1P6M 0.18µm CMOS process. As seen in die micrograph (Fig. 3.11), the core fits within a small 0.9mm x 0.5mm footprint. The ADC accepts a full-scale differential input signal of $2V_{pp}$. Though the ADC architecture can accept input signal larger than $2V_{pp}$, linearity suffers because of the non-linearity of the sampling switches outside this input signal range. Fig. 3.12 shows the INL and DNL plots, which indicate no missing codes at 14-bit resolution. A peak SNDR of 72dB (11.7-bit ENOB) is achieved for a 2MHz input. 8192 point FFT plots, shown in Fig. 3.13, demonstrate 87dB and 82dB SFDR for 2MHz and 8MHz input signals respectively, at -0.5dB full scale. At 0dB full-scale input, SFDR drops by about 2dB. Fig. 3.14 summarizes the measured SFDR, SNDR for varying input frequencies. SFDR and SNDR fall to 81dB and 68dB respectively for a 10MHz input signal, this is partly due to low-pass filtering discussed in section 3.5-C.

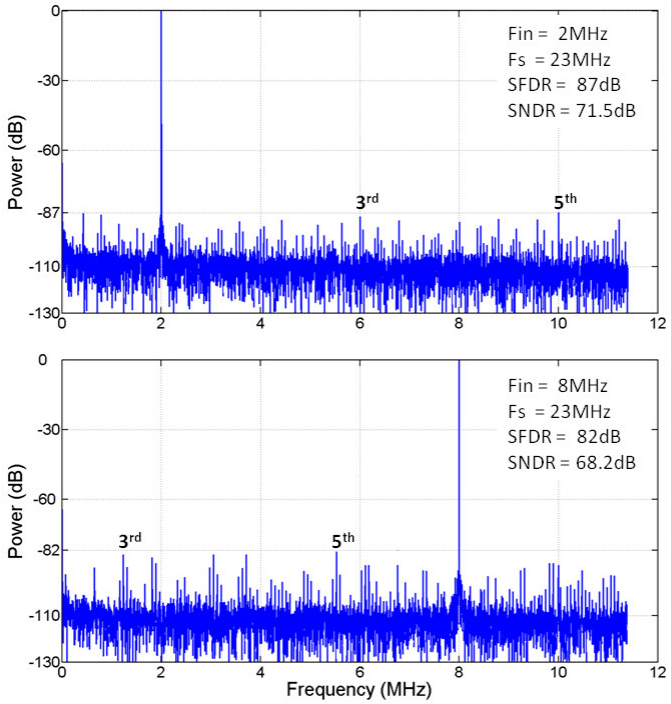

Fig. 3.13: 8192 point FFT plots for 2MHz and 8MHz inputs

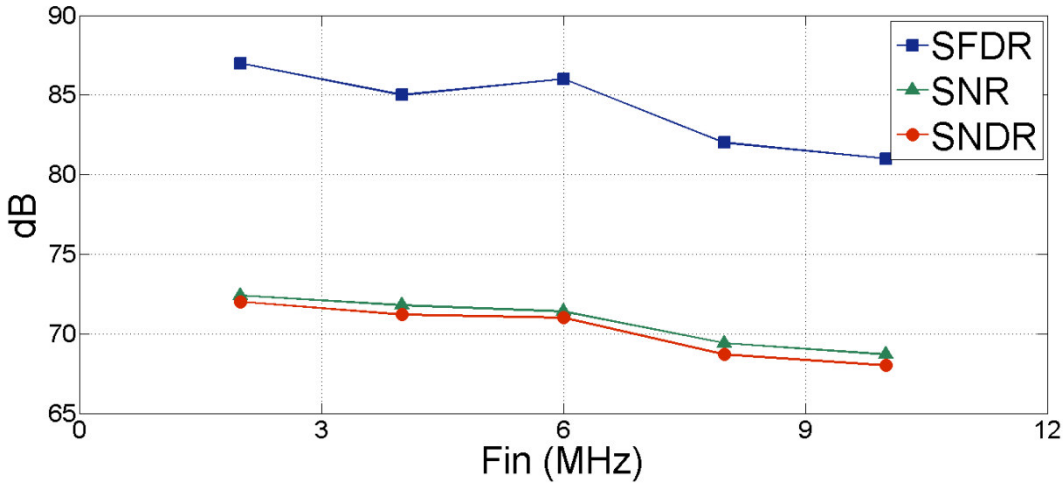

Fig. 3.14: SFDR, SNR & SNDR vs. input frequency (Fs = 23MHz)

The prototype consumes a total power (excluding I/O) of 48mW at the full conversion speed of 23MS/s. The digital block consumes 8mW, which is low for an ADC of this resolution and speed [39]. Another 8mW is dissipated by the second-stage 10-bit cyclic ADC. The first and second integrators dissipate 17mW and 14mW, respectively.

About 1mW of the total 48mW is consumed by clock generation. Table 3.3 summarizes the measured specifications of the prototype ADC.

SNDR (2MHz input)	72dB (11.7-bit ENOB)
Conversion Rate	23MS/s
Linearity (14b level)	|INL|<2LSB |DNL|<1LSB
SFDR (2MHz @ -0.5dB FS)	87dB
Input Range	2Vpp differential
Power Supply	2V
Power Consumption	40mW (Analog) 8mW (Digital)
Core Area	$0.5mm^2$
Process	0.18µm CMOS

Table 3.3: ADC specification summary

3.7 Optimum Design Model

The proposed pipelined resetting ΣΔ ADC architecture, discussed in this chapter, is suitable for high-resolution (≥12-bit) moderate speed ADCs. This section gives broad design guidelines for an optimum ADC, based on this architecture. Consider an ADC design requirements for an N-bit linearity (N≥11) with effective sampling speed of $F_{s,eff}$.

Capacitor matching of ~11-bits limits the second-stage Nyquist ADC, for back-end residual quantization, to 10-bits. The second-stage ADC conversion speed should be equal or slightly better than $F_{s,eff}$. The SAR architecture is well suited for low $F_{s,eff}$ while the pipeline architecture is better suited for higher $F_{s,eff}$.

As in a conventional N-bit pipeline ADC, with a second stage resolution of 10-bits, the first stage resolution is (N-10)-bits. The required first-stage gain is equal to $2^{(N-10)}$. Let $F_{s,max}$ be the maximum sampling speed possible. The maximum sampling speed $F_{s,max}$, in a switched-capacitor circuit implementation, is limited by op-amp settling and the resolution of the passive front-end S/H[5]. Hence, $F_{s,max}$ is dependent on the process technology used; e.g. transistor speed, parasitics, power supply, availability of low-V_{th} transistors etc. The maximum possible oversampling ratio is given by:

$$R = F_{s,max} / F_{s,eff} \tag{3.14}$$

For a first stage n^{th}-order integrator architecture, the stage-gain is given as follows:

$$G = k\prod_{i=1}^{n}(R + i - 1) \tag{3.15}$$

The factor 'k', which is usually <1, is a function of integrator gains in the actual SC implementation. In our prototype ADC architecture k=0.5. Usually k decreases as n increases, because of the larger signal swings associated with higher-order architectures. We can determine the architecture order 'n' from the required stage-gain as follows:

$$G \geq 2^{(N-10)} \tag{3.16}$$

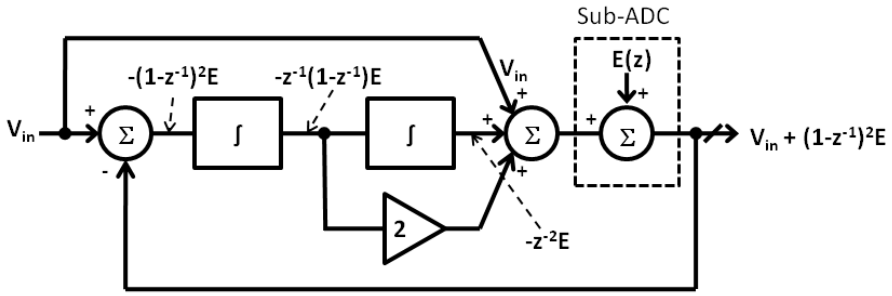

Fig. 3.15: Second-order CIFF modulator

[5] The passive front-end S/H needs to be at least (N+2)-bits accurate.

There are many implementations possible for an n^{th}-order ($n \geq 2$) resetting ΣΔ modulator. The CIFF modulator [63] is a popular architecture for implementing ΣΔ ADCs. Fig. 3.15 shows the block diagram of a second-order CIFF modulator. In this architecture, the input signal along with integrator outputs is sampled onto the sub-ADC (or quantizer). The difference of the input V_{in} and the quantizer output which contains the input signal V_{in}, results in a signal independent of V_{in} (Fig. 3.15). This difference is fed to the first integrator input. Hence only quantization error circulates in the integrators, which leads to lower input signal distortion. The sub-ADC directly sees the input signal. Thus, a front-end S/H or RC calibration is necessary to reduce error between input signal sampled by sub-ADC and first integrator. Like other higher order (order≥2) architectures, this architecture also suffers from instability [18].

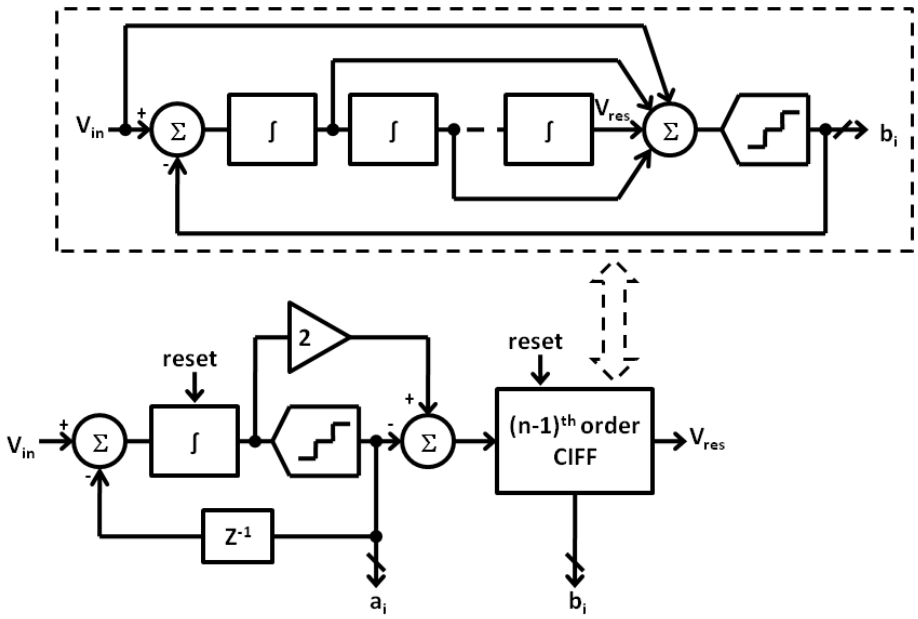

Fig. 3.16: Proposed n^{th} (≥3) order front-end resetting ΣΔ modulator architecture

For an n^{th}(≥3) order integrator architecture, a 1-(n-1) MASH architecture with the $(n-1)^{th}$ order modulator implemented using a CIFF architecture (Fig. 3.16), is proposed.

Such an architecture is beneficial because it eliminates the drawbacks of the direct n^{th} order CIFF modulator architecture and retains most of its advantages. The first-order ΣΔ modulator sampling the input signal eliminates the need for a front-end S/H (section 3.4-D). The first-order integrator gain or sub-ADC resolution can be adjusted to decrease the signal fed to the $(n-1)^{th}$ CIFF modulator, thus ensuring stability without limiting the input signal range. The $(n-1)^{th}$ CIFF modulator would retain its advantage of low distortion. In our prototype ADC, a 1-1 MASH architecture is used to implement a second-order modulator.

3.8 Conclusion

This chapter proposes a pipelined ADC architecture based on a resetting ΣΔ modulator. Analysis developed in this chapter outlines the design trade-offs and explains the advantages of this oversampling architecture over the conventional pipeline ADC architecture. Intuitive explanations are presented to show the advantages of replacing an MDAC stage in a conventional pipeline ADC with a resetting ΣΔ modulator. The proposed architecture has several advantages including lower gain-error, lower capacitor mismatch error and lower settling error. Moreover, replacing the first MDAC stage of a pipeline ADC with a resetting integrator eliminates the need for a front-end S/H stage. These advantages are not limited to high OSR architectures. Such advantages are very beneficial for the design of high-resolution, low-power, moderate-speed ADCs. This chapter also proposes architecture design guidelines (section 3.7) for optimal design of such high-resolution, moderate-speed ADCs.

The experimental prototype demonstrates the ability of such low-OSR resetting ΣΔ modulator architectures to achieve high-resolution. In this prototype, a front-end based on resetting ΣΔ modulator is pipelined with a simple cyclic ADC. The architecture achieves a calibration-free, power-efficient and area-efficient ADC design, which is often difficult to achieve in traditional ADC architectures. The architecture achieves high resolution (14-bit linearity) despite having a low OSR of 5.

CHAPTER 4

SAR ASSISTED PIPELINE ARCHITECTURE

4.1 Introduction

Many applications in electronics, especially portable battery-powered equipment, demand low-power, high-resolution and moderate-speed ADCs. An ADC based on the Successive-approximation (SAR) architecture usually requires a single comparator and a binary weighted capacitor array for implementation [20]. The use of only one comparator makes the SAR architecture the architecture of choice for low-power applications [45-47]. SAR ADCs also show good process scalability because they do not rely on analog building blocks. But the resolution and speed achieved with the SAR architecture have been limited due to limited capacitor matching, large comparator noise and their serial decision making architecture. Time-interleaved SAR architectures [48-50] have been reported for high-speed applications, but these have limited resolution because of mismatches between the parallel interleaved SAR ADCs. Pipeline ADCs [10, 21-23], on the other hand can achieve high speeds and resolutions. However pipeline ADC dissipate a considerable amount of power in their op-amps and require extensive calibration schemes to compensate for op-amp gain error and capacitor mismatch.

This chapter proposes a new, hybrid ADC architecture based on SAR and pipeline architectures. This ADC pipelines a 6-bit MDAC with a 7-bit SAR ADC. For the first stage, a "half-gain" MDAC is implemented that reduces the op-amp power and increases its open-loop gain. Use of the SAR architecture for the first stage sub-ADC, instead of the usual flash architecture, reduces power and eliminates the need of a front-end S/H. Furthermore, the use of the SAR architecture for the second stage, helps reduce power and achieve high-resolution, thus eliminating the need for more pipeline stages. The overall power consumption of the ADC is targeted at only 3.5mW.

Section 4.2 describes the ADC architecture in detail. Section 4.3 analyzes the advantages of this new architecture over conventional SAR and pipeline architectures. Finally, sections 4.4 and 4.5 present circuit details and simulated results of the prototype ADC.

4.2 Proposed ADC Architecture

The proposed ADC (Fig. 4.1) is a two-stage pipeline architecture without a dedicated front-end S/H. The first stage of the pipeline is a 6-bit MDAC, which includes a 1-bit redundancy. The second stage is a 7-bit SAR ADC.

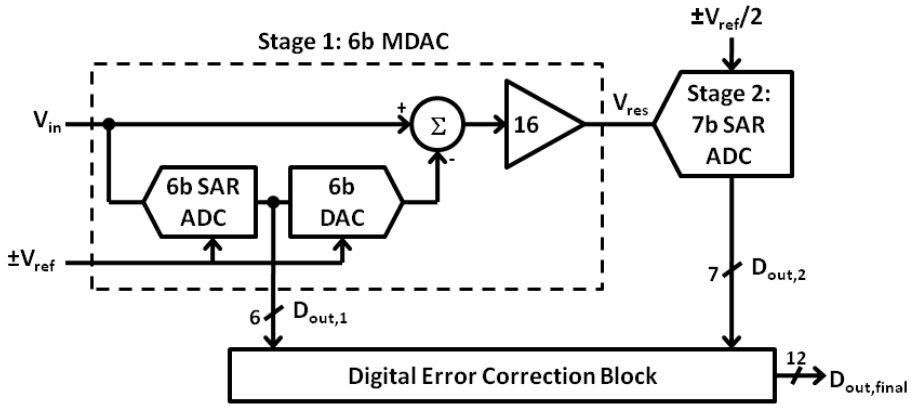

Fig. 4.1: ADC architecture

The first stage sub-ADC uses the SAR architecture, instead of the usual flash architecture, which reduces the number of comparators required from 63 to 1 and eliminates the need for an active front-end S/H. This is discussed in more details in section 4.3-A. The stage-gain of the first stage is 16 instead of the conventional gain of 2^{6-1} (=32) for a 6-bit MDAC stage. Since the implemented gain of 16 is half of the conventional gain of 32, we call this "half-gain" implementation. The half-gain MDAC implementation reduces the required op-amp bandwidth by half and can potentially increase the op-amp open-loop gain. The advantages and disadvantages of this implementation are discussed in section 4.3-B.

The second stage 7-bit ADC also has SAR architecture. Because of the half-gain implementation of the first stage, the residue signal V_{res}, has half the signal-range as compared to residue signals in conventional pipeline ADC architectures. This implies that the second-stage ADC has to quantize V_{res} to 7-bit resolution, in this "half-range". Hence "half-reference" voltages ($\pm V_{ref}/2$) are fed to the second stage to adjust for the half-gain implementation of first stage. In actual implementation, half-reference voltages are not

required. The implementation of this half-reference design is discussed in more details in section 4.3-C.

4.3 Architecture Advantages

This new ADC architecture differs from conventional pipeline architectures in a number of ways. The first stage MDAC has a large resolution of 6-bits, which enhances the ADC linearity [52]. The first stage sub-ADC has a SAR architecture, instead of the usual flash architecture, to implement this relatively-large 6-bit resolution. The alternative, a 6-bit flash would not be practical because of the large number of comparators required. The first stage also has a half-gain implementation. To adjust for the first stage half-gain implementation, the second stage has a half-reference implementation. We now discuss the advantages and disadvantages of this architecture in detail.

A. Stage 1 Sub-ADC

Fig. 4.2 shows the single-ended circuit implementation of the first stage. The actual implementation is fully differential. The CDAC for the SAR sub-ADC is the same as the input sampling capacitor array for this stage. This eliminates the need for any sampling path matching between the MDAC and its sub-ADC [53] or a dedicated front-end S/H. Use of a single comparator, instead of 63 comparators as in flash architecture, significantly reduces power consumption and area.

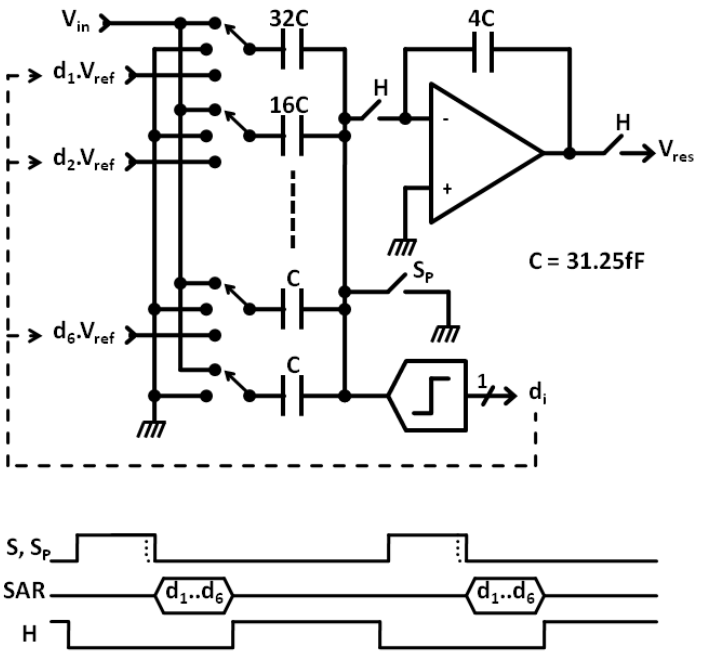

Fig. 4.2: Stage 1 MDAC implementation

A disadvantage of using the SAR architecture for the first stage sub-ADC is that a larger decision time is required by the sub-ADC, which reduces either the sample time or the hold time available for the MDAC. In our prototype ADC it is the sample time, which is reduced. The alternative of a decrease in the hold time of the MDAC, would require a larger bandwidth from the op-amp, thus increasing power consumption. The sampling time is reduced to 7.3ns, compared to the half clock period of 10ns, yet it is sufficient to achieve >12-bit resolution from the sampling circuit. The input sampling switches are boot-strapped for better linearity [64].

The 1-bit redundancy, present in the MDAC architecture, allows for large sub-ADC decision errors. This redundancy relaxes the SAR sub-ADC's CDAC top plate settling requirements, which reduces the total sub-ADC decision time. The SAR sub-ADC incorporates a fast low-power comparator with a dynamic preamplifier. Section

4.4-A describes this dynamic preamplifier based comparator in more detail. The sub-ADC needs a total decision time of 2.4ns to give a complete 6-bit decision.

B. Stage 1 "Half-Gain" Implementation

For an N-bit pipeline ADC with a large M-bit front-end MDAC resolution, a high MDAC gain of 2^{M-1} is required. But at the same time, the output of the MDAC needs to be only (N-M+1)-bit accurate. An analysis of the front-end MDAC resolution versus the required op-amp bandwidth [66], shows that since the larger gain requirement is offset by the lower accuracy requirement, the required bandwidth stays the same for different values of M. It is possible to further decrease the required op-amp bandwidth (and hence reduce op-amp power dissipation) by breaking this resolution-bandwidth equilibrium. We propose a "half-gain" architecture in which we decrease the gain of our first stage 6-bit MDAC from 32 to 16. Use of this smaller gain gives us two advantages. Firstly, the feedback factor increases from 1/33 to 1/17 (Fig 4.2). This increases the closed-loop bandwidth by a factor of about 2. Equivalently, for the same settling error the op-amp bandwidth can be decreased by a factor of about 2. Secondly, the voltage swing required at the output of the op-amp decreases. This allows us to stack more cascode transistors in the output stage of the op-amp which enhances the op-amp gain.

There are two disadvantages of this "half-gain" architecture. Firstly, this implementation leads to a smaller thermal noise budget for the second stage. This is not a problem since the second stage SAR ADC has low thermal noise[6]. Secondly, second stage sees an input signal having half the full-scale range. This is handled using a "half-reference" implementation of the second stage described below.

[6] The capacitor array for stage 2 is sized for matching and the thermal noise is very low for the chosen capacitor sizes.

C. Stage 2 "Half-Reference" Implementation

The second stage 7-bit SAR ADC is implemented as shown in Fig. 4.3. Only half the capacitors, in each binary weighted capacitor bank, are connected to the reference. Thus a half-reference is implemented without actually providing $\pm V_{ref}/2$ reference voltages. It can be seen in this half-reference implementation, the number of unit capacitors required is same as that of an 8-bit SAR ADC. Thus the circuit complexity is equivalent to that of an 8-bit SAR ADC. The advantages of having half-gain MDAC in first stage far outweigh the disadvantages of increasing the second stage complexity.

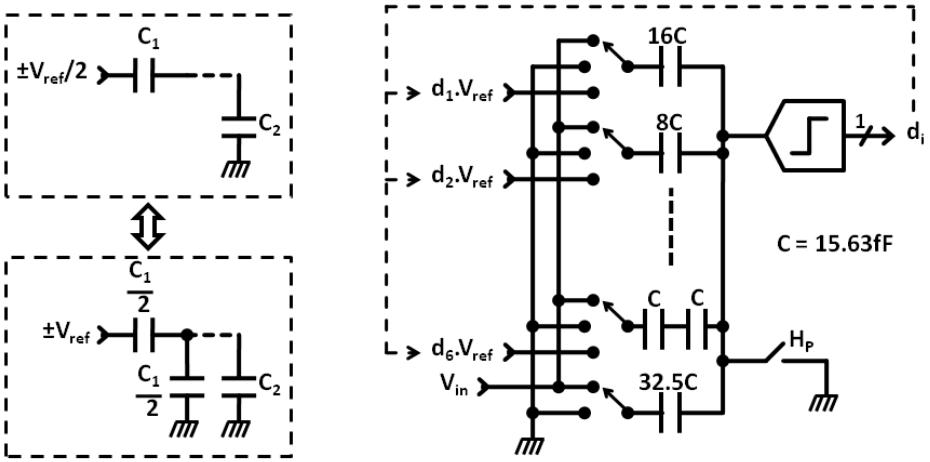

Fig. 4.3: Stage 2, 7-bit SAR ADC implementation

4.4 Circuit Details

We now discuss the detailed circuit implementation of the three main parts of the ADC; the stage 1 SAR sub-ADC comparator, the stage 1 op-amp and the stage 2 SAR ADC.

A. Stage 1 SAR Sub-ADC Comparator

Fig. 4.4 shows the circuit implementation of the first stage SAR sub-ADC comparator. The comparator is implemented as a dynamic preamplifier followed by a latch. It has a small decision time (<100ps) as compared to the dynamic comparator [67] used in [46, 47]. The preamplifier, having a gain of about 2, dissipates 1mA peak current to achieve good settling and reduce input referred offset. The preamplifier is switched on and off dynamically, so that average power consumption of the comparator is less than 100µA.

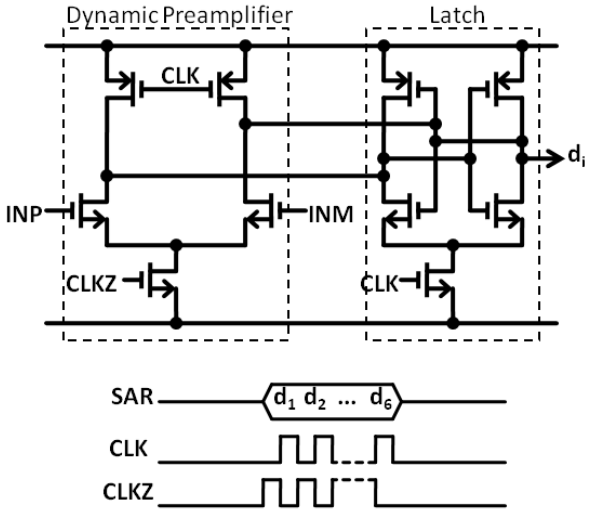

Fig. 4.4: Stage 1 SAR sub-ADC comparator

B. Stage 1 Op-Amp

The first stage MDAC op-amp (Fig. 4.5) is implemented as telescopic triple-cascode with NMOS-input and has a minimum simulated gain of 75dB. The tail transistor is biased near linear region with a V_{DS} of 70mV and all other transistors are biased in sub-threshold with a constant V_{DS} of 140mV. With this biasing scheme, the op-amp supports a maximum output swing of 390mV in 1.3V supply. This output swing is more

than sufficient due to the reduced swing requirements of the half-gain MDAC implementation.

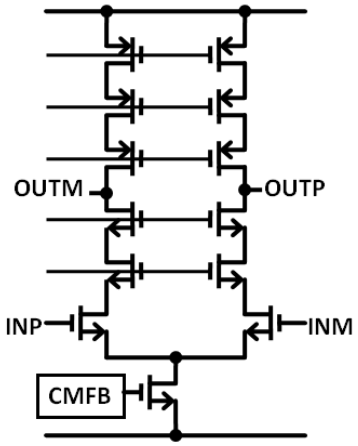

Fig. 4.5: Stage 1 op-amp

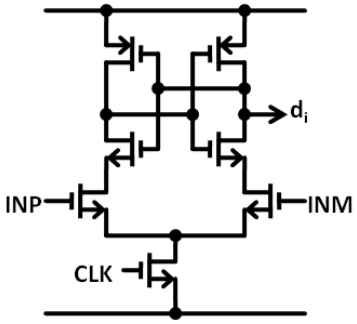

Fig. 4.6: Dynamic comparator [67]

C. Stage 2 7-bit SAR ADC

The second stage SAR ADC has a sufficient half-clock period of 10ns to give a 7-bit decision. Therefore a dynamic comparator (Fig. 4.6) [67] is used as the comparator for this ADC to reduce power consumption. The large first stage MDAC gain of 16 almost eliminates the noise contribution of the second stage. Thus the capacitors are sized for matching instead of thermal noise. The comparator noise is also of little concern because of this same reason.

4.5 Measurement Results

The prototype ADC is fabricated in a 1P9M 65nm CMOS process. The core fits within a small footprint of 0.16mm^2, as shown in the layout view and die micrograph (Fig. 4.7). The ADC accepts a full-scale differential input signal of $2V_{pp}$.

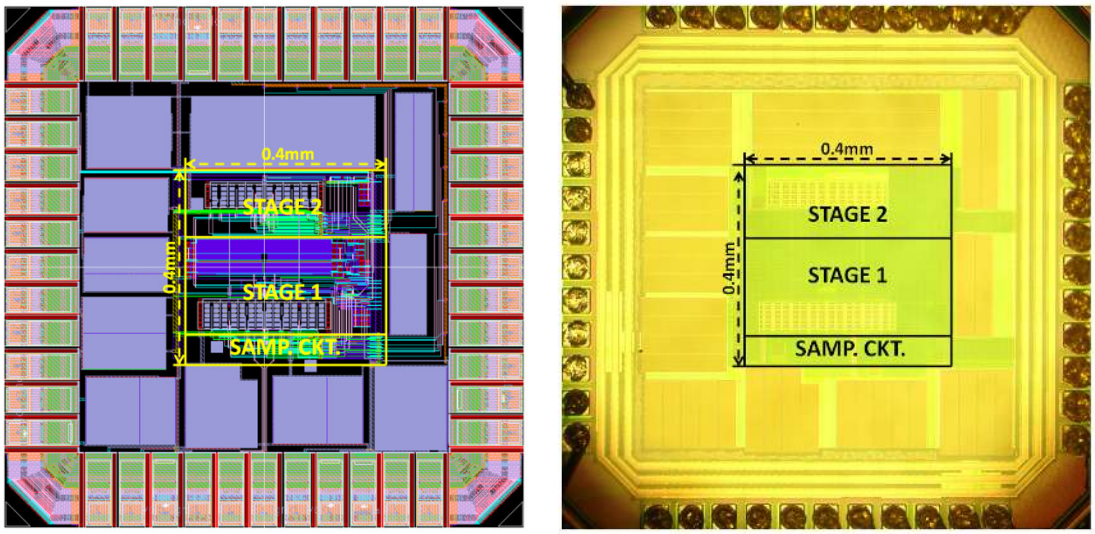

Fig. 4.7: Layout view and die micrograph

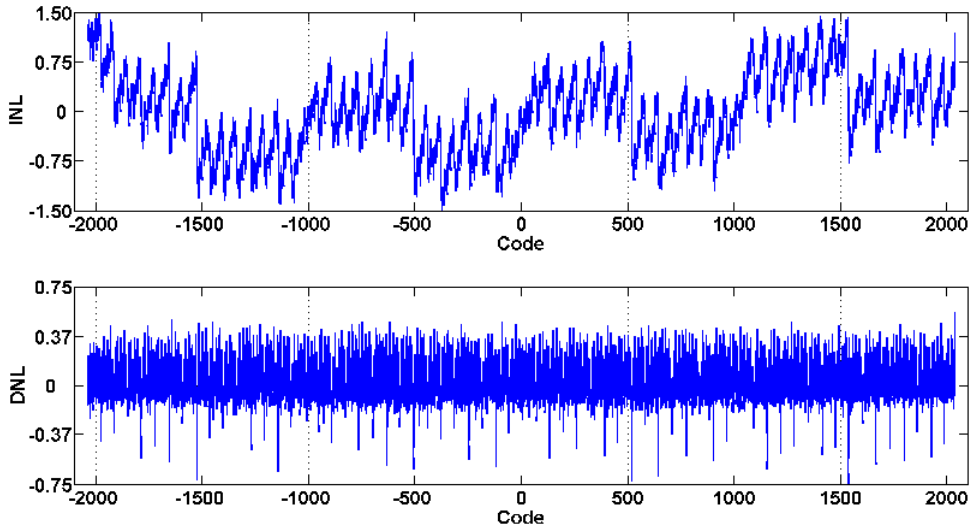

Fig. 4.8: Measured INL and DNL at 12-bit level

Fig. 4.8 shows the INL and DNL plots that indicate no missing codes at 12-bit level. A peak SNDR of 66dB (10.7b ENOB) is achieved for a 2MHz input. An 8192 point FFT plot, shown in Fig. 4.9, demonstrates 78dB SFDR for a 4MHz input signal at -0.5dB full scale. Fig. 4.10 summarizes the measured SFDR, SNDR for varying input

frequencies. SFDR and SNDR fall to 75dB and 64.4dB respectively for a 20MHz input signal. The chip consumes 3.5mW at full conversion speed of 50MS/s.

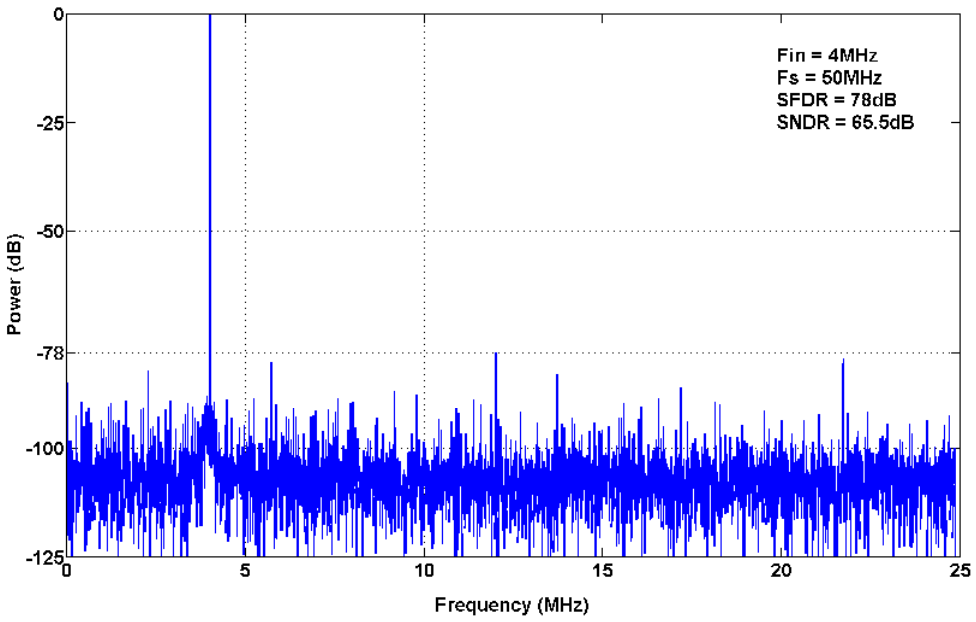

Fig. 4.9: 8192 point FFT for 4MHz input

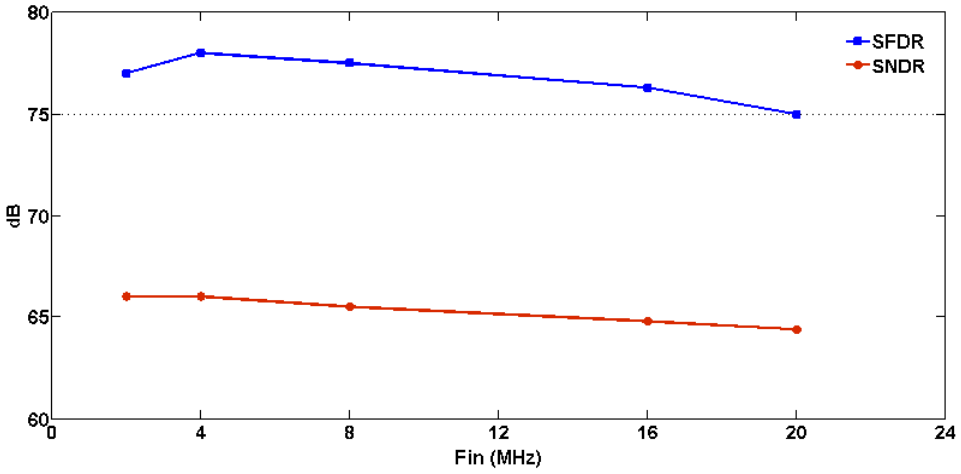

Fig. 4.10: SFDR & SNDR vs. input frequency (Fs = 50MHz)

4.6 Conclusion

This chapter proposes a new SAR-assisted two-stage pipeline ADC architecture. The first stage sub-ADC uses the SAR architecture to implement a relatively large sub-ADC resolution of 6-bit. Sharing the same input sampling capacitor array for the MDAC and SAR sub-ADC's CDAC eliminates the need for a dedicated front-end S/H. The use of a novel "half-gain" first stage MDAC increases the closed-loop bandwidth and hence decreases the power-consumption of the op-amp. This half-gain implementation, developed for the first time, also allows more cascode transistors in the op-amp, because of smaller signal swing, which enhances gain. The second stage ADC also uses SAR architecture to implement a large 7-bit resolution. This eliminates the need for more pipeline stages and reduces power consumption. A "half-reference" implementation in the second stage, to adjust for half-gain implementation of first stage MDAC, eliminates the need for actual half reference voltages. This has also been introduced for the first time.

Measured results demonstrate the ability of this simple and elegant hybrid architecture. The architecture achieves a very power-efficient and area-efficient ADC design, which is difficult to achieve with traditional ADC architectures. The architecture achieves a very low FOM of 52fJ/conversion-step, which is usually difficult to achieve for an ADC of such resolution and speed.

CHAPTER 5

CONCLUSION AND SUGGESTIONS FOR FUTURE RESEARCH

5.1 Conclusion

The conventional pipeline ADC architecture quantizes the input signal in stages. Each stage quantizes its input and passes the amplified quantization error to the next stage. The stages work in a pipeline fashion that leads to a high throughput but poor latency. This architecture has been a popular choice for implementing ADCs over a large range of sampling speeds and resolutions.

Pipeline ADCs require accurate gain blocks to amplify the quantization noise, before it is passed to the next stage. Such gain blocks are implemented with op-amps having large linear gains and supporting large output swings. Modern CMOS scaling has enabled fast transistors, but transistor gain and accuracy have suffered. Low-voltage operations in SoC implementations have further worsened this scenario.

Recent pipeline ADC publications have tried to address these issues with varying degree of success. One of the successful techniques is digital calibration [10, 21-23] in which analog inaccuracies e.g. finite op-amp gain, op-amp non-linearity, capacitor mismatches, etc. are compensated in the digital domain. All calibration techniques increase chip complexity and sometimes also power dissipation. Techniques involving

replacement of op-amps with high speed comparators [31-33] have also been reported, but accuracy and speed have been limited.

This research work aims at improving the accuracy and energy efficiency of pipeline ADCs. This work investigates calibration-free techniques to improve the ADC accuracy in modern CMOS processes. Non-conventional techniques are also investigated to reduce the overall power consumption of the ADCs. Hybrid architectures are proposed that improve the overall accuracy and energy efficiency of the pipeline ADC.

In the approach proposed in this work, the oversampling architecture is combined with the pipeline architecture to achieve a high-resolution, calibration-free ADC. This chip is a pipeline of a front-end second-order resetting ΣΔ modulator, with low-OSR of 5, and a back-end 10-bit cyclic ADC. This ADC achieves a 14-bit linearity, 11.7-bit ENOB and 87dB SFDR at an effective speed of 23MS/s. The hybrid architecture eliminates the need for a dedicated front-end S/H. The ADC dissipates 48mW, which is low for an ADC of such resolution and speed. The resetting ΣΔ architecture with a low-OSR, is used for the first time for high-speed applications.

In the second proposed approach, the SAR architecture is combined for the first time with the pipeline architecture to achieve a high-resolution low-power ADC. Large stage resolution in pipeline ADCs, enabled with the help of SAR architecture, is investigated. This prototype ADC is a 2 stage pipeline of a front-end 6-bit MDAC and a back-end 7-bit SAR ADC. The use of the SAR architecture in the first stage sub-ADC eliminates the need for a dedicated front-end S/H and reduces the power consumption. The “half-gain” MDAC implementation reduces the power dissipation and enhances gain of the first stage op-amp. Measurements show that the ADC achieves a 12-bit linearity,

50MS/s speed and a low FOM of 52fJ/conversion-step. The first stage half-gain MDAC implementation, followed by second stage "half-reference" SAR implementation, is a novel architecture introduced and developed for the first time here.

Fig. 5.1 shows the energy (power/sampling-frequency) versus resolution (SNDR) plot of all recent ADC published in leading circuits' conferences [68]. The first ADC design described in this work compares well with other high resolution ADCs published. The second ADC design described in this work is so far the most energy-efficient ADC published for such resolution and speed.

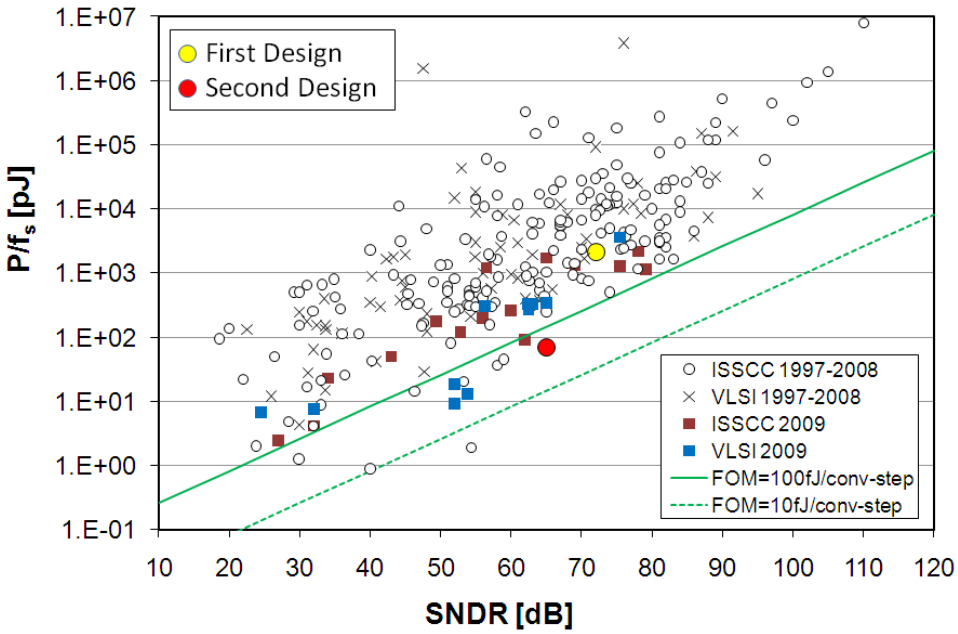

Fig. 5.1: ADC performance survey [68]

5.2 Suggestions for Future Research

There are some drawbacks of the ADC architectures proposed and bottlenecks faced during this research. Based on these drawbacks and bottlenecks, suggestions for future research are proposed in this section. They are as follows.

The first chip is a 14-bit 23MS/s ADC implemented in a 0.18μm CMOS process. With digital CMOS process reaching gate lengths of 45nm nowadays, the first suggestion for future work is a much higher speed version of the first chip in such a scaled digital CMOS processes. Sampling speeds of 500MHz or higher, would be possible in these processes, yielding a high-resolution ADC with an effective speed larger than 100MS/s.

In the second chip, the SAR sub-ADC decision time eats into the sample time of the first-stage MDAC, and because of this the architecture has speed limited to about 100MS/s. Future research might be aimed at eliminating this drawback. Flash assisted SAR sub-ADC architectures can be developed to eliminate the speed bottleneck of this architecture. For example, a coarse but fast 3-bit flash decision followed by fine 3-bit SAR decision could help this architecture to achieve speeds greater than 100MS/s.

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