Improving Quality of Manufacturing Test using Cell-Aware ATPG

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Abstract: *The existing fault models like stuck-at, small delay defect, transition and bridge fault models and their associated patterns are becoming less efficient, as the technology moves to increasingly smaller geometries. It is because traditional defect models target the faults only on IC gate boundaries, and the interconnects between the cells, but significant population of defects (perhaps up to 50%) occurs within the cells or gates which are not specifically target by existing ATPG fault models. In this paper a new ATPG methodology known as Cell-aware test is implemented explicitly to target the defects caused by cell-internal open and short faults and improve the manufacturing test quality by minimizing the test escapes. This work explains how a Cell-Aware ATPG method performs a characterization on the GDSII data of library cell`s to produce a CAT library view (UDFM), test Pattern generation and comparison between Traditional and Cell-Aware ATPG. The Cell-Aware ATPG is implemented using Tessent Testkompress, traditional ATPG is also developed to study and analyze both ATPG methodologies comparatively. Experiment results shows a significant improvement in faults being targeted at an expense of increase in pattern count and run-time. Obtained 71.28% and 59.38% test coverage for UDFM static and UDFM delay respectively. Achieved significant improvement in the test escapes with Cell-Aware Patterns when compared to traditional ATPG patterns.*

Keywords—ATPG, GDSII, UDFM, CAT, IDDQ

I. INTRODUCTION

As the transistor size reduces, the possibility of occurrence of fabrication faults increases significantly, these defects may go undetected when we use existing fault models and it leads to large number of test escapes. Reducing the DPPM becomes a major issue for any design. Furthermore, identifying manufacturing failures becomes necessary for addressing problems in the fabrication of the recent technology node. Existing fault models represent issues such as stuck-at and transition faults. In addition, small delay defect, N-detect algorithms are also developed in the effort to reduce test escapes. Stuck-at and transition fault models can target the defects on cell ports and on the interconnects, missing cell-internal defects which increase significantly in lower technology nodes.

N-detect can detect more faults than the stuck-at and transition fault models, with an expense of increment in pattern count. Small portion of faults which are internal to cell's can be targeted through IDDQ testing, where the steady state current is measured to detect the defects like shorts. Nevertheless, this is not relevant, as it can categorize the good ICs as faulty if ICs are selected based on a threshold. Few of the issues that are raised by existing methods can be solved by a Cell-Aware ATPG, which is based on post-layout transistor netlist. The cell aware fault models are generated by evaluating layout information to detect as many faults as possible within the library cell. Then extensive analog simulations are performed by considering different PVT corners to determine the detection of defects which are internal to cell's and increase their test-coverage. As anticipated, the generated CAT fault models give higher cell-internal test-coverage in comparison with the other existing fault models. But this comes at an expense of pattern count and run-time penalty.

In this paper, presented a brief summary of the Cell-Aware test methodology in Part II, advantages of the Cell-Aware ATPG over traditional ATPG is described in Section III and presented experiment results of cell aware ATPG and traditional ATPG in Section IV.

II. CELL-AWARE ATPG METHODOLOGY

The Cell-Aware ATPG methodology has two major steps. The first step is the user defined fault models (UDFM) generation flow, which is to perform once for every technology library. The technology dependent Cell-Aware fault models generation flow is shown in Fig. 1. The Cell-Aware test library view generation flow requires several backend data: GDSII view of all the technology library cells and extracted detailed standard parasitic format (DSPF). The first step in CAT library view generation flow is extraction of layout and after that an analog defect simulation, and then optimization of CAT fault models to generate the CAT library mode

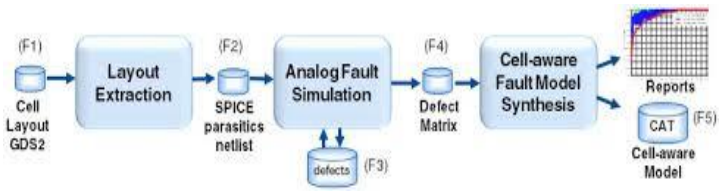

Fig. 1. CAT library view generation.

A. *Layout Extraction*

The foremost step of the library view generation flow from Figure. 1 is the extraction of layout, it takes GDSII view (F1) of each library cell and generates a SPICE transistor netlist including parasitic elements like capacitors and resistors (F2) in detailed standard parasitic format (DSPF).

B. *Analog Fault Simulation*

The next step in the UDFM creation flow is analog fault simulation. It will extract the abstracted defects from the detailed standard parasitic format SPICE netlist. The resulting abstracted faults are contained in the defects file F3 as shown in fig 1. The faults considered for generating CAT library view are open, bridge, Tleak (Transistor partially ON), Tdrive (Transistor partially Off), port-bride, port-open. Some defects highlighted on layout and schematic is shown in Fig. 2. The faults that Cell-Aware test considers are a superset of stuck-at and transition faults, because both transient

analog simulations and DC are carried out to generate UDFM's. The following stage is to do an exhaustive analog defect simulation for all the considered faults to find out the possible cell-input combination sets that target the faults. This results a fault matrix for a particular technology library cell or gate, which recapitulate each fault detection results, is stored in the file F4 in Fig. 1.

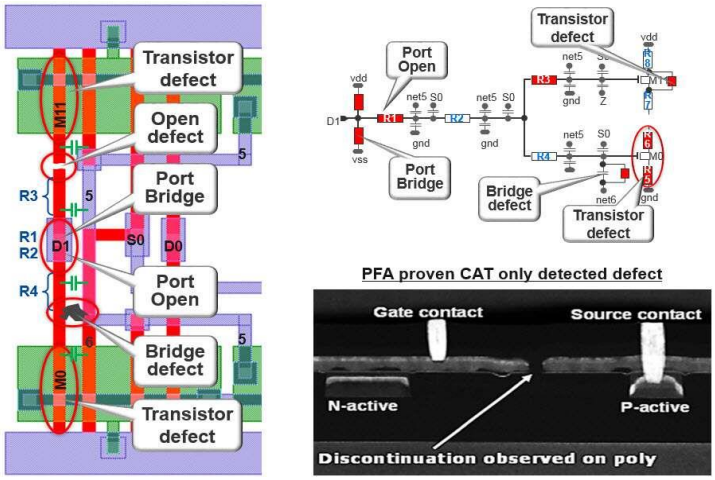

Fig. 2. Defect extraction from cell layout.

C. *CAT Fault Model Synthesis*

The next step of the user defined fault model generation flow is the synthesis of CAT fault models, it optimizes the exhaustive defect matrix which are created from previous step in order to generate the corresponding UDFM's, which are stored in file F5. The Cell-Aware fault model file has one or more alternative test stimulus for each fault which are internal to cells. This ensures that Cell-Aware ATPG has the flexibility to pick between all alternative test stimulus to catch certain cell internal faults.The next major part of the Cell-Aware ATPG methodology is well-known design flow to generate CAT patterns here we use Cell-Aware ATPG instead of normal ATPG**,** which is shown in Fig. 3**.**

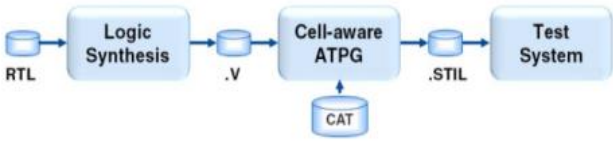

Fig. 3. Well-known design flow.

Cell-Aware ATPG is a defect-based ATPG that takes the post-layout and technology-dependent CAT library view to create more efficient test pattern sets to significantly bring down the fault level of shipped ICs. Cell-Aware test is able to generate test vectors for very large designs.

III. TRADITIONAL ATPG AND CELL-AWARE ATPG COMPARISON

In case of traditional methods, front-end models are used to generate traditional ATPG fault models. These fault models are used for all technology libraries regardless of the library features like threshold voltage, drive strength, channel length, extraction temperature or cell height. This

causes the same test patterns to be created irrespective of the cell variant or technology library used. Also, these traditional fault models will detect faults only at cell boundaries and on interconnects. But in recent technology nodes half of the faults are from internal to the cells. These cell internal faults may go undetected when we use normal ATPG patterns, hence it leads to a large number of test escapes.

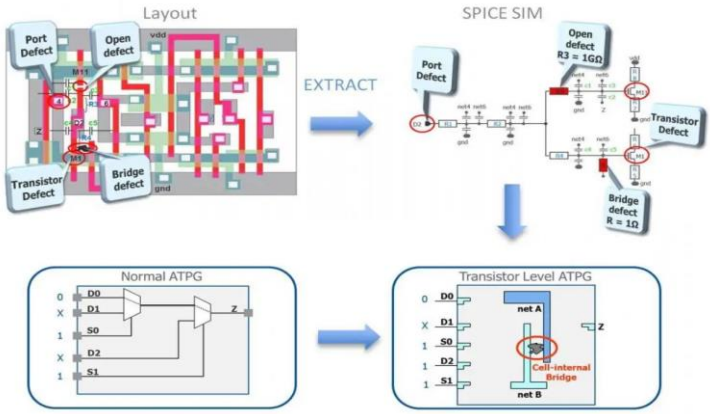

Fig. 4. Traditional and Cell-Aware ATPG Faults.

Cell-Aware fault models are generated to target the defects specifically cell internal defects. The cell Aware ATPG which is founded on post-layout transistor netlist improves the manufacturing test quality and minimize the test escapes. The pattern count is greater in case of Cell-Aware ATPG with respect to stuck-at and transition patterns. Since Cell-Aware fault models that are generated while varying the cell parameters and library features. Fig. 4 shows defects targeted by traditional and CAT fault models.

IV. EXPERIMENTAL RESULTS

Implemented Cell Aware ATPG on SOC subsystem in Tessent Testkompress to generate patterns. The cell Aware ATPG results for CAT static and CAT dynamic are shown in below Table 1. Test coverage obtained for Static faults is around 71.28% and for dynamic faults it is around 59.38%. Pattern count is almost double in case of CAT Dynamic as compared to CAT Static. ATPG run-time is also more in case of CAT Dynamic as compared to CAT Static.

TABLE 1. Cell-Aware ATPG Statistic Report details.

	CAT Static	CAT Dynamic
Fault Count	148155899	180637181
Test Coverage	71.28%	59.38%
Pattern Count	18309	38274
Run Time (sec)	157128.6	3017391.2

The Traditional ATPG is also implemented on same SOC subsystem and its results are shown in table 2. for stuck-at and transition faults. After observing the above ATPG statistics results of both CAT and Traditional

TABLE 2. Traditional ATPG Statistic Report details.

	Stuck-at	Transition
Fault Count	20995622	20995622
Test Coverage	83.44%	80.42%
Pattern Count	11914	32753
Run Time (sec)	35716.4	1484815.1

ATPG, the number of patterns and ATPG run-time of CAT increases significantly when compared to normal ATPG. The achieved test coverage for Traditional ATPG is more when compared to Cell-Aware ATPG. Gate level simulations are performed on the design to validate CAT patterns as well as traditional ATPG patterns, simulations are passed. Both ATPG methodology Patterns are also passed on the tester (ATE) and achieved significant improvement in the test escapes with Cell-Aware Patterns when compared to traditional ATPG patterns.

V. CONCLUSION

The implementation of Cell-Aware ATPG on soc subsystem is carried out with the motive to improve the manufacture test quality by minimizing test escapes. Mentor Graphics Tessent Testkompress tool is used for test pattern generation. The UDFM's (cell-aware models) generated by CAT library view flow is given to the ATPG tool as one of the inputs to target the faults, specifically cell internal faults. The traditional ATPG is also implemented on the same soc subsystem to study and analyze comparatively. From the analysis of the results, it is seen that there is a significant increase in fault count, run time and pattern count in case of Cell-Aware ATPG than normal ATPG.

From the observations made on results, it can be noted that the reason for increase in fault count in case of CAT is, it will also target the faults which are internal to the cells along with faults on the cell boundaries and on interconnects. The results derived by executing the ATPG framework is led to conclude that the objective of developing ATPG framework comprising of tests the cell internal faults and significant improvement in the test escapes, has been achieved. The future scope of CAT ATPG is, to optimize the test patterns and improvement in the ATPG tool run time.

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